Rev. 0.10

Data Sheet

S6D04D1X21

Preliminary

MOBILE DISPLAY DRIVER IC

TRADEMARK & COPYRIGHT INFORMATION

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REVISION HISTORY

Ver.	Date	History
0.00	2008-12-30	- Initial Release
0.10	2009-01-14	- table. 21 RGB interface AC characteristics is modified

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Preface

About This Reference Specification

This document is to provide a complete reference specification of S6D04D1 IC design. It also provides useful information to those who works on a panel module or a set.

IMPORTANT NOTICE

Precautions against Light

The conductivity of a semiconductor is strongly influenced by electro-magnetic radiation such as visible light, infrared light, ultraviolet light, or gamma radiation. When light is absorbed, electron-hole pairs are generated raising the conductivity of the material, eventually altering the electrical characteristics of the IC. Therefore, if the packages that expose IC's to external light sources, such as COB, COG, TCP, and COF, are used, effective means to shield the IC from the light coming in all directions – top, bottom, and the sides – must be devised. Full observation of the following precautions is strongly recommended.

1. Make sure that the IC and substrate (board or glass) are protected from a stray light.
2. Always test and inspect products under the environment with no light penetration.

CHAPTER 1

OVERVIEW

1 OVERVIEW

1.1. INTRODUCTION

S6D04D1 is a single-chip display driver IC for a TFT-LCD panel. Integrated on this chip are source drivers with built-in memory, gate drivers and power sources. S6D04D1 can support a TFT-LCD panel up to a resolution of 240-RGB x 432-dot graphics with 16M-color. S6D04D1 also supports various types of peripheral interface such as 80-series MCU interface (8-/9-/16-/18-/24-bits data), 3-wire 9bit / 4-wire 8bit serial interface, and MDDI(Mobile Display Digital Interface) S6D04D1 supports various types of RGB interface (24-/18-/16-/8-/6-bits data).

The Integrated on-chip functions that are described in this document include:

- Power saving: It reduces the overall power consumed in a TFT-LCD panel module.
- Internal GRAM:
- Internal DC/DC voltage converter
- MIE (Mobile Image Enhancement) functions

S6D04D1 features several power saving functions to reduce the overall power consumed in a TFT-LCD panel module: S6D04D1 operates at low voltage and has internal GRAMs that can store 240-RGB x 432-dot 16M-color image data. In addition, it has an internal DC/DC voltage converter that generates various voltages needed for driving the TFT-LCD panel by using breeder resistors and the voltage followers.

1.2. PRODUCT OPTIONS

S6D04D1 offers more than one option in order to meet customer-specific functions from the customers.

Table 1 describes its functions.

Table 1. List of S6D04D1 options

Options	Remarks
-X21	Reference design of S6D04D1 which supports various Host interfaces

1.3. FEATURES

S6D04D1 offers the following key features:

- **A single-chip TFT-LCD Controller/gate driver/source driver with built-in Graphic RAM**
- **Supported Display panel resolution: 240*R/G/B (H) * 432 (V) , 240*R/G/B (H) * 400 (V) & 240*R/G/B (H) * 320 (V)**
- **Integrated 2,488,320bit of graphic RAM (GRAM)**
  - **GRAM configuration: 240 x 432 x 24-bits = 2,488,320bits**
- **Supported Interfaces**
  - **3-wire 9-bit data, 4-wire 8-bit data serial interface (for RGB parallel Interface)**
  - **8-/9-/16-/18-/24- bit interface with 80-Series MCU (so called 80-Series)**
  - **VSYNC I/F**
  - **MDDI(Mobile Display Digital Interface)**
- **Outputs**
  - **Common electrode output**
  - **Gate outputs**
  - **Source outputs**
- **Color Display mode**
  - **Full color mode (Idle mode off): 16M / 260k / 65k colors**
  - **Reduced color mode (Idle mode on): 8-colors (3-bit binary mode)**
- **Color modes on the display host interface**
  - **16-bits/Pixel: RGB= (565) using the 1,843k bit frame memory**
  - **18-bits/Pixel: RGB= (666) using the 1,843k bit frame memory**
  - **24-bits/Pixel: RGB= (888) using the 1,843k bit frame memory**
- **Display features**
  - **Partial display mode**
- **Driving scheme: line inversion & frame inversion**
- **MIE (Mobile Image Enhancement) functions**
  - **Adaptive luminance/contrast enhancement function.**
  - **Reduce the power consumption of backlight.**
- **SE (Sharpness Enhancement) functions**
- **On-chip functions**
  - **Voltage Boosters**
  - **Adjustable VCOM voltage source generator**
  - **An oscillator for display clock generation & Timing generation**
  - **Factory default value (Contrast, Module ID, Module version, etc) can be stored inside IC**
  - **MTP (Multi-time Programmable) Memory**
  - **MTP initialization & program voltages are generated automatically from the built-in power circuit.**
  - **Each 8-bits product ID1, ID2, ID3**

- 6-bits VCM Offset adjustment
- Each 5-bits for VML, GVD Offset adjustment
- 1 bit for MTP writing protection

- **Voltage Supplies**
  - 2.3V – 3.3V for VCI, supply voltage for Analog blocks
  - 1.65V – 3.3V for VDD3, Supply voltage for I/O
- **Output voltage levels**
  - 2.5V to 5.0V for GVDD, Source output voltage
  - AVDD, Power supply for driver circuit (Note 1)
  - Maximum 6.0V for VCOM, Common electrode output voltage
  - 11.25V to 16.50V for VGH, Positive Gate output voltage (Note 2, Note 3)
  - -13.75V to - 6.75V for VGL, Negative Gate output voltage (Note 2)
- **CMOS compatible inputs**
- **COG package**
- **Operating temperature range: -40℃ to +85℃**

Note1. Available AVDD Min: 4.5V at VCI1 = 2.25V, Max=6V at VCI1 = 3V

Note2. |VGH| & |VGL| Min: VCI1 = 2.25V, |VGL| Max: VCI1=2.75V, |VGH - VGL| Max = 30V

Note3. Maximum |VGH| should be lower than or equal to 16.5V in normal operating condition, regardless of VCI1 & BT settings.

Note4. Blank display means: For normally white panel, the blank display indicates white display. For normally black panel, the blank display indicates black display

1.4. BLOCK DIAGRAM

1.4.1. Module Level

Figure 1 shows the block diagram of a mobile display panel module and related interface signals required by set makers and module makers. Level I interface signals represent the requirements by a set manufacturer that must be complied to by a module manufacturer. Level II interface signals, on the other hand, represent the requirements from the module manufacturer to that, typically, a driver IC manufacturer must comply.

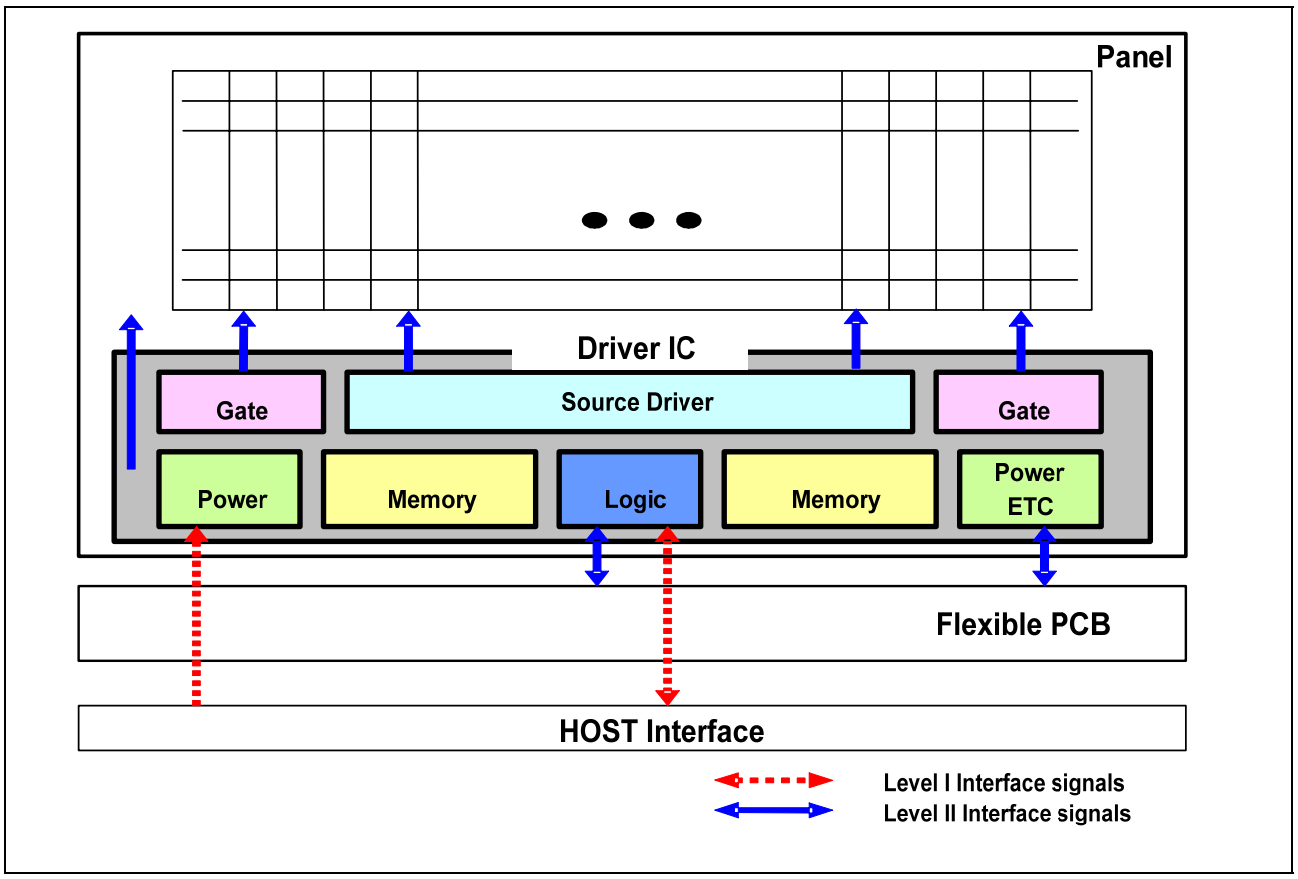


Figure 1. Interface signal flow of a mobile display panel module.

There are also Level III signals which are for internal use only for the driver IC itself. These signals may not necessarily be released to the customer since they are designed for a specific manufacturing purpose and are supposed to be hidden features.

The reference specifications shown in this document serve only as guidelines to Level I and II interface signals only; the reason being that a specification related to Level I and II considers the parasitic and design requirements within the flexible PCB used by a display module maker. IC specification will offer related information among Level I/II on how each interface signals relates to each other.

1.4.2. Functional Block Diagram of the IC

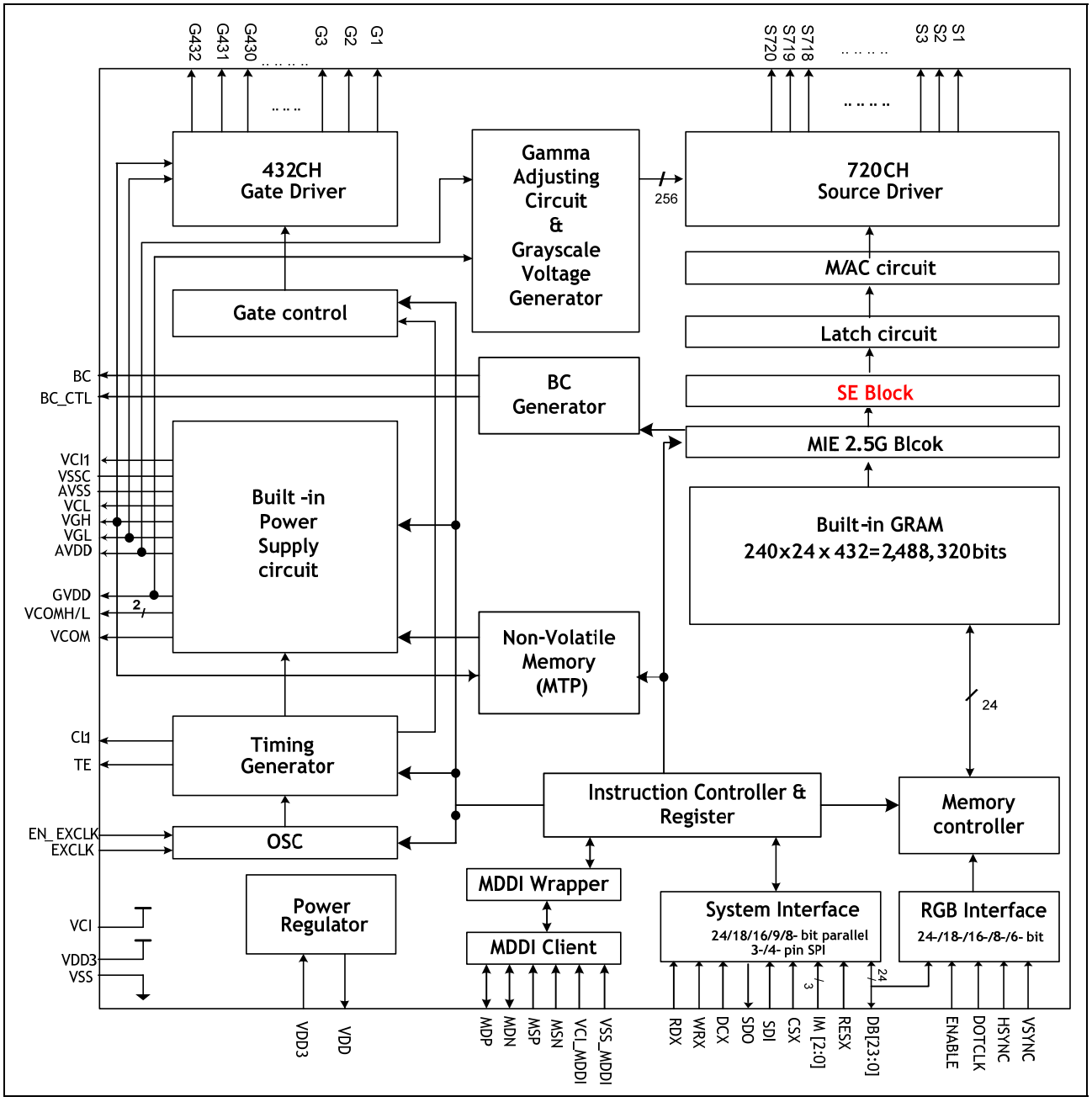


Figure 2. S6D04D1 block diagram

1.5. PAD INFORMATION

1.5.1. Configuration of Signal Pads

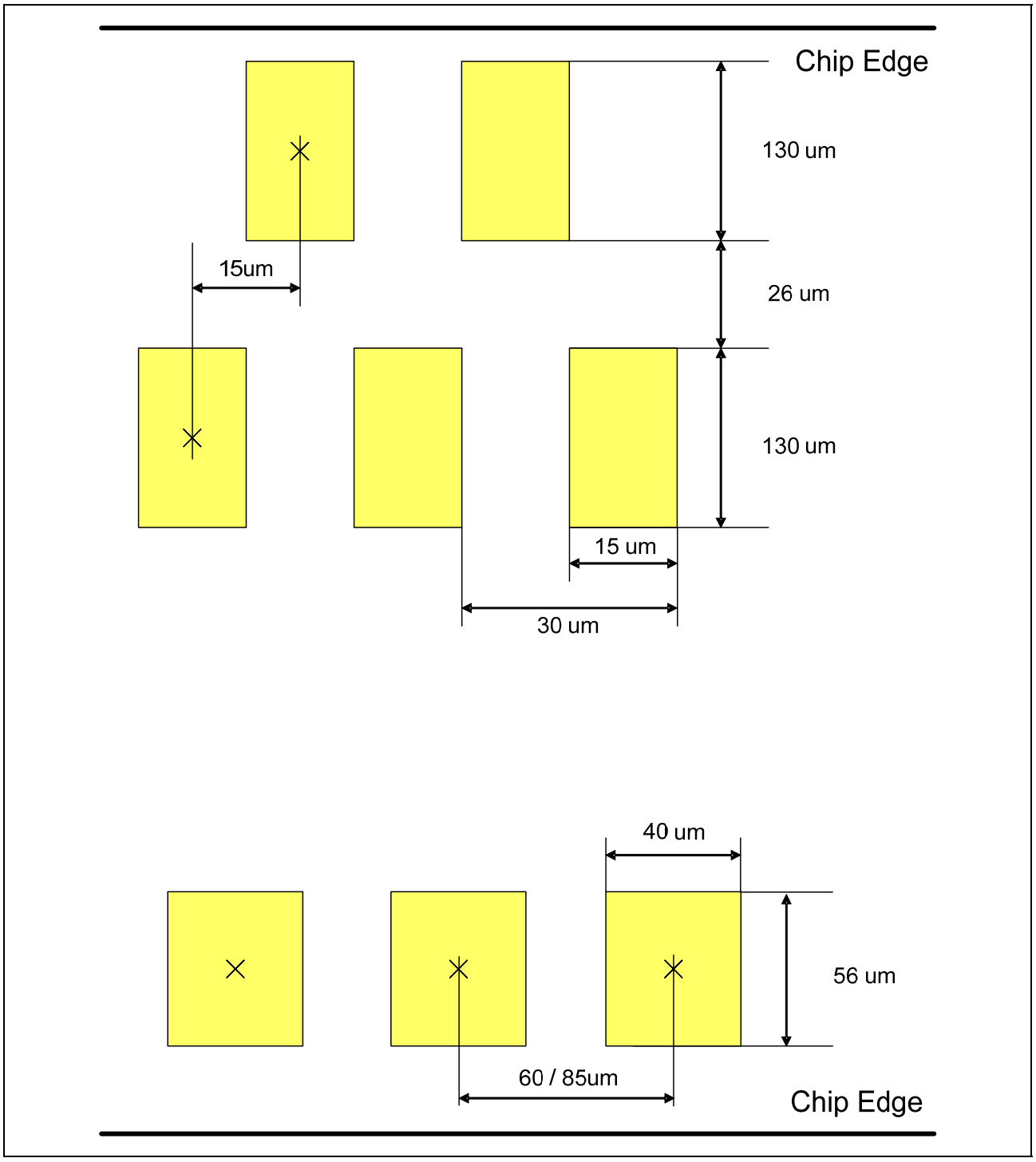


Figure 3. S6D04D1 pad configuration

Note. Pattern Surface

1.5.2. Bump

Table 2. S6D04D1 pad dimensions

Item	Pad No.		Size		Unit
			X	Y	
Chip size	-		18,280	1,224	μm
Pad pitch	Input Side	(1~166, 191~192, 196~286)	60		
		(166~191, 192~196)	85		
	Output Side		15		
Bumped pad top size	Input side		40±2	56±2	
	Output side		15±2	130±2	
Bumped pad height	Height		15±3 (in wafer)		
	Tolerance in chip		Under 2		
	Dimple height		Under 2		
Chip thickness	-		300		

Note1. Scribe lane 80um include in this die size

Note2. Wafer thickness can be varied based on the customer's need

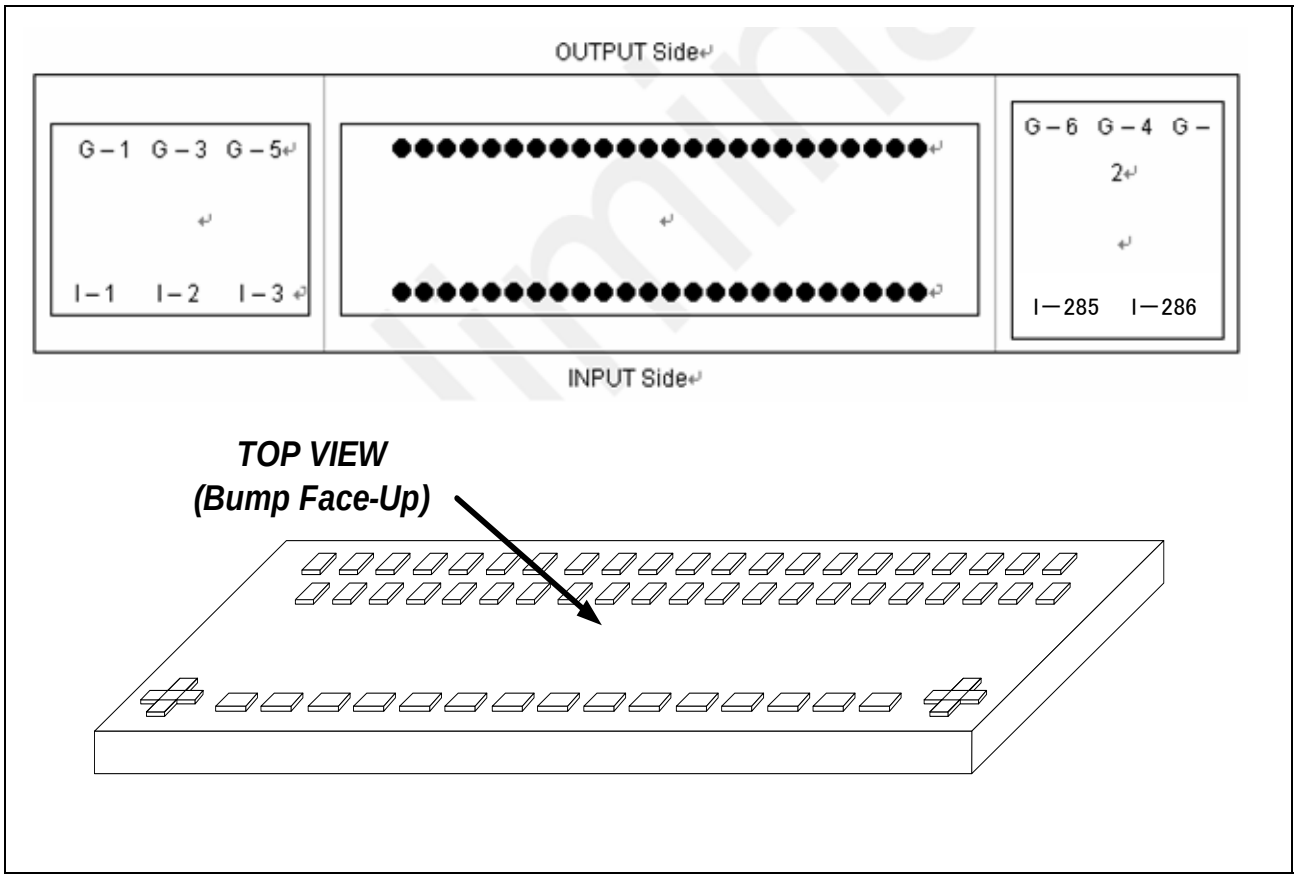


Figure 4. Pad arrangement layout

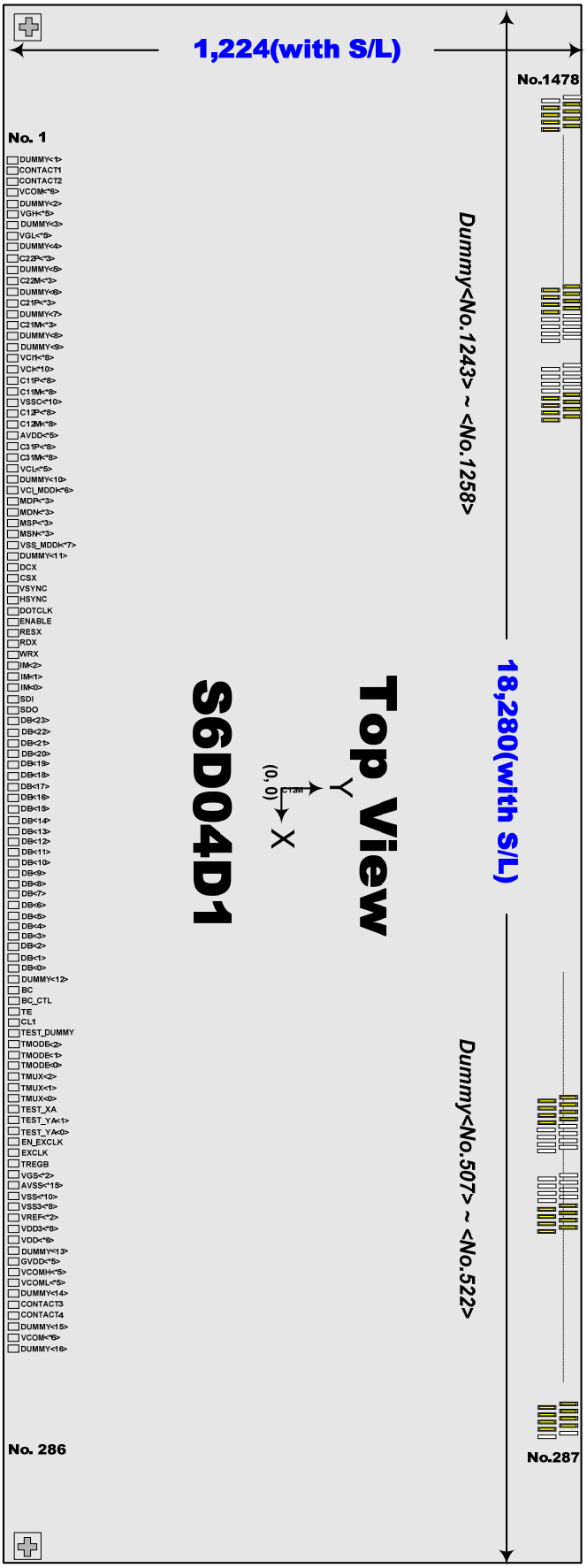


Figure 5. Chip outline

1.5.3. Align Key

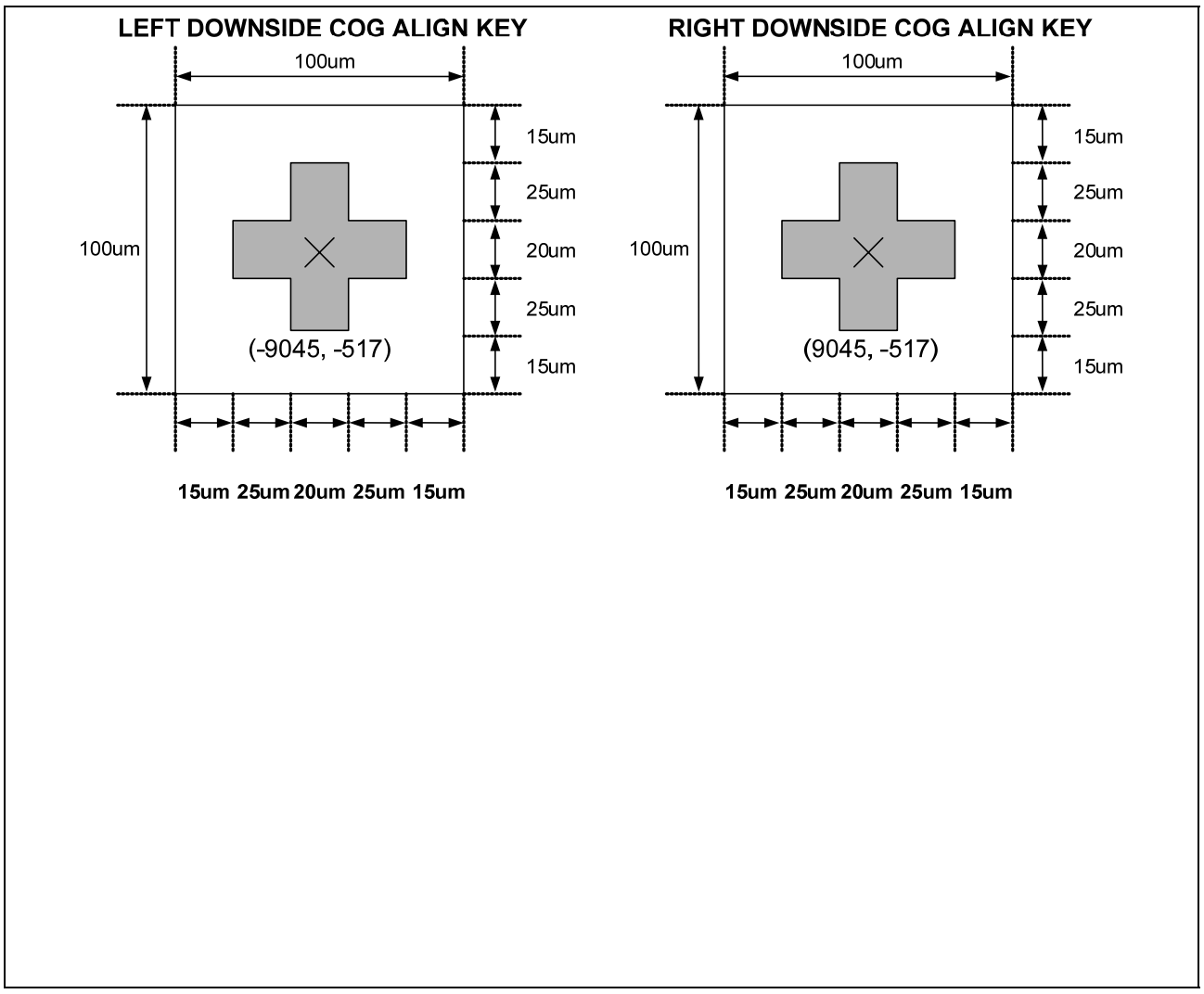


Figure 6. COG align key configuration and coordinate

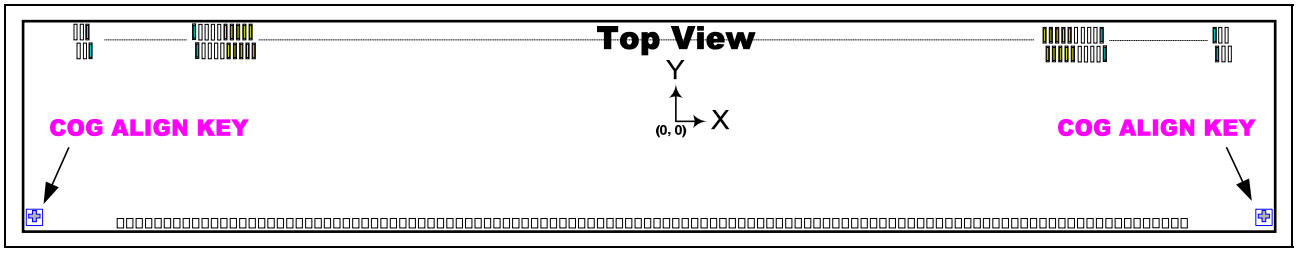


Figure 7. COG align key arrangement layout

1.6. DESCRIPTION OF SIGNAL PADS

1.6.1. Pads for Power Supplies

Table 3. Pads for power supplies

Name	I/O	Description
VDD	O	Voltage regulator output for internal memory and logic circuit. Do not apply any external power to this pad. Connect a capacitor for stabilization.
VDD3	P	Power supply for I/O block provided from outside
VCI	P	Power supply for analog and voltage booster block.
VCI_MDDI	I	Power supply ffor MDDI I/O block. Must be connected to VCI level.
AVSS	P	GND for analog circuits.
VSSC	P	GND for voltage booster circuits.
VSS	P	GND for logic circuits.
VSS3	P	GND for for I/O block provided from outside
VSS_MDDI	I	GND for MDDI I/O block.
AVDD	O	Internally generated voltage output pad for source driver block. Output voltage of 1st booster circuit (=2 x VCI1) Input voltage to 2nd booster circuit. Connect a capacitor for storage function.
VCI1	O	Reference input voltage for 1st booster circuit & 3rd booster circuit . Connect a capacitor for stabilization. <note 1> VCI1 cannot exceed 3V
VGH	O	Positive power output of the 2nd booster circuit. Gate “ON” level voltage. Connect a capacitor for storage function.
VGL	O	Negative power output of the 2nd booster circuit. Gate “OFF” level voltage. Connect a capacitor for storage function.
VCL	O	3rd booster output voltage. Power supply for generating VCOML block. Connect a capacitor for storage function.
VGS	I	Reference voltage input for grayscale voltage generator. Connect an external resistor or to the system ground.
VREF	O	Reference voltage for generating GVDD voltage.
GVDD	O	Reference voltage input for grayscale voltage generator. Reference voltage input for VCOMH / VCOML voltage generator. An internal register can be used to adjust the GVDD voltage. Connect a capacitor for stabilization.

Table 4. Pads for power supplies (continued)

Symbol	I/O	Description
VCOMH	O	High level output voltage of VCOM. An internal register can be used to adjust the VCOMH voltage. Connect a capacitor for stabilization.
VCOML	O	Low level output voltage of VCOM. An internal register can be used to adjust the difference voltage between VCOMH and VCOML. Connect a capacitor for stabilization.

Table 5. Pads for power supplies (continued)

Symbol	I/O	Description
VCOM	O	Power supply pad for the TFT- display common electrode. Charge recycling method is used with VCI voltage. Connect this pad to the TFT-display common electrode
C11P C11M C12P C12M	-	Connect the charge-pumping capacitor for generating AVDD level.
C21P C21M C22P C22M	-	Connect the charge-pumping capacitor for generating VGH, VGL level.
C31P C31M	-	Connect the charge-pumping capacitor for generating VCL level.

1.6.2. Signal Pads for Logic Interface

Table 6. Signal pads for logic interface

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>MDP/MDN</td><td>I/O</td><td>Differential Data Input/output pads for MDDI. When the forward link activates,MDP/MDN receive data form host. When the reverse link activates, MDP/MDN transmit data to host.
If MDDI is not used, this pad should be unconnected.</td></tr>
<tr><td>MSP/MSN</td><td>I/O</td><td>Differential Strobe input pads for MDDI. These pads always receive strobe data regardless of link direction.
Also these pads are output pads for MDDI failsafe function.
If MDDI is not used, thse pad should be unconnected.</td></tr>
<tr><td>IM[2:0]</td><td>I</td><td>Selects the interface mode.
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface mode</th><th>DB pad</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>80 MCU 24-bit Parallel I/F</td><td>DB[23:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>80 MCU 18-bit Parallel I/F</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>80 MCU 16-bit Parallel I/F</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>80 MCU 9-bit Parallel I/F</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>80 MCU 8-bit Parallel I/F</td><td>DB[7:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data Serial interface</td><td>Refer to table7</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data Serial interface</td><td>Refer to table7</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>MDDI</td><td>-</td></tr>
</table></td></tr>
<tr><td>RESX</td><td>I</td><td>Active low. This signal is used to reset the device and must be applied to initialize the chip properly.</td></tr>
<tr><td>CSX</td><td>I</td><td>Chip select signal. Activate MCU interface mode by setting this to ‘low’. This pad can be permanently connected to “Low” in MCU interface mode only.
If not used, connect this pad to either VSS or VDD3.</td></tr>
<tr><td>DCX</td><td>I</td><td>Display Data/Command selection signal in parallel interface
- DCX=’1’: Display Data or Command parameter.
- DCX=’0’: Command Index.

Serial interface clock (SCL) in 3-wire/9-bit serial data interface.</td></tr>
<tr><td>RDX</td><td>I</td><td>Read Enable in 80-parallel interface.
If not used, connect this pad to VDD3.</td></tr>
<tr><td>WRX</td><td>I</td><td>Write Enable in 80-parallel interface.
If not used, connect this pad to either VSS or VDD3.

Serial interface clock (SCL) in 4-wire/8-bit serial data interface.</td></tr>
</table>

Table 7. Signal pads for logic interface(continued)

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>DB[23:0]</td><td>I/O</td><td>Data Bus. assignment of data bus in table
<table>
<tr><th colspan="4">Interface Mode</th><th colspan="2">Description</th></tr>
<tr><th>IM</th><th>RIM</th><th>VFPF (Note)</th><th>Interface Mode</th><th>Index</th><th>Data</th></tr>
<tr><td>100</td><td>X</td><td>X</td><td>80 MCU 24-bit Parallel</td><td>DB[7:0]</td><td>DB[23:0]</td></tr>
<tr><td>011</td><td>X</td><td>X</td><td>80 MCU 18-bit Parallel</td><td>DB[7:0]</td><td>DB[17:0]</td></tr>
<tr><td>010</td><td>X</td><td>X</td><td>80 MCU 16-bit Parallel</td><td>DB[7:0]</td><td>DB[15:0]</td></tr>
<tr><td>001</td><td>X</td><td>X</td><td>80 MCU 9-bit Parallel I/F</td><td>DB[7:0]</td><td>DB[8:0]</td></tr>
<tr><td>000</td><td>X</td><td>X</td><td>80 MCU 8-bit Parallel I/F</td><td>DB[7:0]</td><td>DB[7:0]</td></tr>
<tr><td rowspan="5">101</td><td>0</td><td>111</td><td>3-wire 9-bit data Serial Interface & RGB 24-bit I/F</td><td>SDI</td><td>DB[23:0]</td></tr>
<tr><td>0</td><td>110</td><td>3-wire 9-bit data Serial Interface & RGB 18-bit I/F</td><td>SDI</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>101</td><td>3-wire 9-bit data Serial Interface & RGB 16-bit I/F</td><td>SDI</td><td>DB[15:0]</td></tr>
<tr><td>1</td><td>111</td><td>3-wire 9-bit data Serial Interface & RGB 8-bit I/F</td><td>SDI</td><td>DB[7:0]</td></tr>
<tr><td>1</td><td>110</td><td>3-wire 9-bit data Serial Interface & RGB 6-bit I/F</td><td>SDI</td><td>DB[5:0]</td></tr>
<tr><td rowspan="5">110</td><td>0</td><td>111</td><td>4-wire 8-bit data Serial Interface & RGB 24-bit I/F</td><td>SDI</td><td>DB[23:0]</td></tr>
<tr><td>0</td><td>110</td><td>4-wire 8-bit data Serial Interface & RGB 18-bit I/F</td><td>SDI</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>101</td><td>4-wire 8-bit data Serial Interface & RGB 16-bit I/F</td><td>SDI</td><td>DB[15:0]</td></tr>
<tr><td>1</td><td>111</td><td>4-wire 8-bit data Serial Interface & RGB 8-bit I/F</td><td>SDI</td><td>DB[7:0]</td></tr>
<tr><td>1</td><td>110</td><td>4-wire 8-bit data Serial Interface & RGB 6-bit I/F</td><td>SDI</td><td>DB[5:0]</td></tr>
<tr><td>111</td><td></td><td></td><td>MDDI</td><td>-</td><td>-</td></tr>
</table>
Note1. “X“ denotes “Don’t care"
Note2. VFPF = COLMOD[6:4] (Refer to 3Ah Command)

Must be connected to VDD3 or VSS level when not used.</td></tr>
<tr><td>SDI</td><td>I</td><td>Serial data bus. If not used, connect this pad to either VDD3 or VSS.</td></tr>
<tr><td>SDO</td><td>O</td><td>Serial Output data.</td></tr>
</table>

Table 8. Signal pads for logic interface(continued)

Name	I/O	Description
TE	O	Tearing effect output pad to synchronize MCU to frame writing, activated by S/W command. When this pad is not activated, this signal stays low. If not used, leave this pad unconnected.
DOTCLK	I	Pixel clock signal in RGB I/F mode. If not used, connect this pad to either VDD3 or VSS.
VSYNC	I	Vertical Sync signal in RGB I/F mode. If not used, connect this pad to either VDD3 or VSS.
HSYNC	I	Horizontal Sync signal in RGB I/F mode. If not used, connect this pad to either VDD3 or VSS.
ENABLE	I	Data Enable signal in RGB I/F mode. If not used, connect this pad to either VDD3 or VSS.

Note. If CSX is connected to VSS in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there should be no influence to the Power Consumption of the display module.

When CSX='1', there is no influence to the parallel interface.

Table 9. Pads for source/gate driver output signal

Name	I/O	Description
S1 to S720	O	Signal pads for Source driver output.
G1 to G432	O	Signal pads for Gate driver output.

Table 10. MIE pins

Symbol	I/O	Description
BC	O	This pin is used to PWM output for back light control of LED driver. If not used, this pin should be opened.
BC_CTL	O	This pin is used to enable the back light LED driver (active high). If not used, this pin should be opened.

Table 11. Miscellaneous signal pads

Name	I/O	Description
CL1	O	Output pads used only for test purpose at IC-side. In normal operation, leave this pad unconnected.
CONTACT1 CONTACT2 CONTACT3 CONTACT4	-	Contact resistance measurement pad.In normal operation, leave this unconnected. These pads are floating. CONTACT1 and CONTACT2 are connected in IC. CONTACT3 and CONTACT4 are connected in IC. When measuring an ohmic resistance of the contact, do not apply any power.

Table 12. Test signal pads and dummy pads.

Name	I/O	Description
TMODE[2:0]	I	Input pads used only for test purpose at IC-side. During normal operation, connect this pad to VSS.
EN_EXCLK	I	Input pads used only for test purpose at IC-side. During normal operation, connect this pad to VSS.
EXCLK	I	Input pads used only for test purpose at IC-side. During normal operation, connect this pad to VSS.
TREGB	I	Input pads used only for test purpose at IC-side. During normal operation, connect this pad to VSS.
TMUX[2:0]	I	Input pads used only for test purpose at IC-side. During normal operation, connect this pad to VSS.
TEST_XA	I	Input pads used only for test purpose at IC-side. During normal operation, connect this pad to VSS.
TEST_YA[1:0]	I	Input pads used only for test purpose at IC-side. During normal operation, connect this pad to VSS.
TEST_Dummy	I	Input pads used only for test purpose at IC-side. During normal operation, connect this pad to VSS.
Dummy[1:16]		Input-side dummy pads. These pads have no potential.
Dummy[17:56]		Output-side dummy pads. These pads have no potential.

1.7. INTERFACE PAD CONFIGURATION

Table 13. Interface pad configuration1 (parallel mode)

PIN NAME	80 MCU					MDDI
	24bit	18bit	16bit	9bit	8bit	
IM[2]	VDD3	VSS	VSS	VSS	VSS	VDD3
IM[1]	VSS	VDD3	VDD3	VSS	VSS	VDD3
IM[0]	VSS	VDD3	VSS	VDD3	VSS	VDD3
MDP/MDN	Floating					MDP/MDN
MSP/MSN	Floating					MSP/MSN
DB [23:18]	DB [23:18]	VDD3/ VSS	VDD3/ VSS	VDD3/ VSS	VDD3/ VSS	VDD3/VSS
DB [17:16]	DB [17:16]	DB [17:16]	VDD3/ VSS	VDD3/ VSS	VDD3/ VSS	VDD3/VSS
DB [15:9]	DB [15:9]	DB [15:9]	DB [15:9]	VDD3/ VSS	VDD3/ VSS	VDD3/VSS
DB [8]	DB [8]	DB [8]	DB [8]	DB [8]	VDD3/ VSS	VDD3/VSS
DB [7:0]	DB [7:0]	DB [7:0]	DB [7:0]	DB [7:0]	DB [7:0]	VDD3/VSS
SDI	VDD3/VSS					VDD3/VSS
CSX	CSX					VDD3/VSS
WRX	WRX					VDD3/VSS
RDX	RDX					VDD3
DCX	DCX					VDD3/VSS
RESX	RESX					RESX
VSYNC	(VSYNC) Note1*					VDD3/VSS
HSYNC	VDD3/VSS					VDD3/VSS
ENABLE	VDD3/VSS					VDD3/VSS
DOTCLK	VDD3/VSS					VSS
TMODE[2:0]	VSS					VSS

Note1. In VSYNC Interface, VSYNC signal is valid. Other cases VSYNC have to tied to VDD3 or VSS.

Table 14. Interface pad configuration2 (serial mode)

PIN NAME	RGB(3wire)					RGB(4wire)				
	24bit	18bit	16bit	8bit	6bit	24bit	18bit	16bit	8bit	6bit
IM[2]	VDD3					VDD3				
IM[1]	VSS					VDD3				
IM[0]	VDD3					VSS				
DB [23:18]	DB [23:18]	VDD3/ VSS	VDD3/ VSS	VDD3/ VSS	VDD3/ VSS	DB [23:18]	VDD3/ VSS	VDD3/ VSS	VDD3/ VSS	VDD3/ VSS
DB [17:16]	DB [17:16]	DB [17:16]	VDD3/ VSS	VDD3/ VSS	VDD3/ VSS	DB [17:16]	DB [17:16]	VDD3/ VSS	VDD3/ VSS	VDD3/ VSS]
DB [15:8]	DB [15:8]	DB [15:8]	DB [15:8]	VDD3/ VSS	VDD3/ VSS	DB [15:8]	DB [15:8]	DB [15:8]	VDD3/ VSS	VDD3/ VSS
DB [7:6]	DB [7:6]	DB [7:6]	DB [7:6]	DB [7:6]	VDD3/ VSS	DB [7:6]	DB [7:6]	DB [7:6]	DB [7:6]	VDD3/ VSS
DB [5:0]	DB [5:0]	DB [5:0]	DB [5:0]	DB [5:0]	DB [5:0]	DB [5:0]	DB [5:0]	DB [5:0]	DB [5:0]	DB [5:0]
SDI	SDI									
CSX	CSX									
WRX	VDD3/VSS					SCL				
RDX	VDD3									
DCX	SCL					DCX				
RESX	RESX									
VSYNC	VSYNC									
HSYNC	HSYNC									
ENABLE	ENABLE									
DOTCLK	DOTCLK									
TMODE[2:0]	VSS									

CHAPTER 2

ELECTRICAL SPECIFICATION

2 ELECTRICAL SPECIFICATIONS

2.1. ABSOLUTE MAXIMUM RATINGS

Table 15. Absolute maximum ratings

Item	Symbol	Rating	Unit
Supply voltage for logic block	VDD - VSS	-0.3 to +3.3	V
Supply voltage for I/O block	VDD3 - VSS	-0.3 to +5.0	V
Supply voltage for step-up circuit	VCI - VSS	-0.3 to +5.0	V
LCD Supply Voltage range	AVDD – VSS	-0.3 to +6.5	V
	VGH - VSS	-0.3 to +22.0	V
	VSS – VGL	-0.3 to +22.0	V
	VSS - VCL	-0.3 to +5.0	V
	|VGH – VGL|	-0.3 to +33	V
Input Voltage range	Vin	- 0.3 to VDD3 + 0.5	V
Operating temperature	Topr	-40 to +85	°C
Storage temperature	Tstg	-55 to +110	°C

Note1. The absolute maximum rating is the limit value. When the IC is exposed to the operating environment beyond this range, the IC does not assure normal operations and may be damaged permanently, not be able to be recovered.

Note2. The operating temperature is the range of device-operating temperature. They do not guarantee chip performance.

Caution

Stresses above these absolute maximum ratings may cause permanent damage. These are stress atings only and functional operation at these conditions is not implied. Exposure to maximum rating conditions for extended periods may reduce device reliability.

2.2. DC ELECTRICAL CHARACTERISTICS

2.2.1. Basic Characteristics

Table 16. DC electrical characteristics (Ta = 25℃).

Characteristic	Symbol	Condition	MIN	TYP	MAX	Unit	Note
Power supply for I/O	VDD3		1.65	-	3.3	V	*1
Power supply	VCI		2.3	-	3.3	V	
LCD driving voltage	VGH		11.25	-	16.50	V	*8
	VGL		-13.75	-	-6.75	V	
	VCL		-3.0	-	-2.25	V	
	AVDD		4.5	-	6.0	V	
	GVDD		2.5	-	5.0	V	
	VGH-VGL				30.0	V	
	VCI-VCL				6.0	V	
Logic power supply	VDD	Ta= 25°C	1.4	1.5	1.6	V	*7
Reference Voltage	VREF	Ta= 25°C	1.9	2.0	2.1	V	*7
Logic Input voltage, high	V_{IH}		0.7*VDD3	-	VDD3	V	*2
Logic Input voltage, low	V_{IL}		0	-	0.3*VDD3	V	*2
Logic output voltage, high	V_{OH}	I_{OH}= -0.5mA	0.8*VDD3	-	VDD3	V	*3
Logic output voltage, low	V_{OL}	I_{OL} = 0.5mA	0.0	-	0.2*VDD3	V	*3
Leakage current, input	I_{IL}	VIN = VSS3 or DD3	-1.0		1.0	uA	*2
Leakage current, output	I_{OL}	VIN = VSS3 or DD3	-3.0		3.0	uA	*3
Operating frequency	Fosc	Frame freq. = 64.1 Hz Display line = 432 Ta = 25°C	13.2	13.9	14.6	MHz	*4
Input voltage to the 1st Booster	VCI1		1.35	-	3.0	V	*5
Power efficiency of the 1st Booster	η_{AVDD}	Load current = 4mA	90	95	-	%	
Power efficiency of the 2nd Booster	η_{VGH}	Load current = 100uA	90	95	-	%	
Power efficiency of the 3rd Booster	η_{VGL}	Load current = 100uA	90	95	-	%	
Power efficiency of the 4th Booster	η_{VCL}	Load current = 300uA	90	95	-	%	
Current consumption during normal operation	IVDD3	No load, Ta= 25 °C, VC I = 3V,Frame(f) = 63Hz	-	-	1300	uA	*6
	IVCI		-	-	11.5	mA	-

Characteristic	Symbol	Condition	MIN	TYP	MAX	Unit	Note
Current consumption during Sleep-In mode	$IVDD3_{SI}$	Supplied : VDD3, VCI, VSS3, Ta = 25 °C	-	-	25	uA	-
	IVCISI		-	-	5	uA	
Current consumption during Deep-standby mode	$IVDD3_{SI}$	Supplied : VDD3, VCI, VSS3, Ta = 25 °C	-	-	5	uA	-
	$IVCI_{SI}$		-	-	5	uA	
Reference voltage for generating GVDD voltage.	VREF		-	2.0	-	V	
Reference voltage input for g rayscale voltage	GVDD		2.5		5.0	V	
High level output voltage of VCOM.	VCOMH		2.5		5.0	V	
Low level output voltage of VCOM.	VCOML		VCL + 0.5		0	V	
Power supply for display common electrode.	VCOM		-	-	6.0	V	

Note1. VSS3 = 0V.

Note2. Signals under consideration; CSX, RDX, WRX, DB0 to DB23, and RESX

Note3. Signals under consideration; DB0 to DB23

Note4. Target frame frequency = 64.1 Hz, Display line = 432, Back porch = 8, Front porch = 8, RTN4-0 = “10110”, CRTN4-0 = “10110” (Fosc can be observed indirectly by measuring CL1 pad (Fosc / (22x22))

Note5. Practical VCI1 range is over 2.25V. VCI1 under 2.25V is used only for power-up period.

Note6. CPU access is inactive.

Note7. VDD and VREF are internally generated voltage outputs. Do not apply external power supply at these pins in normal operation.

Note8. VGH should be lower than 16.5V except MTP programming session. In case of MTP programming, VGH can be set over 16.5V for a short period such as 100 ~ 200msec.

Table 17. DC characteristics for LCD driver outputs (TYP: VCI=VDD3=3.0V, Ta=25°C)

Characteristic	Symbol	Condition	MIN	TYP	MAX	Unit	Note
On resistance of Gate driver output	R_{onvgh}	VGH = 6.3V VGL = -6.3V	-	-	7.0	kΩ	-
	R_{onvgl}		-	-	7.0	kΩ	-
On resistance of source driver output	R_{onp}	AVDD = 4.5V AVSS = 0V	-	-	30	kΩ	-
	R_{onn}		-	-	30	kΩ	-
On resistance of binary driver Output	R_{onpb}	GVDD = 4.5V AVSS = 0V	-	-	300	kΩ	-
	R_{onnb}		-	-	300	kΩ	-
Output voltage deviation (Mean value) AVDD=5.0V, GVDD=4.5V	ΔV_O	AVDD – 0.8V ≤ V_{SO}	-	-	±55	mV	*1
		0.8V < V_{SO} < AVDD-0.8V	-	-	±25	mV	*1
		V_{SO} ≤ 0.8V	-	-	±55	mV	*1
Delay, source driver	t_{SD}	AVDD = 5.5V GVDD = 5V SAP = '0011'	-	-	25.8	us	*2

Note1. VSO is the output voltage of analog output pads; S1 through S720

Note2. tSD : LCD Source driver delay.

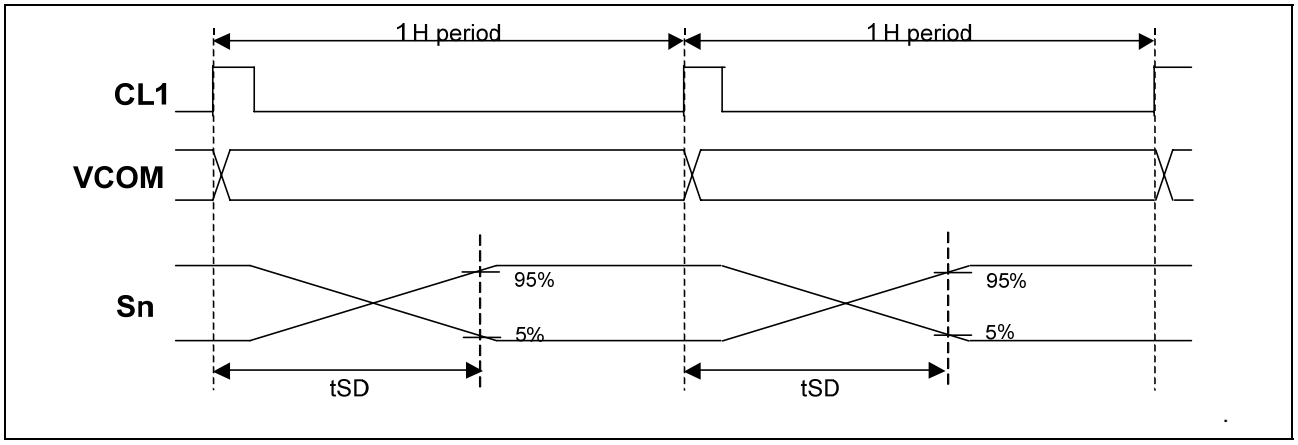


Figure 8. LCD source driver delay

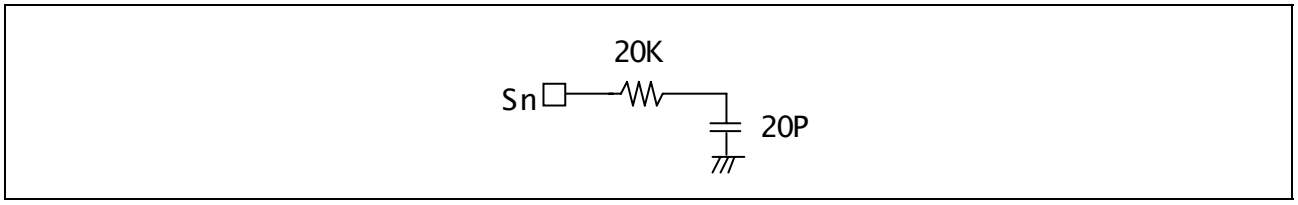


Figure 9. Load condition (source driver)

2.3. AC CHARACTERISTEICS

2.3.1. Parallel Interface Characteristics (80-series MCU)

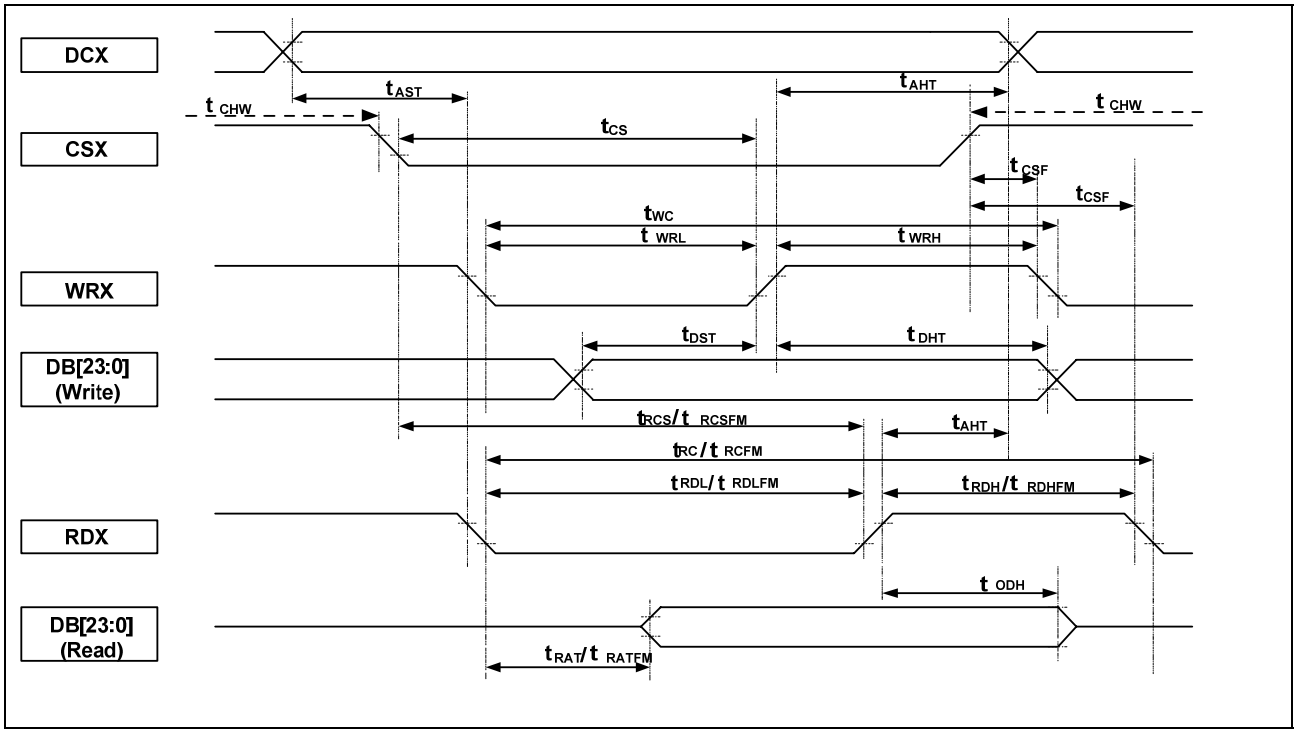


Figure 10. MCU 80 interface AC characteristics

Table 18. MCU 80 interface AC characteristics

Signal	Symbol		Parameter	MIN	MAX	Unit	Description
DCX	tAST		Address setup time	0	-	ns	
	tAHT		Address hold time (Write/Read)	10	-	ns	
CSX	tCHW		Chip select “H” pulse width	0	-	ns	
	tCS		Chip select setup time (Write)	25	-	ns	
	tRCS		Chip select setup time (Read ID)	45	-	ns	
	tRCSFM		Chip select setup time (Read FM)	355	-	ns	
	tCSF		Chip select wait time (Write/Read)	10	-	ns	
WRX	CASE 1	tWC	Write cycle	84	-	ns	Refer to note 6
		tWRH	Control pulse “H” duration	25	-	ns	
		tWRL	Control pulse “L” duration	25	-	ns	
	CASE 2	tWC	Write cycle	60	-	ns	
		tWRH	Control pulse “H” duration	20	-	ns	
		tWRL	Control pulse “L” duration	20	-	ns	
	CASE 3	tWC	Write cycle	60	-	ns	
		tWRH	Control pulse “H” duration	20	-	ns	
		tWRL	Control pulse “L” duration	20	-	ns	
RDX(ID)	tRC		Read cycle (ID)	160	-	ns	When read ID data
	tRDH		Control pulse “H” duration (ID)	90	-	ns	
	tRDL		Control pulse “L” duration (ID)	45	-	ns	
RDX(FM)	tRCFM		Read cycle (FM)	450	-	ns	When read from the frame memory
	tRDHFM		Control pulse “H” duration (FM)	90	-	ns	
	tRDLFM		Control pulse “L” duration (FM)	355	-	ns	
DB[23:0]	tDST		Data setup time	15	-	ns	For the maximum CL = 30pF, For the minimum CL = 8pF
	tDHT		Data hold time	15	-	ns	
	tRAT		Read access time (ID)	-	40	ns	
	tRATFM		Read access time (FM)	-	340	ns	
	tODH		Output disable time	20	80	ns	

Note1. The rise and fall times of input signals (tr & tf) are less than 15 ns.

Note2. tRAT and tODH timings are based on 20% to 80 % of VDD3-GND.

Note3. Other timings are based on 30% to 70% of VDD3-GND.

Note4. tWRL and tRDL are related with an interval in which CSX=”L” and WRX, RDX=”L” overlap.

Note5. DCX timing is related with an interval in which CSX=”L” and WRX, RDX=”L” overlap.

Note6.

Case 1 : 1 pixel data / 1 WRX clock mode or 2 pixel data / 3 WRX clock mode

The others of Case 2 & Case 3

Case 2 : 1 pixel data / 2 WRX clock mode

IM[2:0]=000, COLMOD[2:0]=101, MDT[1:0]=00

IM[2:0]=001, COLMOD[2:0]=101, MDT[1:0]=00

IM[2:0]=001, COLMOD[2:0]=110, MDT[1:0]=00

IM[2:0]=010, COLMOD[2:0]=110, MDT[1:0]=01, 10, 11

IM[2:0]=010, COLMOD[2:0]=111, MDT[1:0]=01

IM[2:0]=011, COLMOD[2:0]=111, MDT[1:0]=01

Case 3 : 1 pixel data / 3 WRX clock mode

IM[2:0]=000, COLMOD[2:0]=110, MDT[1:0]=00

IM[2:0]=000, COLMOD[2:0]=111, MDT[1:0]=00

IM[2:0]=001, COLMOD[2:0]=110, MDT[1:0]=01

IM[2:0]=001, COLMOD[2:0]=111, MDT[1:0]=00

2.3.2. Serial Interface Characteristics (3-wire/ 9-bit Serial Interface)

SDO is fixed "L" during non-operation.

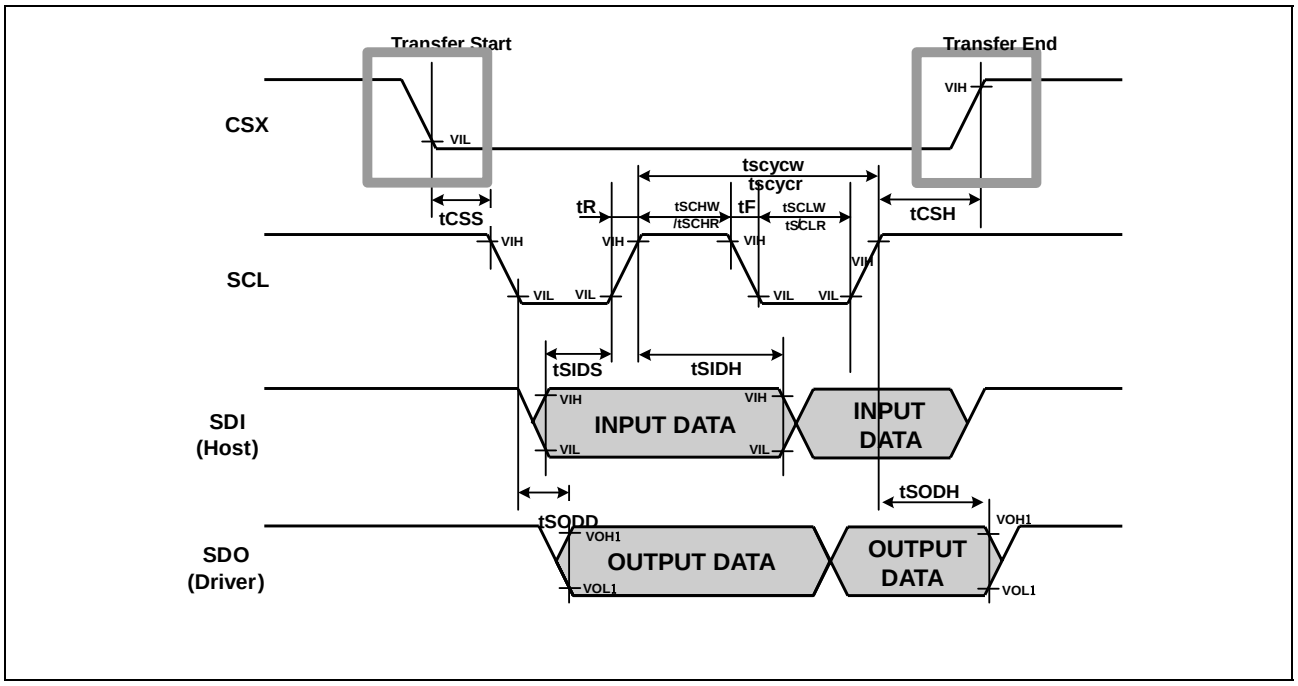


Figure 11. 3- wire 9bit Serial interface characteristics

Table 19. Serial interface AC characteristics(3-wire 9bit)

Characteristic	Symbol	specification		Unit
		Min.	Max.	
Serial clock write cycle time	tscycw	100		ns
Serial clock read cycle time	tscycr	150		ns
Serial clock rise / fall time	tR, tF		15	ns
Pulse width high for write	tSCHW	35		ns
Pulse width high for read	tSCHR	60		ns
Pulse width low for write	tSCLW	35		ns
Pulse width low for read	tSCLR	60		ns
Chip Select setup time	tCSS	30		ns
Chip Select hold time	tCSH	30		ns
Serial input data setup time	tSIDS	30		ns
Serial input data hold time	tSIDH	30		ns
Serial output data delay time	tSODD	20	50	ns
Serial output data hold time	tSODH	15	50	ns

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

2.3.3. Serial Interface Characteristics (4-wire/ 8-bit Serial Interface)

SDO is fixed "L" during non-operation.

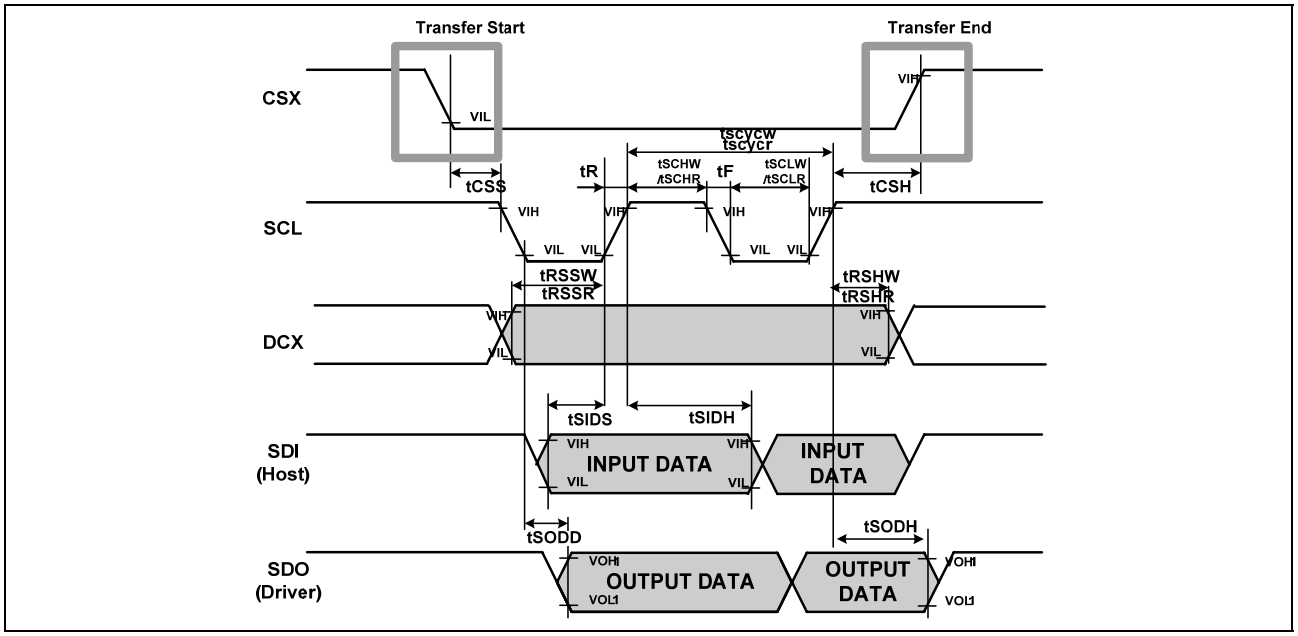


Figure 12. 4 wire 8bit Serial interface characteristics

Table 20. Serial interface AC characteristics(4-wire 8bit)

Characteristic	Symbol	specification		Unit
		Min.	Max.	
Serial clock write cycle time	tscycw	100		ns
Serial clock read cycle time	tscycr	150		ns
Serial clock rise / fall time	tR, tF		15	ns
Pulse width high for write	tSCHW	35		ns
Pulse width high for read	tSCHR	60		ns
Pulse width low for write	tSCLW	35		ns
Pulse width low for read	tSCLR	60		ns
Chip Select setup time	tCSS	30		ns
Chip Select hold time	tCSH	30		ns
RS Setup time for write	tRSSW	30		ns
RS Setup time for read	tRSSR	60		ns
RS hold time for write	tRSHW	30		ns
RS hold time for read	tRSHR	60		ns
Serial input data setup time	tSIDS	30		ns
Serial input data hold time	tSIDH	30		ns
Serial output data delay time	tSODD	20	50	ns
Serial output data hold time	tSODH	15	50	ns

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

2.3.4. RGB Interface Characteristics

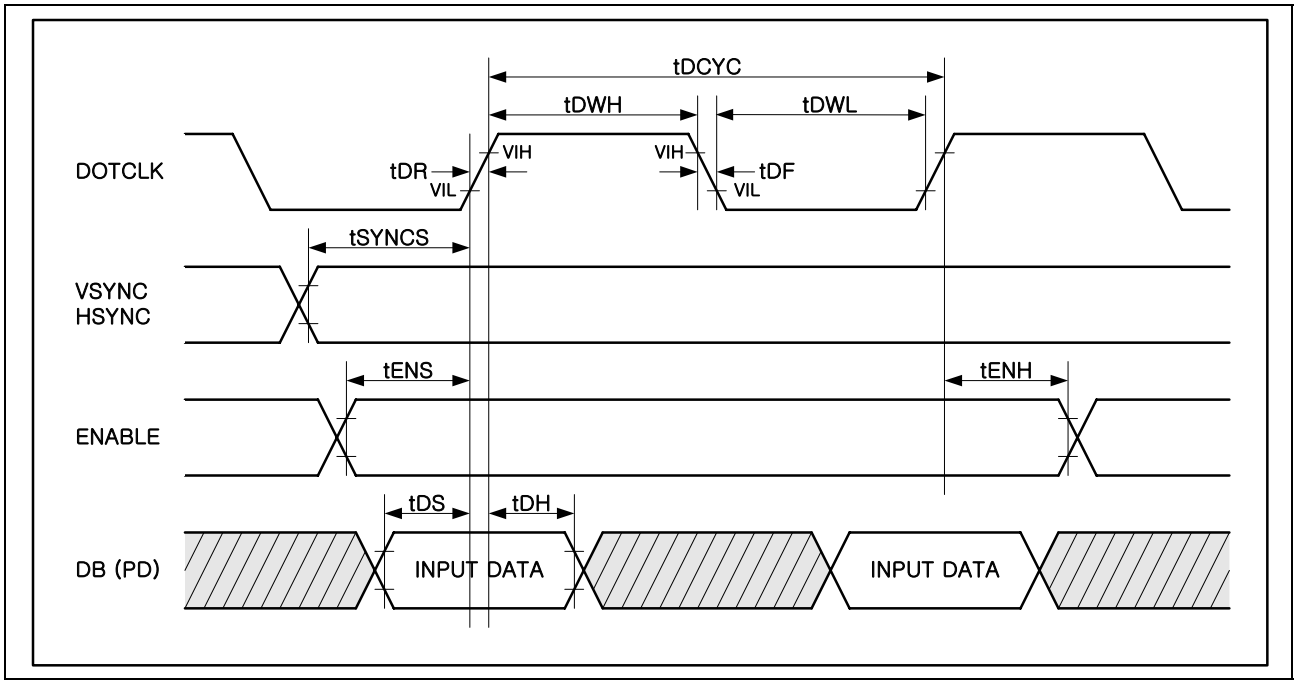


Figure 13. RGB interface characteristics

Table 21. RGB interface AC characteristics

Parameter	Description	24/18/16 bit		8/6 bit		Unit
		Min	Max	Min	Max	
tDCYC	DOTCLK period	100		60		ns
tDWL	DOTCLK pulse width low	45		25		ns
tDWH	DOTCLK pulse width high	45		25		ns
tDR / tDF	DOTCLK rising / falling time		10		10	ns
tSYNCS	VSYNC, HSYNC setup	30		25		ns
tENS	ENABLE setup	50		25		ns
tENH	ENABLE hold	50		25		ns
tDS	Input Data setup	40		20		ns
tDH	Input Data hold	40		20		ns

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

Note1. VSYNC Low Pulse Width ≥1H

Note2. HSYNC Low Pulse Width ≥ 1 DOTCLK (24/18/16 bit I/F)

Note3. HSYNC Low Pulse Width ≥ 3 DOTCLK (8/6 bit I/F)

2.3.5. RESX Signal

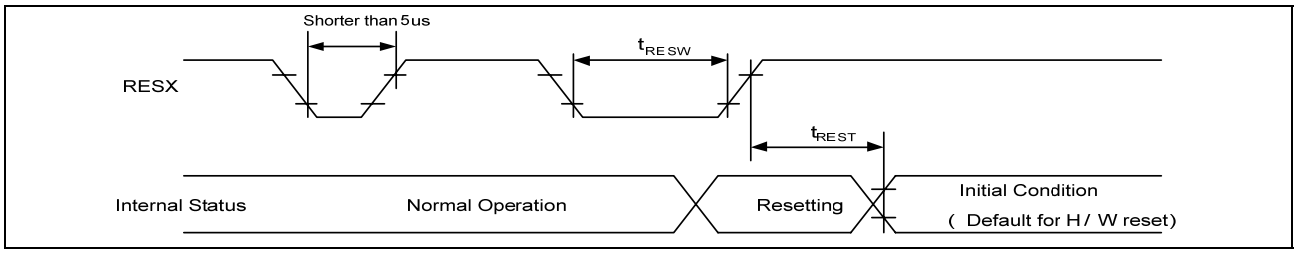


Figure 14. Reset input timing

Table 22. Reset input timing

Symbol	Parameter	Pad	Min	Typ	Max	Unit	Note
tRESW	1) Reset low pulse width	RESX	10	-	-	µs	-
tREST	2) Reset completion time	RESX	-	-	5	ms	Reset during Sleep In mode
		RESX		-	120	ms	Reset during Sleep Out mode

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

Note1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

Table 23. RESX pulse

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset Start

Note2. During the reset period, the display will be blanked (The display is entering blanking sequence, for which the maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains in the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

Note3. During Reset Completion Time, ID1, ID2, ID3 and VCM, VML, GVD Offset value in MTP will be latched to the internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note4. Spike Rejection also applies during a valid reset pulse as shown below:

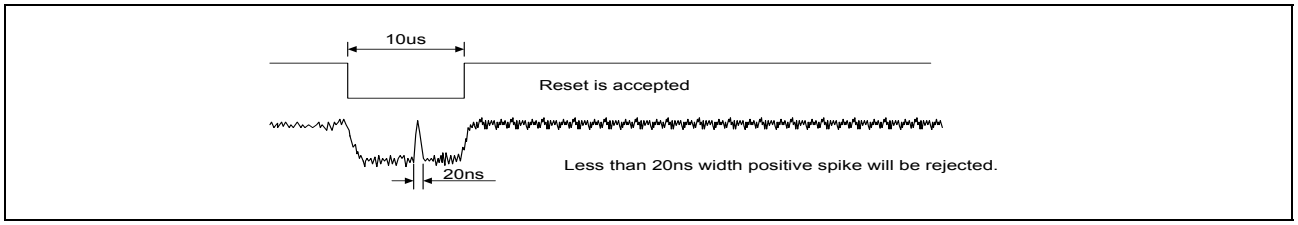


Figure 15. RESX pulse

Note5. It is necessary to wait for 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

2.3.6. Measurement Conditions

The measurement conditions shown in this section is provided for a reference purpose to the module makers. The condition for the actual IC measurement will be determined after the consideration of a practical manufacturing environment of mass production.

2.3.6.1. tRATFM, tODH Measurement Condition

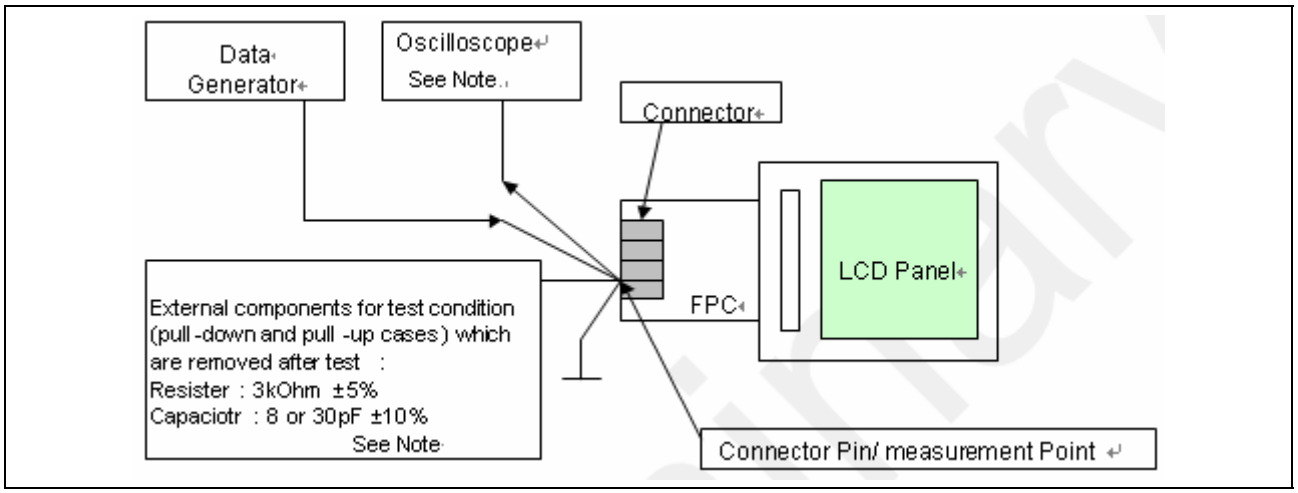


Figure 16. Measurement condition set-up of MCU interface at a module level

Note. Capacitances and resistances of the oscilloscope probe must be included an external components in these measurements

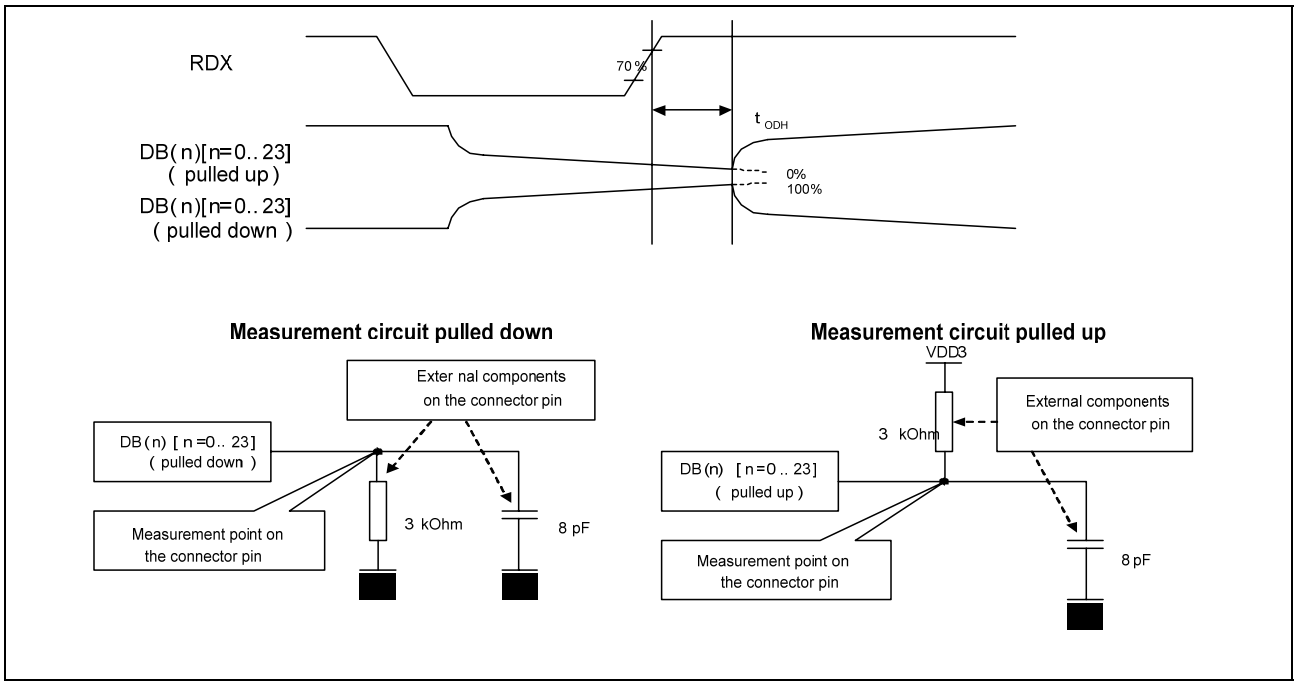


Figure 17. Minimum value measurement of MCU interface

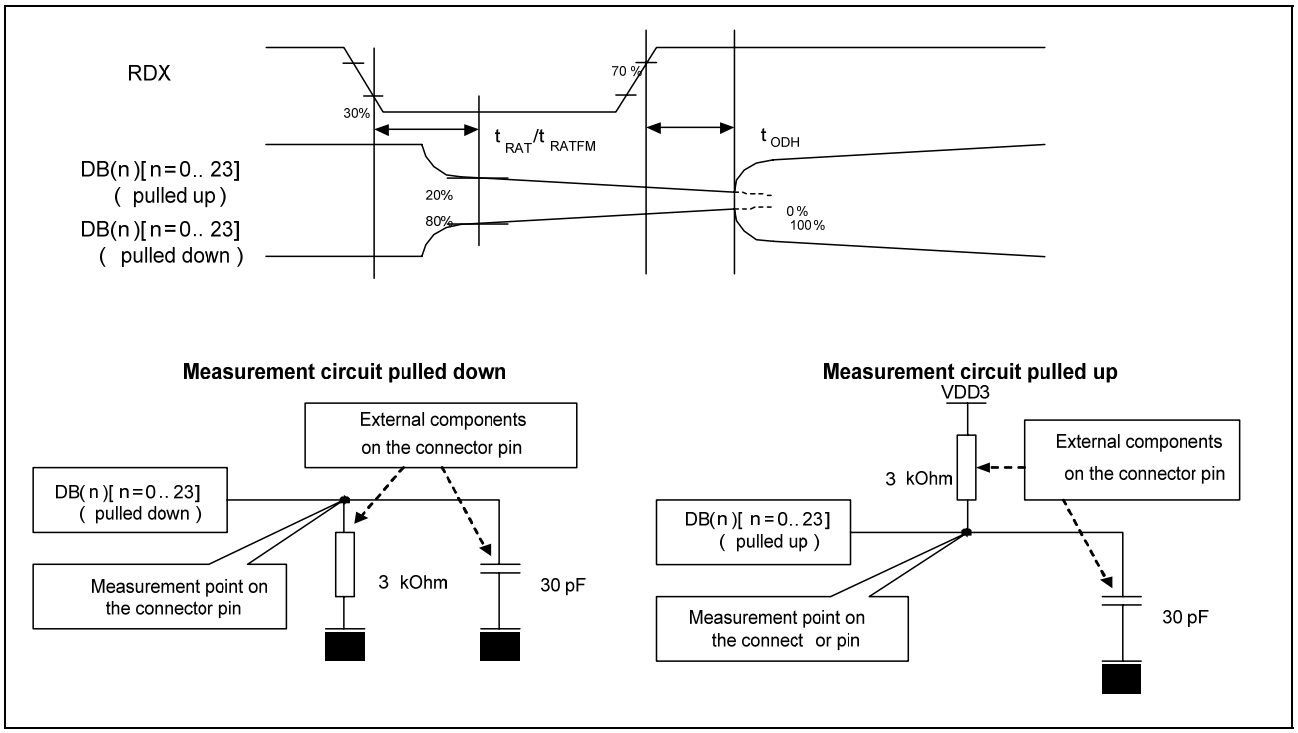


Figure 18. Maximum value measurement of MCU interface

2.3.6.2. tSODD, tSODH Measurement Condition

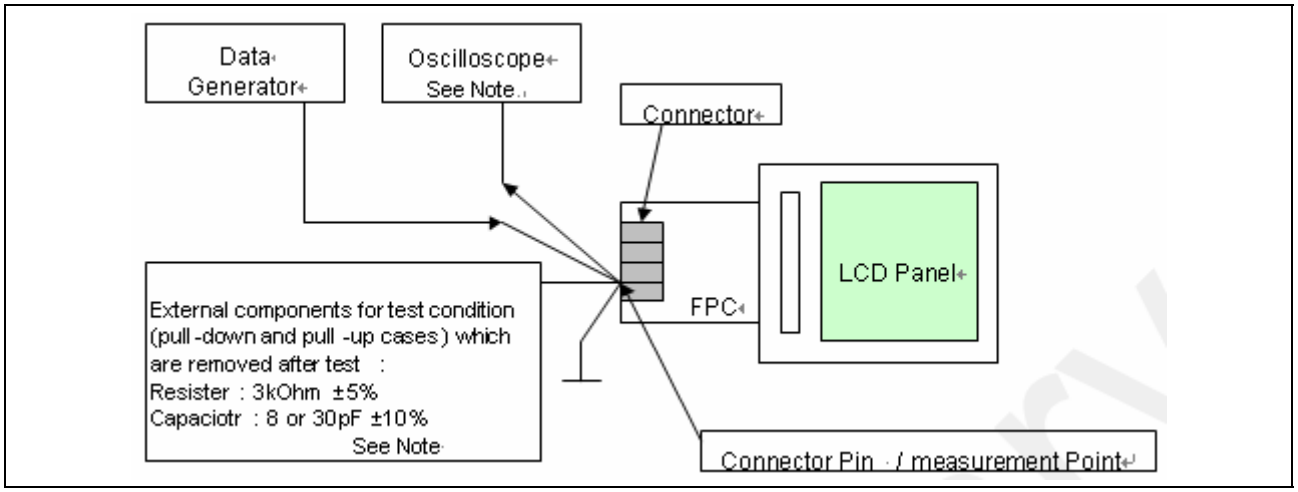


Figure 19. Measurement condition set-up of SPI at a module level

Note. Capacitances and resistances of the oscilloscope probe must be included an external components in these measurements

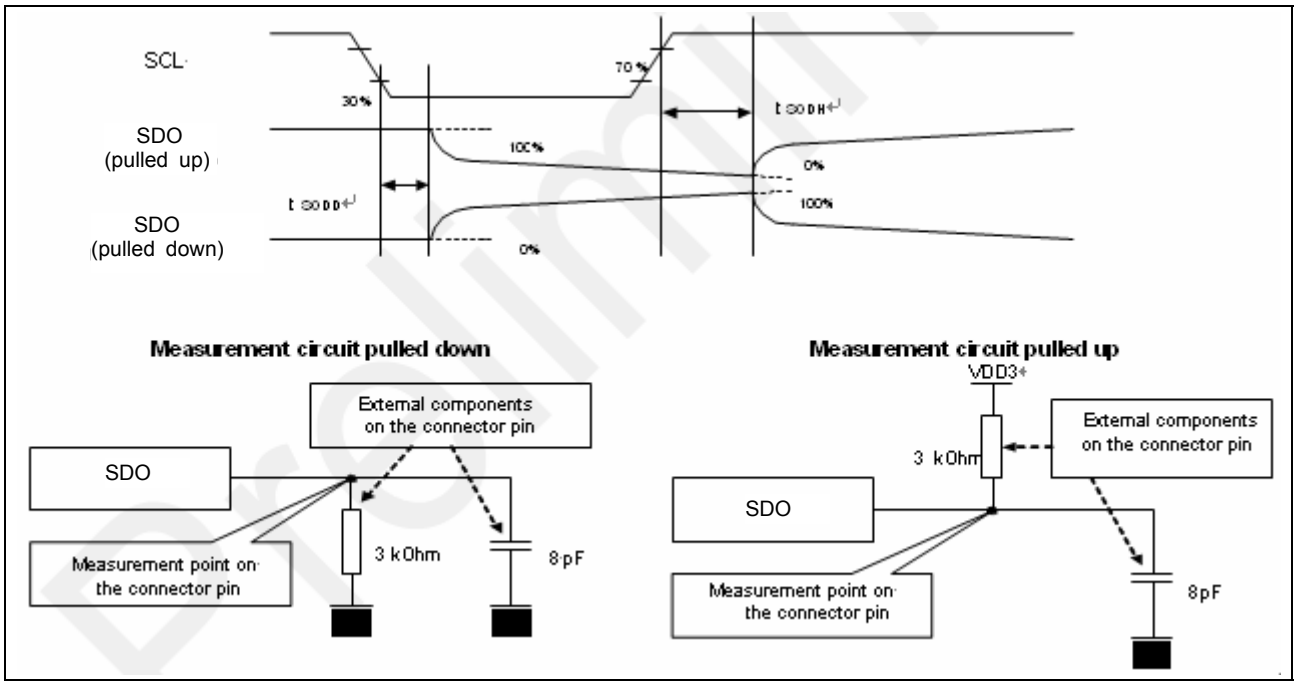


Figure 20. Minimum value measurement of SPI

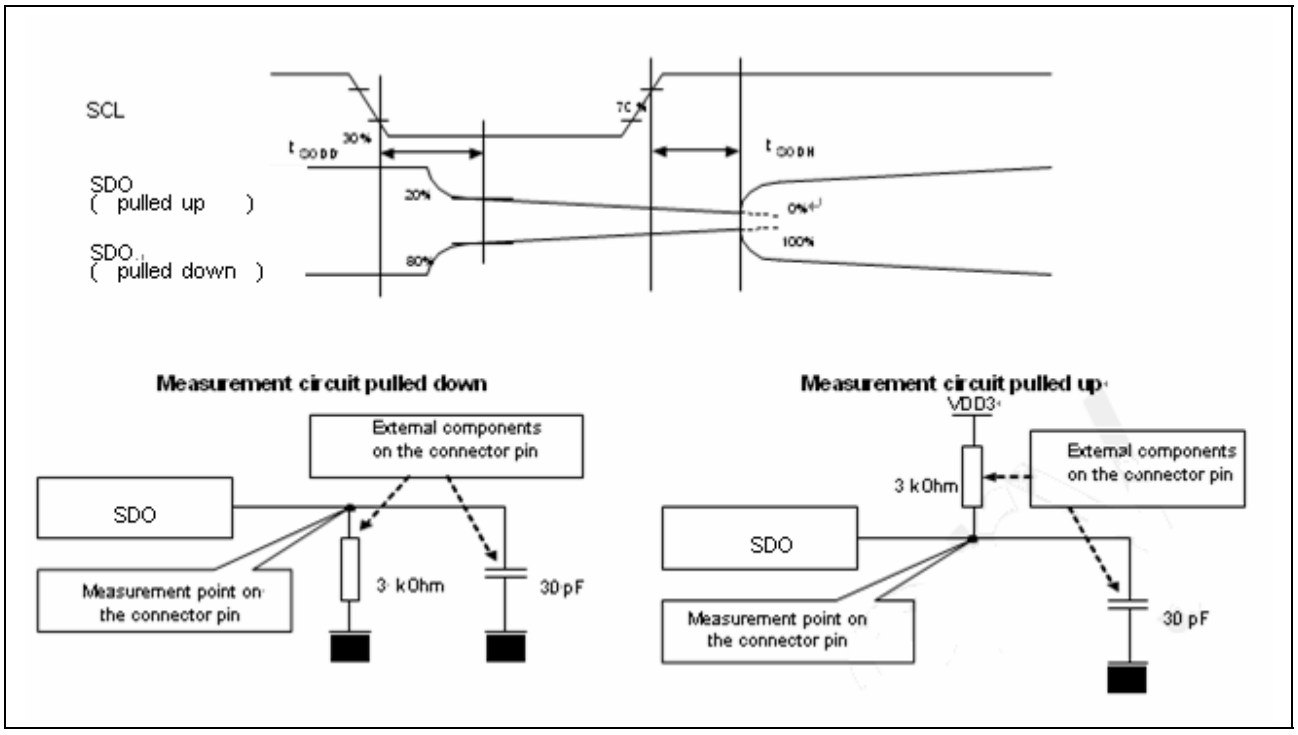


Figure 21. Maximum value measurement of SPI

2.4. MDDI DC/AC CHARACTERISTICS

Table 24. Data/strobe Rx DC characteristics

Parameter	Description	MIN	TYP	MAX	Unit	Note
V_{IT+}	Reciver differential input high threshold voltage. Abobe this differential voltage the input signal shall be interpreted as a logic-one level.			50	mV	
V_{IT-}	Reciver differential input low threshold voltage. Below this differential voltage the input signal shall be interpreted as logic-zero level.	-50			mV	
V_{IT+}	Reciver differential input high threshold voltage (offset for hibernation wake-up). Abobe this defferential voltage the input signal shall be interpreted as a logic-one level.		125	175	mV	
V_{IT-}	Reciver differential input low threshold voltage (offset for hibernation wake-up). Below this defferential voltage the input signal shall be interpreted as a logic-one level.	75	125		mV	
$V_{input-Range}$	Allowable reciver input voltage range with respect to client ground.	0		1.65	mV	
R_{term}	Parallel termination resistance value.	98	100	102	Ω	

Table 25. Driver electrical DC characterisitics

Parameter	Description	MIN	TYP	MAX	Unit	Note
$I_{diffabs}$	Absolute driver differential output current range (Current through the termination resistor).	2.5		4.5	mA	Rterm= 100 Ω
$V_{out-rng-int}$	Signal-ended driver output voltage range with respect to ground, internal mode.	0.35		1.60	V	Under all conditions, including double-drive

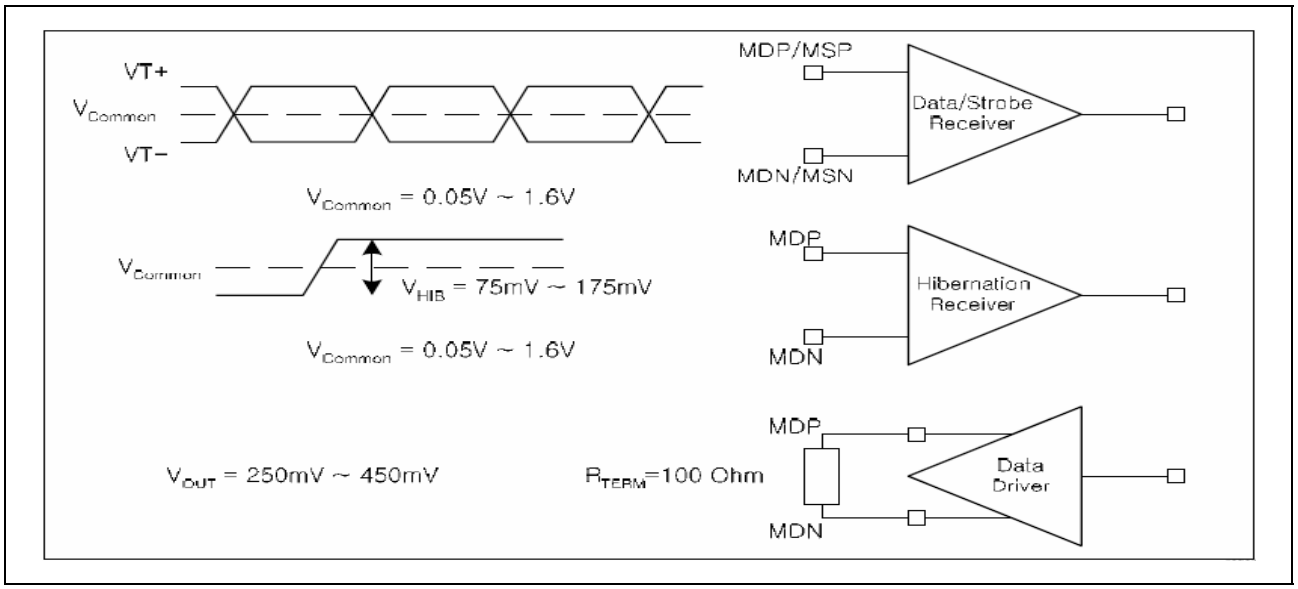


Figure 22. MDDI reciver, driver electrcal diagram

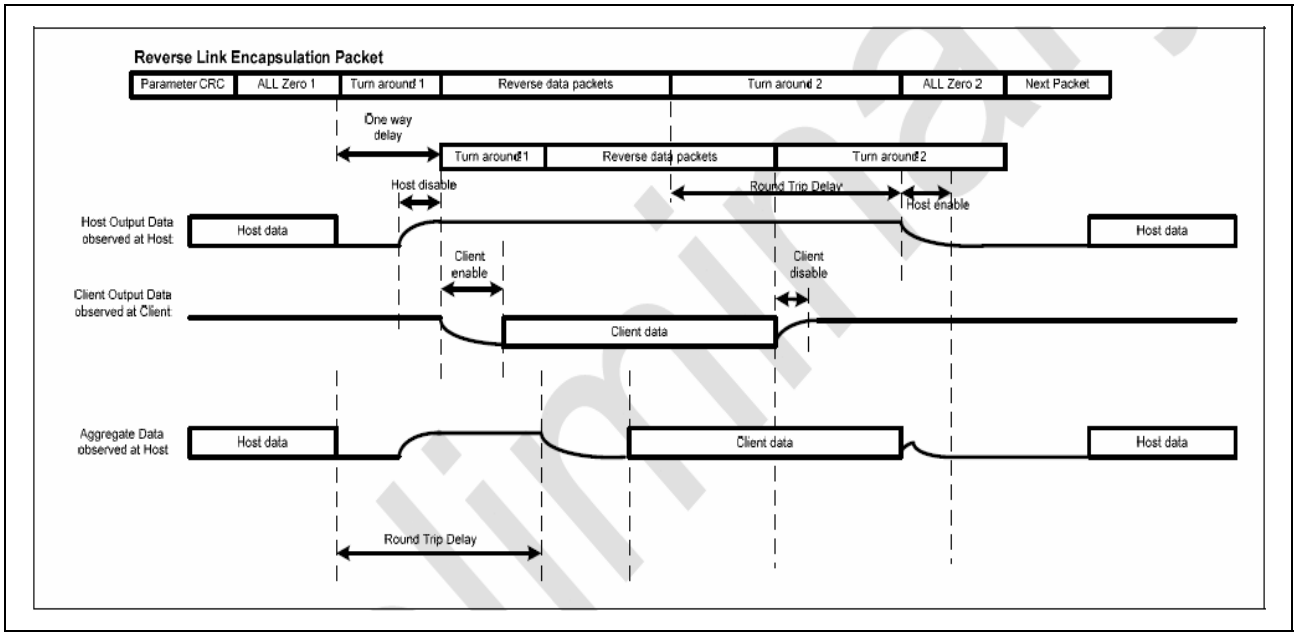


Figure 23. Host enable/disable time and client enable/disable time diagram

Table 26. Reciver AC characteristics

Parameter	Description	MIN	TYP	MAX	Unit
T_{host_enable}	Host output enable time.	6.6		$24*t_{BIT}$	ns
$T_{host\_disable}$	Host output disable time, entire length of the Turn-Around 1 field.	0		$24*t_{BIT}$	ns
T_{client_enable}	Client output enable time, entire length of the Turn-Around 1 field.	0		$24*t_{BIT}$	ns
$T_{client\_disable}$	Client output disable time, measured from the end of the last bit of the Turn-Around 2 field.	0		$24*t_{BIT}$	ns

Note. tBIT=1/Link_Data_Rate, where Link_Data_Rate is the bit rate of a signal data pair.(For example, if the average forward link bit rate is 150Mbps, then tBIT=1/150Mbps=6.6ns)

These specifications are from VESA specification Ver1.0.

CHAPTER 3

INTERFACE

3 INTERFACE

3.1. MPU INTERFACE

3.1.1. Interface Type Selection

While the driver IC is used to parallel interface, it transfers commands, parameters and display data between the driver IC and MPU using a bi-directional data line up to 24 bits of bus width. The interface which communicates with MPU is selected by using a combination of IM [2:0] pins.

Table 27. Interface type selection

Mode	IM2	IM1	IM0
80 MCU 24-bit Parallel I/F	1	0	0
80 MCU 18-bit Parallel I/F	0	1	1
80 MCU 16-bit Parallel I/F	0	1	0
80 MCU 9-bit Parallel I/F	0	0	1
80 MCU 8-bit Parallel I/F	0	0	0
3-wire 9bit Data Serial I/F	1	0	1
4-wire 8bit Data Serial I/F	1	1	0

3.1.2. Pad Description of MPU Interface

MPU interface of the S6D04D1 is changed according to the bus width used. The pin assignments are listed in the table below. The unused input pads have to connect to VSS or VDD3.

When CSX is inactive as high, DB23 to DB0 are placed in the high-impedance state internally.

3.1.2.1. 80-Series MCU Parallel Interface

Table 28. Interface signal description in case of MCU I/F

<table>
<tr><th>Pad signal</th><th>Description</th></tr>
<tr><td>CSX</td><td>Chip select control signal</td></tr>
<tr><td>DCX</td><td>Data bus transfers a command when DCX is low.
Data bus transfers parameters or display data when DCX is high.</td></tr>
<tr><td>RDX</td><td>Read control signal
When RDX is low, the data bus is held on output state.</td></tr>
<tr><td>WRX</td><td>Write control signal
Data is latched on the rising edge of WRX.</td></tr>
<tr><td>DB23 to DB0</td><td>Data bus
<table>
<tr><th>Mode</th><th>DB pads</th></tr>
<tr><td>80 MCU 24-bit Parallel I/F</td><td>DB23-DB0 : 24-bit data</td></tr>
<tr><td>80 MCU 18-bit Parallel I/F</td><td>DB23-DB18 : unused / DB17-DB0 : 18-bit data</td></tr>
<tr><td>80 MCU 16-bit Parallel I/F</td><td>DB23-DB16 : unused / DB15-DB0 : 16-bit data</td></tr>
<tr><td>80 MCU 9-bit Parallel I/F</td><td>DB23-DB9 : unused / DB8-DB0 : 9-bit data</td></tr>
<tr><td>80 MCU 8-bit Parallel I/F</td><td>DB23-DB8: unused / DB7-DB0 : 8-bit data</td></tr>
</table>
If not used, connect these pads to VDD3 or VSS.</td></tr>
</table>

3.1.2.2. 4-wire/8-bit Serial Interface

Table 29. Interface signals in case of 4-wire/8-bit serial interface.

Pad signal	Description
CSX	Chip select signal
DCX	Data bus is regarded as a command when DCX is low. Data bus is regarded as a parameter when DCX is high.
SCL (WRX)	Clock signal During write mode, the data is latched on the rising edge of SCL signal.
SDI	Serial Data signal.
SDO	Serial Output signal

3.1.2.3. 3-wire/9-bit Serial Interface

Table 30. Interface signals in case of 3-wire/9-bit serial interface.

Pad signal	Description
CSX	Chip select signal
SCL (DCX)	Clock signal During write mode, the data is latched on the rising edge of SCL signal.
SDI	Serial Data signal.
SDO	Serial Output signal

3.1.3. Sequence of MPU Interface

In 80 MCU 24-bit parallel interfaces, the chip-select CSX (active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write signal, RDX is the parallel data read signal and DB[23:0] is parallel data. The MCU reads the data at the rising edge of RDX signal. The DCX is the data/command flag. When DCX='1', DB[23:0] bits are display RAM data or command parameters. When DCX='0', DB[7:0] bits are commands. The 80-Series bi-directional interface can be used for communication between the micro controller and LCD driver chip. Interface bus width can be selected with IM[2:0].

Table 31. The function of 80-series parallel interface

DCX	RDX	WRX	Function
L	1	↑	Write 8-bit command
H	1	↑	Write 8-bit parameter or [80 MCU 24-bit Parallel I/F] Write 24-bit display data (DB23 to DB0) [80 MCU 18-bit Parallel I/F] Write 18-bit display data (DB17 to DB0) [80 MCU 16-bit Parallel I/F] Write 16-bit display data (DB15 to DB0) [80 MCU 9-bit Parallel I/F] Write 9-bit display data (DB8 to DB0) [80 MCU 8-bit Parallel I/F] Write 8-bit display data (DB7 to DB0)
H	↓	1	Read 8-bit parameter or Read dummy data (1st output data after read command) or [80 MCU 24-bit Parallel I/F] Read 24-bit display data (DB23 to DB0) [80 MCU 18-bit Parallel I/F] Read 18-bit display data (DB17 to DB0) [80 MCU 16-bit Parallel I/F] Read 16-bit display data (DB15 to DB0) [80 MCU 9-bit Parallel I/F] Read 9-bit display data (DB8 to DB0) [80 MCU 8-bit Parallel I/F] Read 8-bit display data (DB7 to DB0)

Note. ↑ = rising edge

Note. ↓ = falling edge

3.1.3.1. Write Sequence of MPU Interface

The write cycle means that the host writes information (command or/and data) to the driver IC via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (DCX, RDX, and WRX) and data signals (DB[23:0]). DCX bit is a control signal, which represents the data is a command or a data. The data signals represent command if the control signal is low (='0') and represent data if the control signal is high ('1').

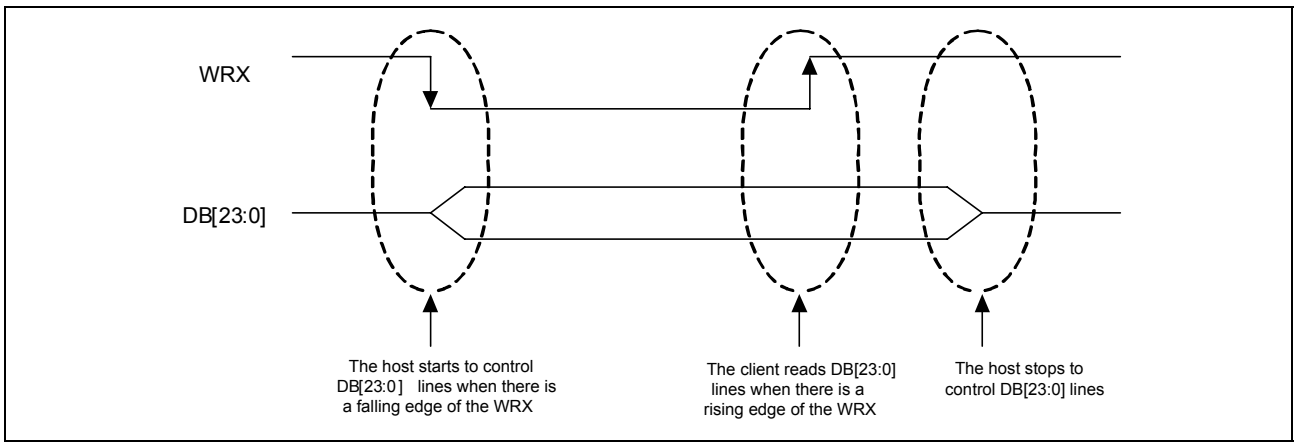


Figure 24. 80-Series WRX protocol

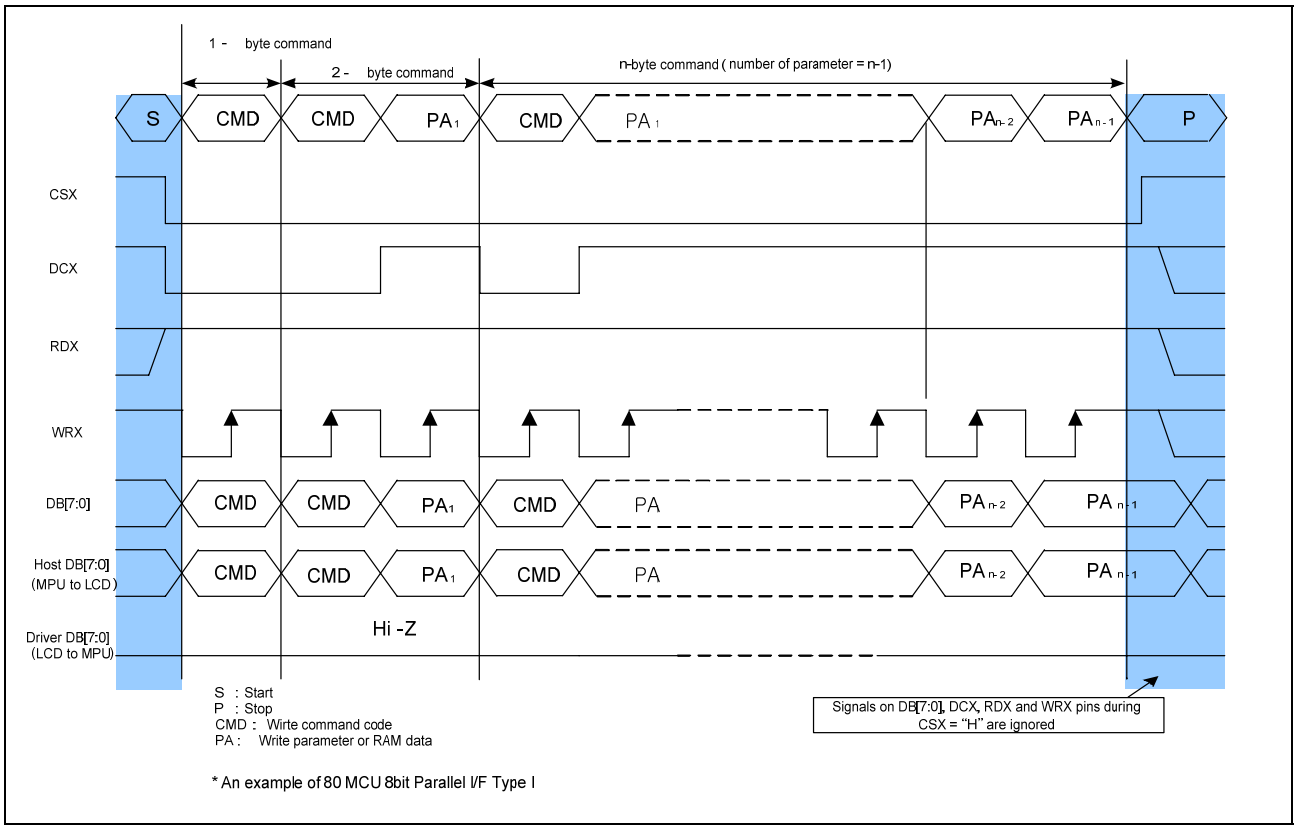


Figure 25. 80-Series parallel bus protocol, write to register or display RAM

3.1.3.2. Read Sequence of MPU Interface

The read cycle (RDX high-low-high sequence) means that the host reads information from driver IC via the interface. The IC sends data (DB[23:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

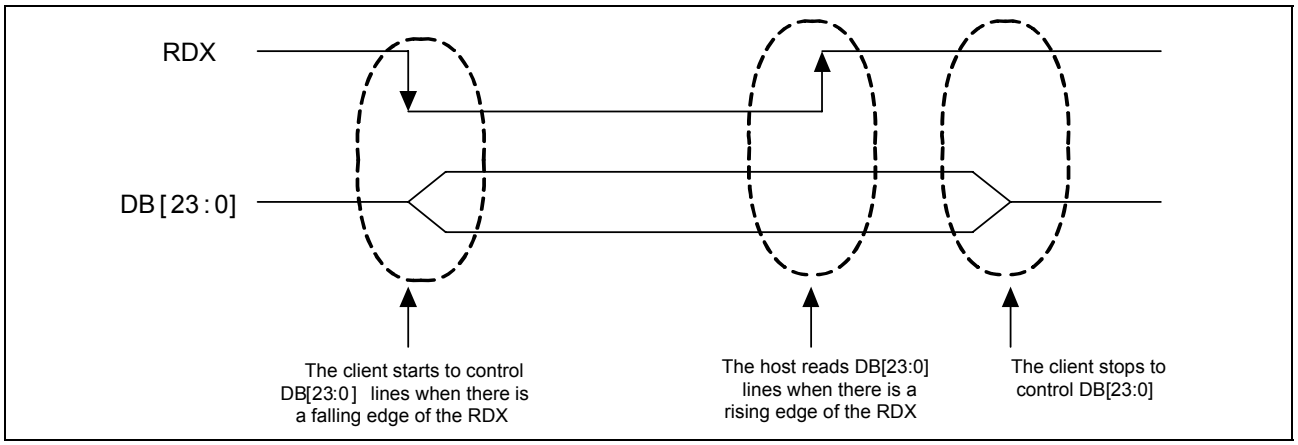


Figure 26. 80-Series RDX protocol

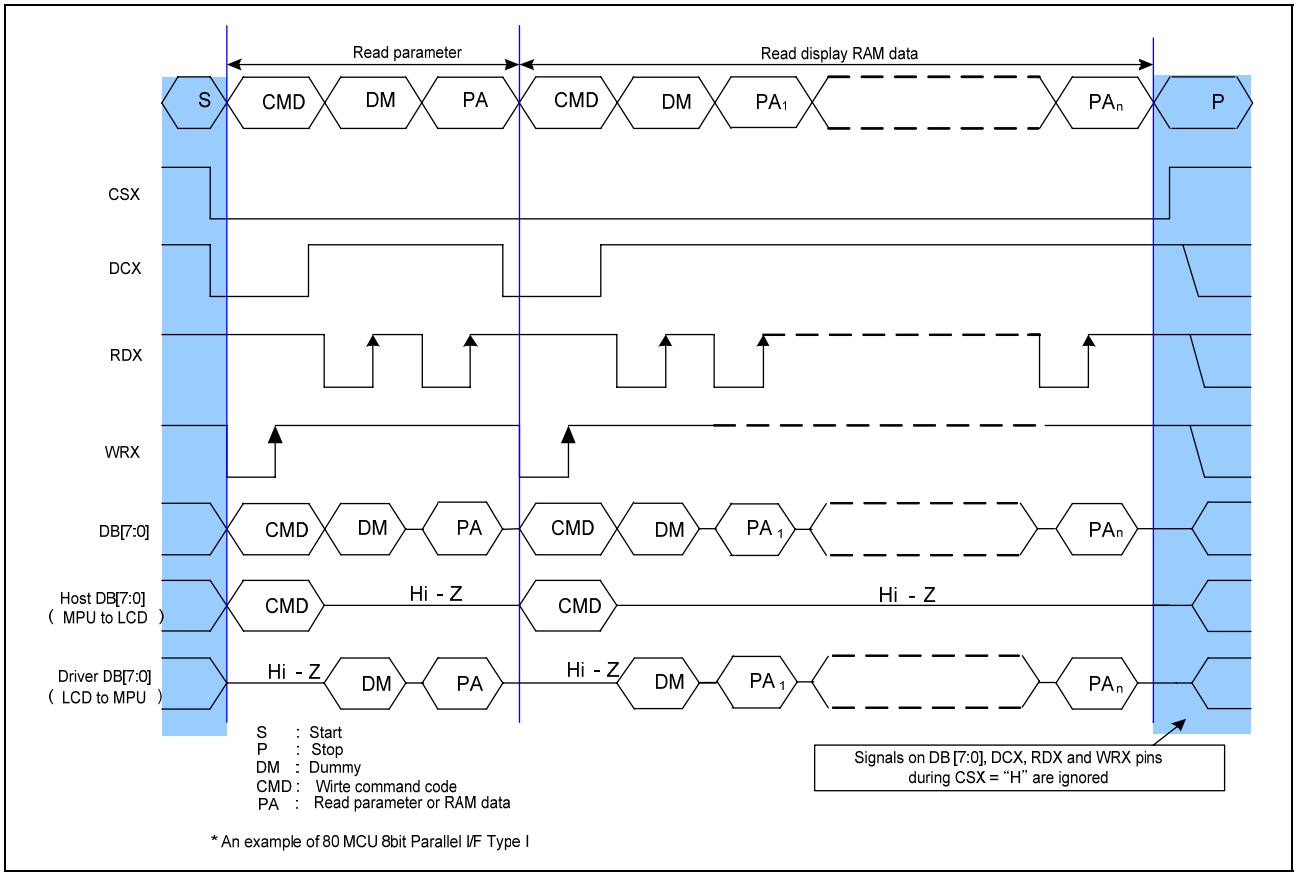


Figure 27. 80-Series parallel bus protocol, read from register or display RAM

3.1.4. Sequence of 4-wire/8-bit Serial Interface

The serial interface is 4-wire/8-bit interface for communication between the micro controller and the LCD driver chip. The 4-wire serial use: CSX (chip enable), DCX (Data / Command selection pad), SCL (WRX) and SDI are used for interface with MCU only, so it can be stopped when no communication is necessary.

3.1.4.1. Write Sequence of 4-wire/8-bit Serial Interface

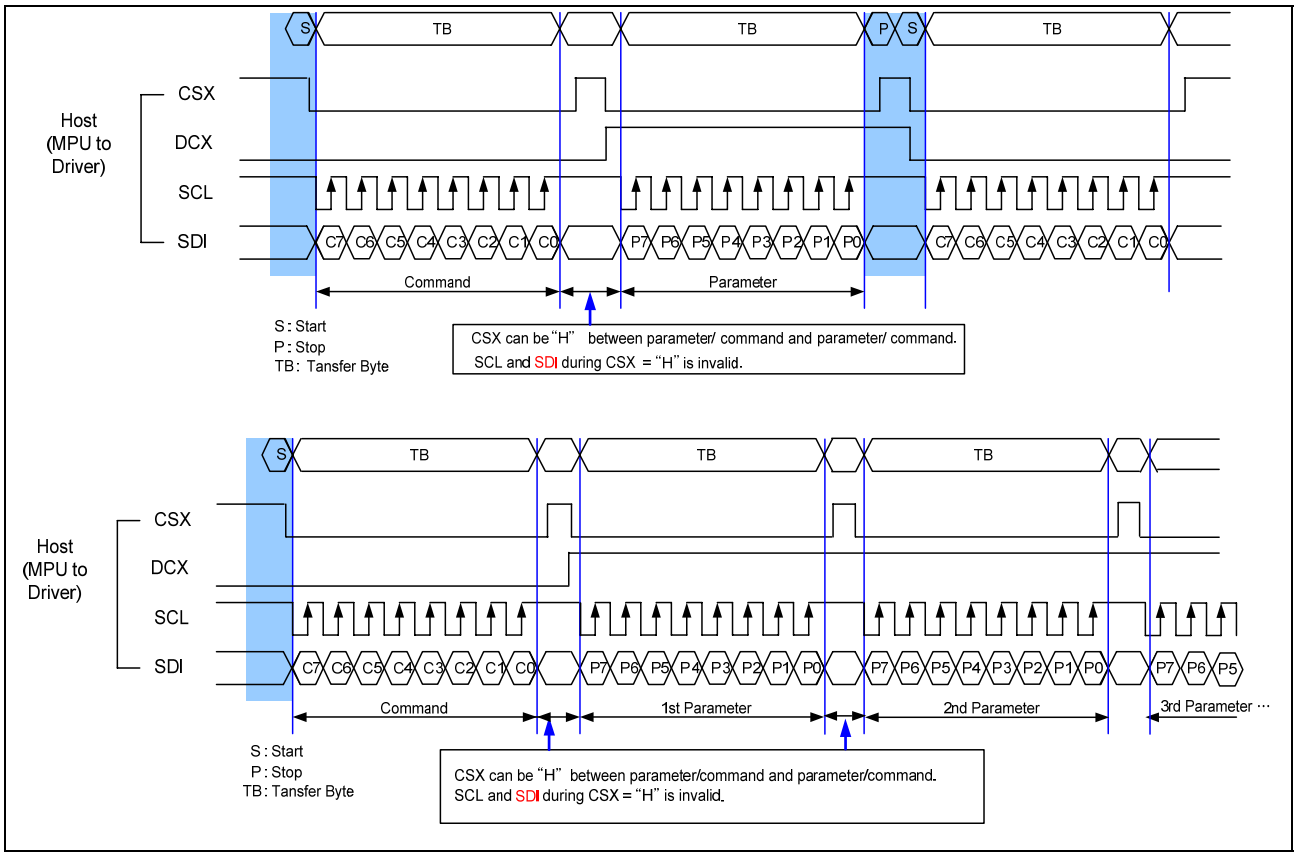


Figure 28. 4-wire/8-bit Data serial interface write mode

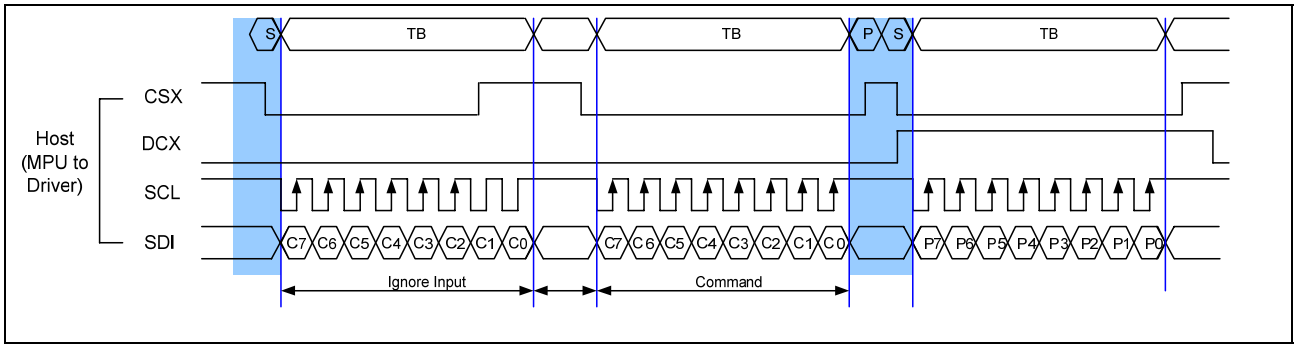


Figure 29. 4-wire/8-bit Data serial interface write mode (CSX="H" during transmission)

3.1.4.2. Read Sequence of 4-wire/8-bit Serial Interface

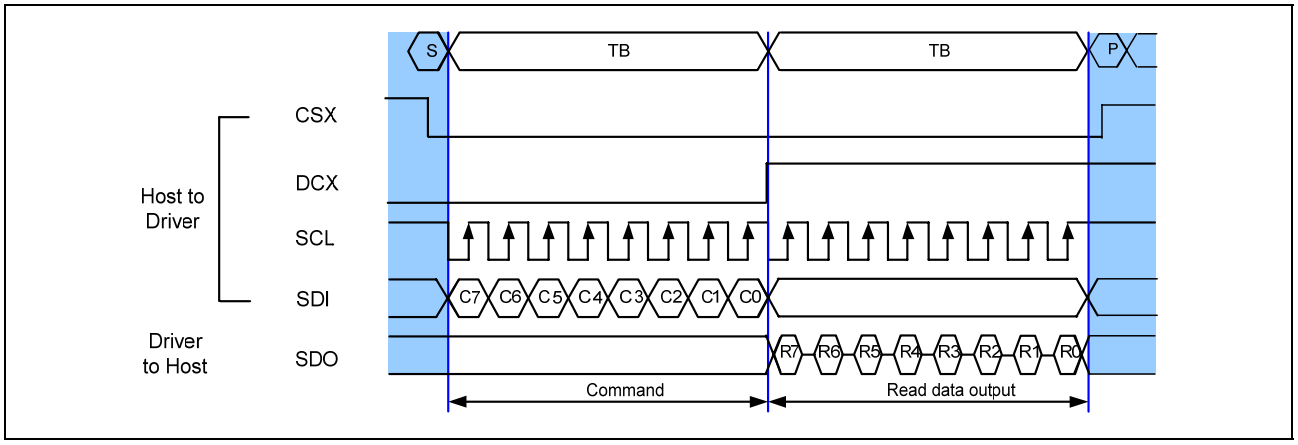


Figure 30. 4-wire/8-bit Data serial interface read 1-byte mode

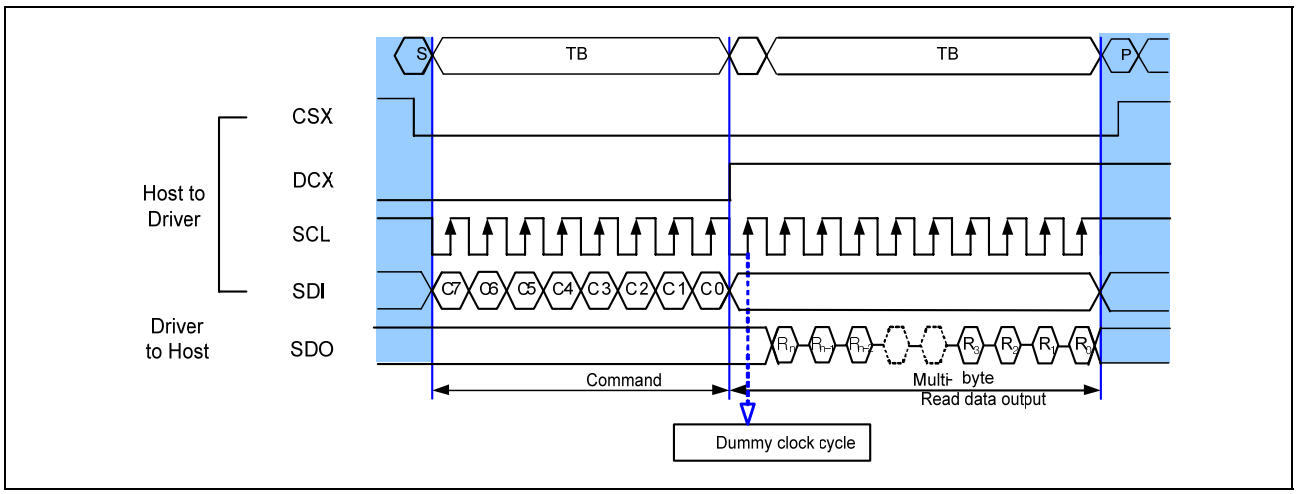


Figure 31. 4-wire/8-bit Data serial interface read multi-byte mode

3.1.5. Sequence of 3-wire/9-bit Serial Interface

The serial interface is 3-wire/9-bit interface for communication between the micro controller and the LCD driver chip. The 3-wire serial use: CSX, SCL (DCX) and SDI are used for interface with MCU only, so it can be stopped when no communication is necessary.

3.1.5.1. Write Sequence of 3-wire/9-bit Serial Interface

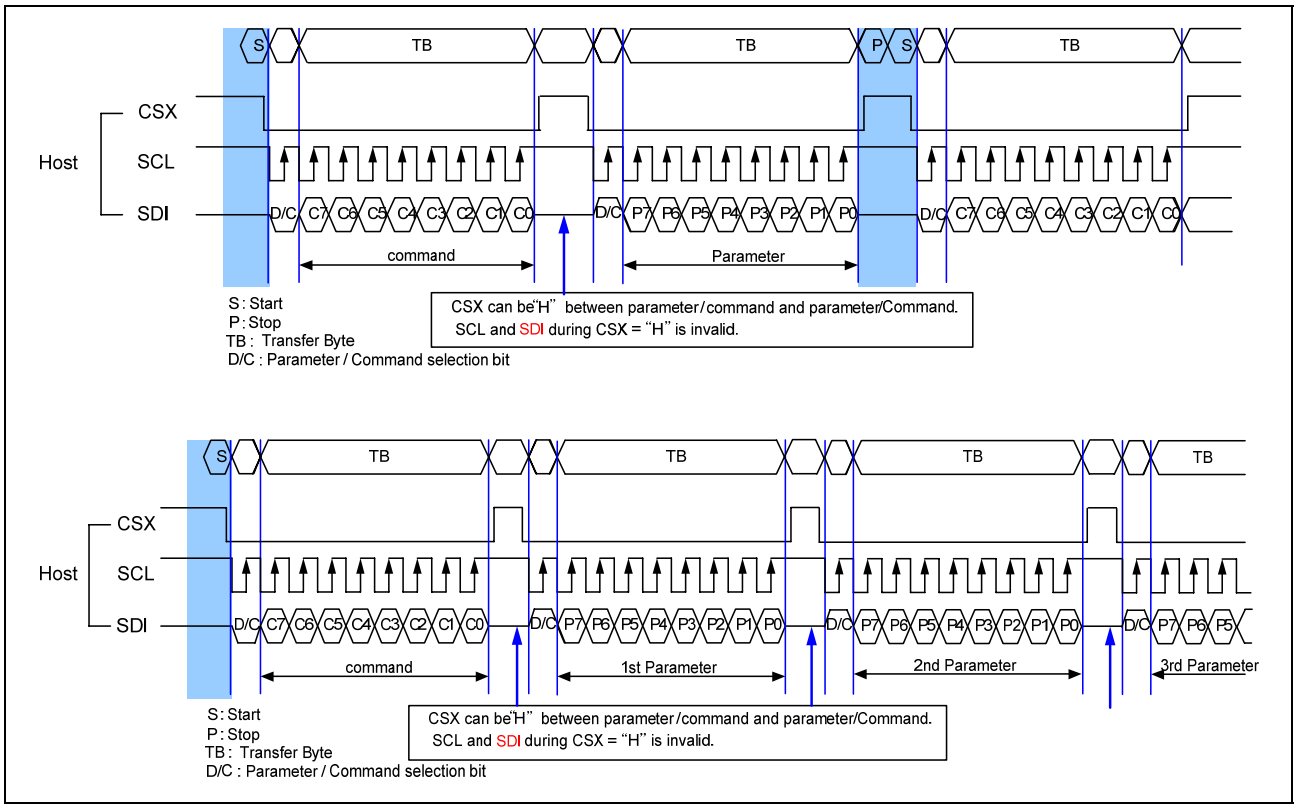


Figure 32. 3-wire/9-bit Data serial interface write mode

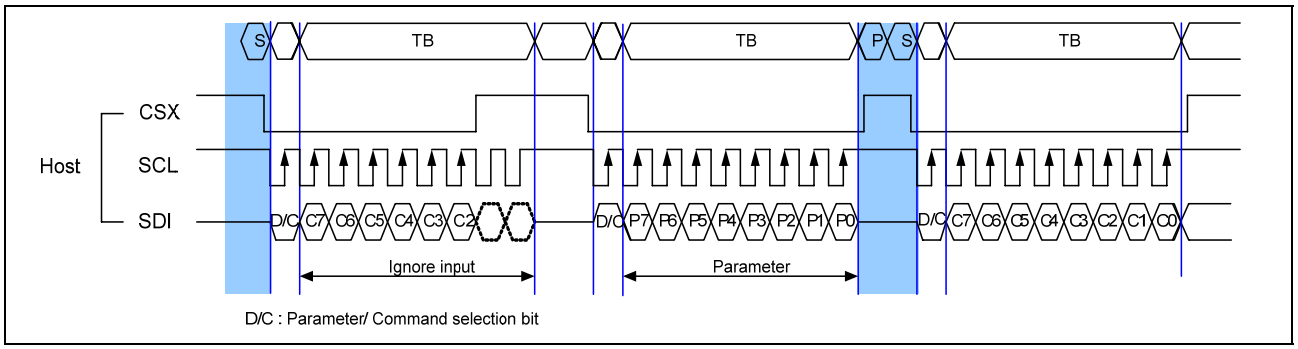


Figure 33. 3-wire/9-bit Data serial interface write mode (CSX="H" during transmission)

3.1.5.2. Read Sequence of 3-wire/9-bit Serial Interface

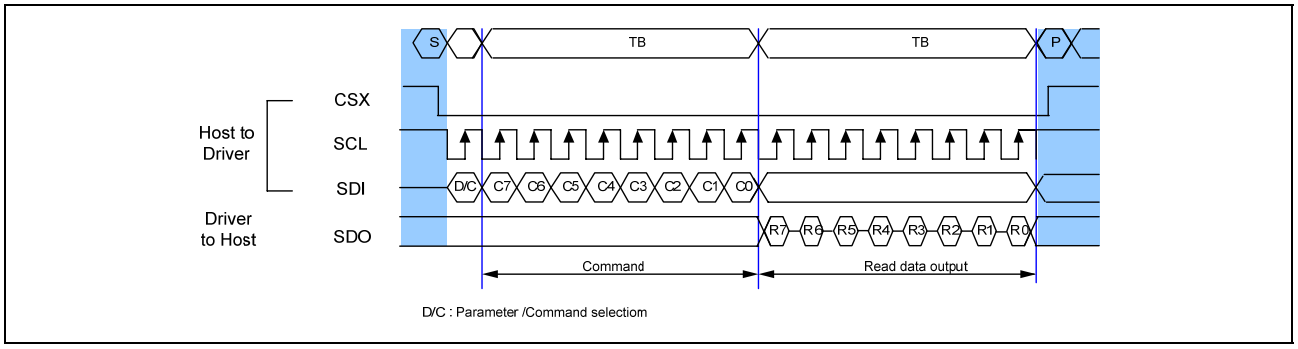


Figure 34. 3-wire/9-bit Data serial interface read 1-byte mode

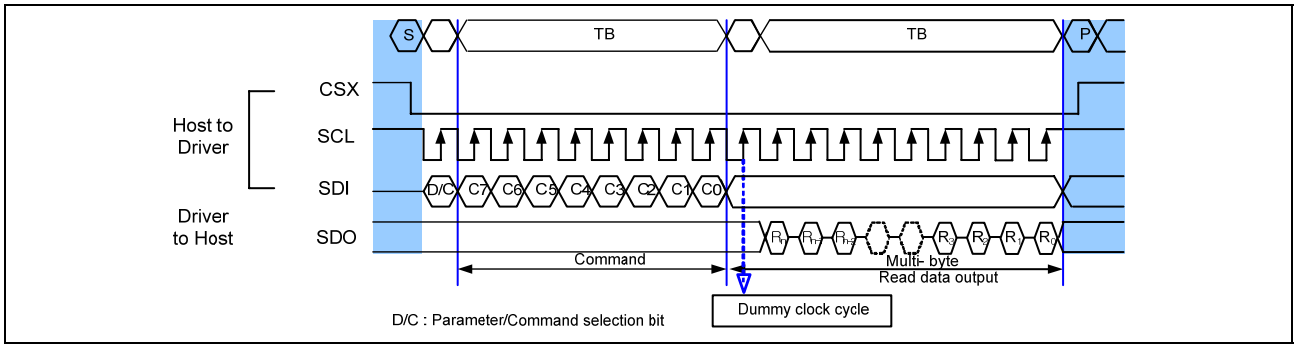


Figure 35. 3-wire/9-bit Data serial interface read multi-byte mode

3.1.6. Description of MPU Interface

The parallel interface of the S6D04D1 can communicated with the MCU using 24 bit bidirectional data bus (DB23 to DB0) to transfer command, parameter and display data.

3.1.6.1. Bidirectional Data Bus

The purpose of MCU interface in the S6D04D1 is to communicate with the MCU in a direct connection. If the driver IC is not selected (CSX = H), the data bus (data line) is placed in the high-impedance state to prevent the other driver IC's from adverse effects. When the driver IC is not selected, inputs through the MCU interface (DCX, RDX, and WRX) have no effect. The example below represents the 80 MCU 24bit Parallel interfaces.

Table 32. Bidirectional data bus description of MCU 24bit

DCX	WRX	RDX	Description
L	↑	1	Command write Commands are input to DB7 to DB0.
H	↑	1	Parameter or display data write Parameters and display data are respectively input to DB7 to DB0 and DB23 to DB0.
H	1	↑	Parameter or display data read Parameters and display data are respectively output to DB7 to DB0 and DB23 to DB0. or dummy data read (1st output data after read command).

3.1.6.2. Data Transfer Pause

It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then S6D04D1 will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command as been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

This applies to the following 4 conditions:

1) Command-Pause-Command

2) Command-Pause-Parameter

3) Parameter-Pause-Command

4) Parameter-Pause-Parameter

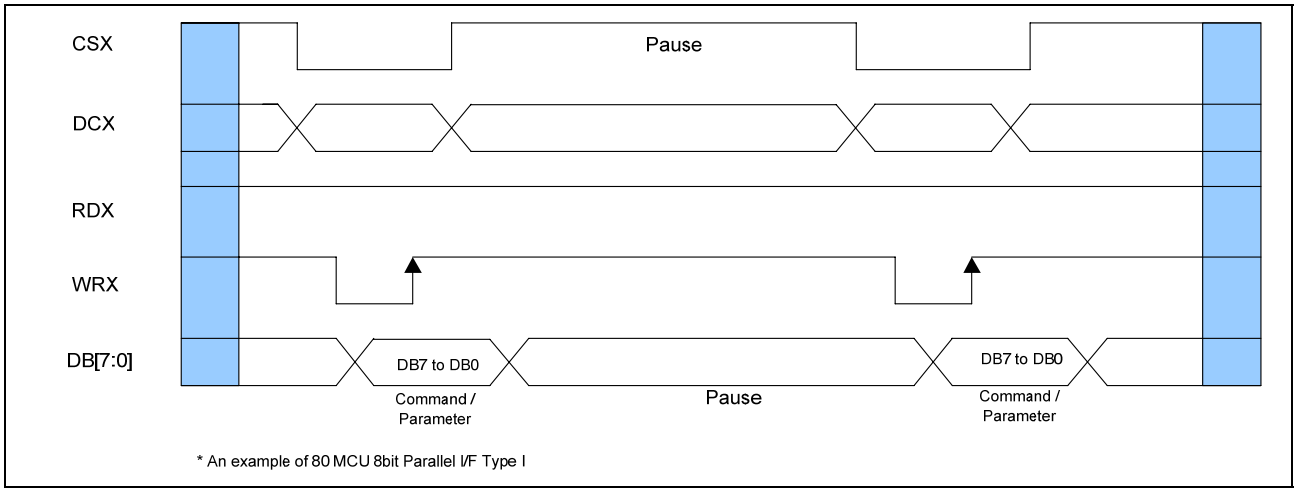


Figure 36. Parallel interface pause

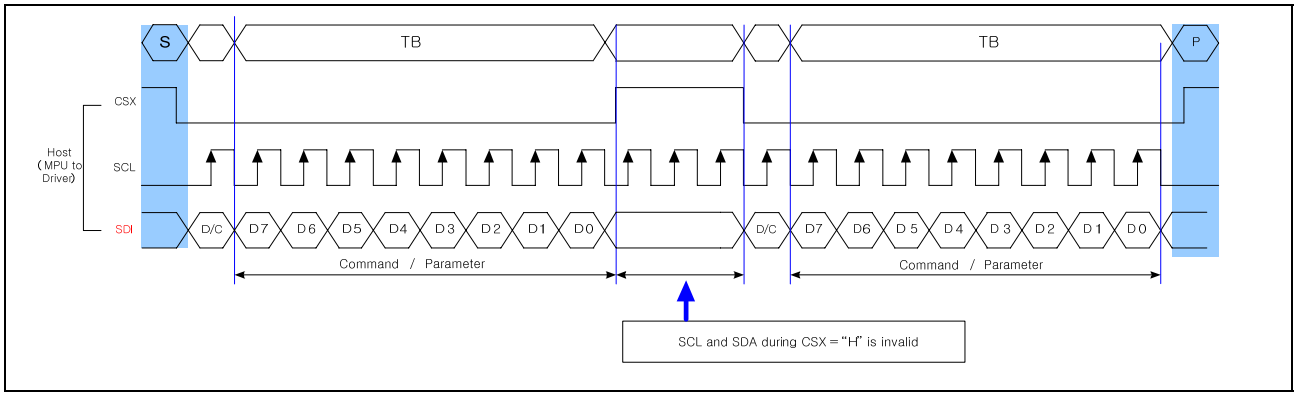


Figure 37. Serial interface Pause

3.1.6.3. Data Transfer Recovery

If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before SDI of the byte has been completed, then S6D04D1 will reject the previous bits have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX has reached the High state.

If there is a break in data transmission by CSX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before SDI of the byte has been completed, then S6D04D1 will reject the previous bits and reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated.

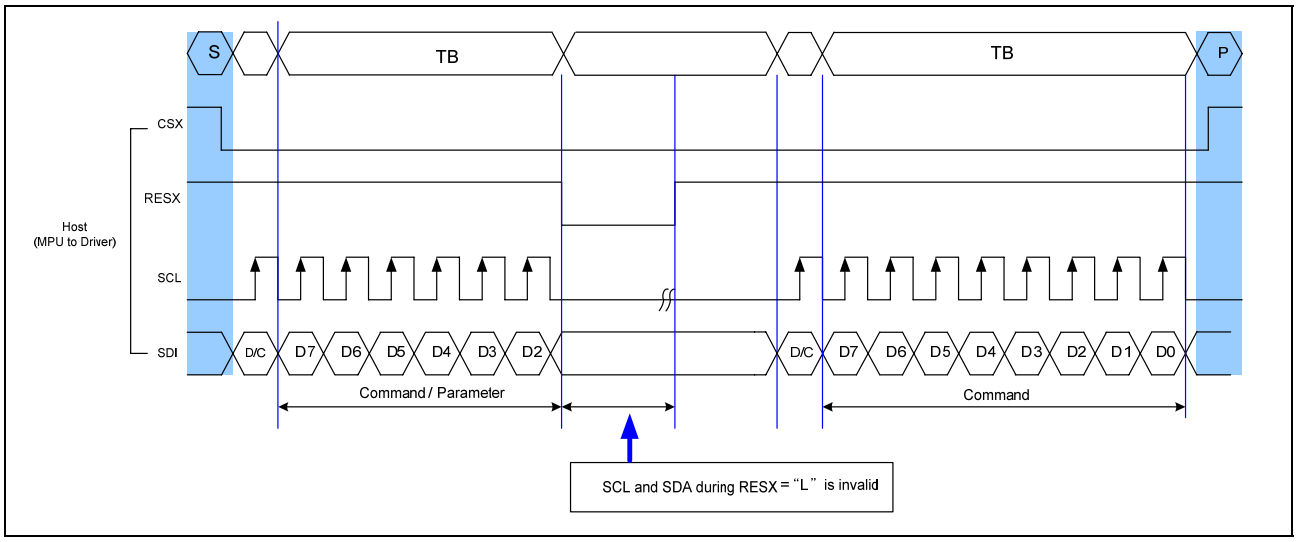


Figure 38. Serial bus protocol, write mode – interrupted by RESX (3-wire 9bit data serial I/F)

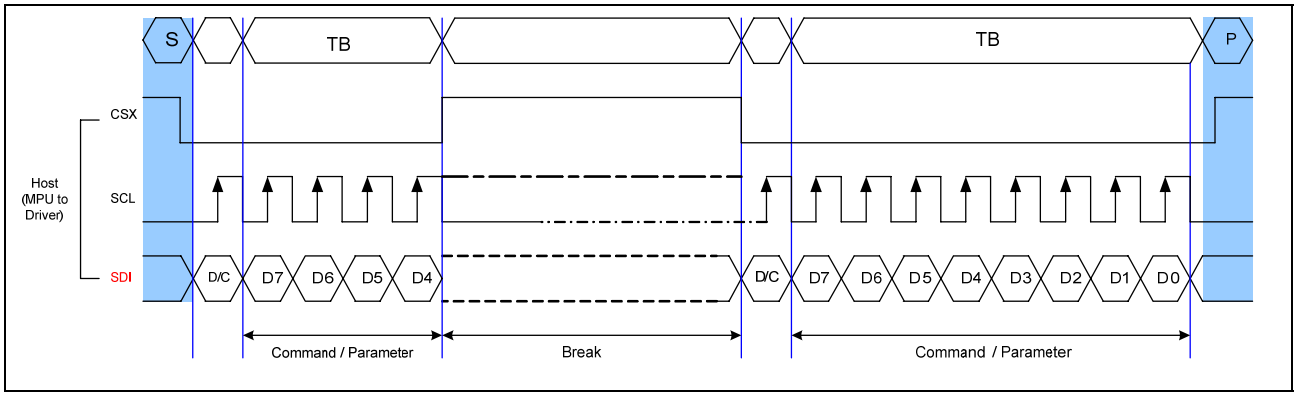


Figure 39. Serial bus protocol, write mode – interrupted by CSX (3-wire 9bit data serial I/F)

If 1, 2 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown in following Figure.

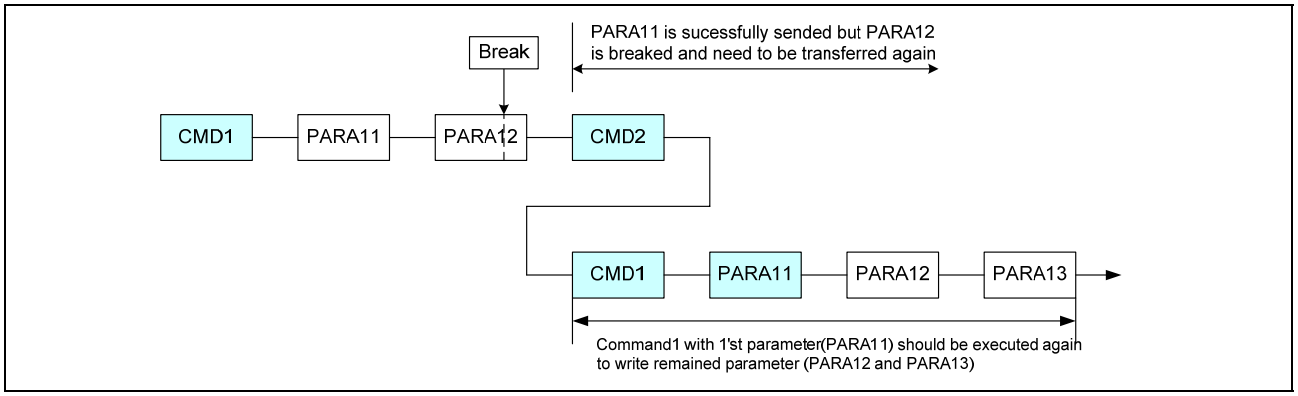


Figure 40. Write interrupt recovery (serial interface)

If 2 or more parameter command are being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains in the previous value.

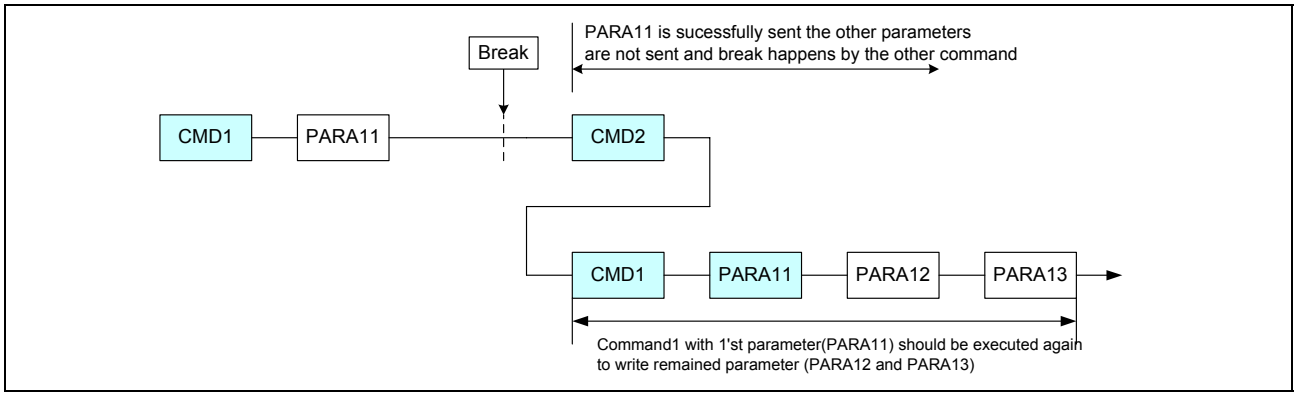


Figure 41. Write interrupt recovery (both serial and parallel interface)

3.1.6.4. Display Module Data Transfer Modes

The Module has 2 color modes for transferring data to the display RAM. Data can be downloaded to the Frame Memory by 2 methods.

Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.

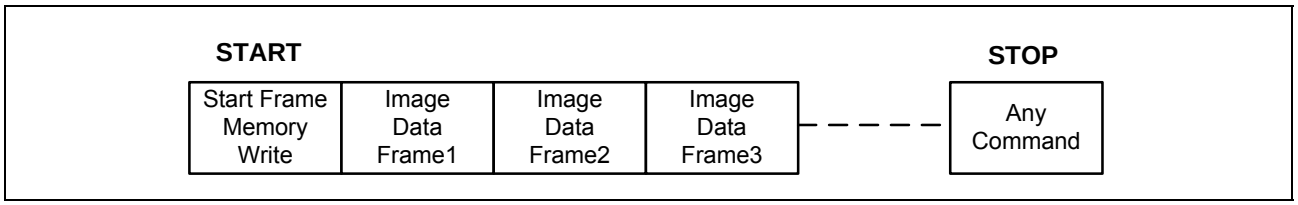


Figure 42. Image data writing method 1

Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Frame Memory Write command is sent, and a new Frame is downloaded.

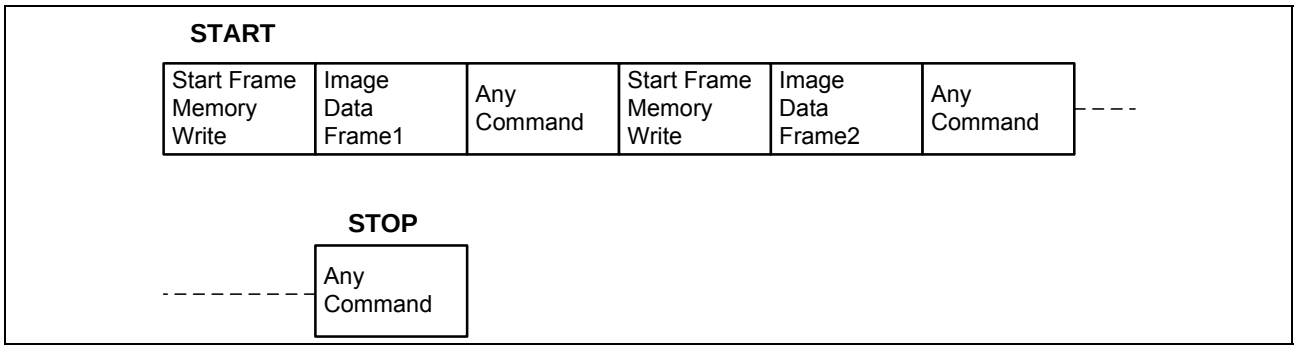


Figure 43. Image data writing method 2

Note. These methods apply to all Data Transfer Color modes on any interfaces.

The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.

3.2. DISPLAY MODULE DATA COLOR CODING

Various data formats are available in which display data can be written to the display data RAM. It is possible to choose a format suitable for the purpose of use. The data format is determined by a combination of COLMOD and MDT commands.

3.2.1. Display Data Format for Write

Table 33. Display data format for wirte

Color mode	Interface (IM[2:0])				
	24bit	18bit	16bit	9bit	8bit
16M Color (COLMOD[2:0] = 111)	24bit 888 1/1 (MDT=00)	16bit 888 2/3 (MDT=00)	16bit 888 2/3 (MDT=00)	8bit 888 1/3 (MDT=00)	8bit 888 1/3 (MDT=00)
		16bit 888 1/2 (MDT=01)	16bit 888 1/2 (MDT=01)		
262k Color (COLMOD[2:0] = 110)	18bit 666 1/1 (MDT=00)	18bit 666 1/1 (MDT=00)	12bit 666 2/3 (MDT=00)	9bit 666 1/2 (MDT=00)	6bit 666 1/3 (MDT=00)
			12bit 666 1/2 (MDT=01)	6bit 666 1/3 (MDT=01)	
			16bit 666 1/2 (MDT=10)		
			16bit 666 1/2 (MDT=11)		
65k Color (COLMOD[2:0] = 101)	16bit 565 1/1 (MDT=00)	16bit 565 1/1 (MDT=00)	16bit 565 1/1 (MDT=00)	8bit 565 1/2 (MDT=00)	8bit 565 1/2 (MDT=00)

Note1. Display data expand (666 → 888 or 565 → 888) method is decided by IPM command. In default condition (IPM = "100"), MSB data are copied to LSB data for expanding. See Figure. 44 and Figure. 45.

Note2. Registers set related to data format (IPM, MDT,..) are on the F6H command (Level 2)

In 65k color mode (16-bit data) data bit should be expanded to 24-bit like below. It will be used "IPM=100"

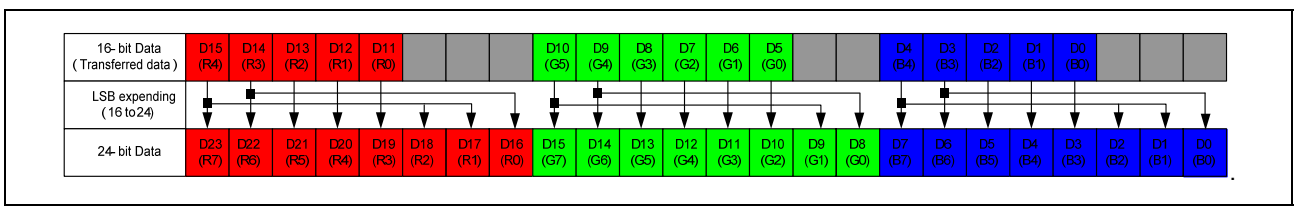


Figure 44. Data expand method (65K color mode)

In 262k color mode (18-bit data) data bit should be expanded to 24-bit like below. It will be used "IPM=100"

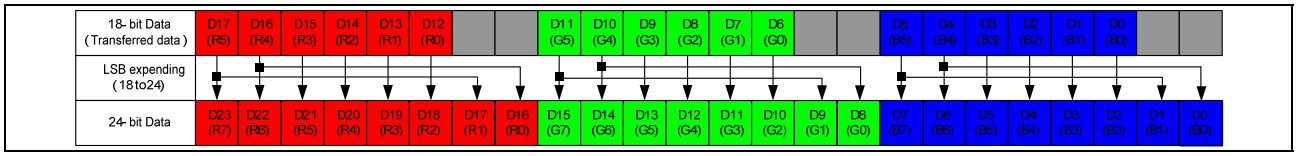


Figure 45. Data expand method (262K color mode)

3.2.2. Display Data Format for Read

3.2.2.1. Read Data Format

In every color mode, output display data is 24bit.

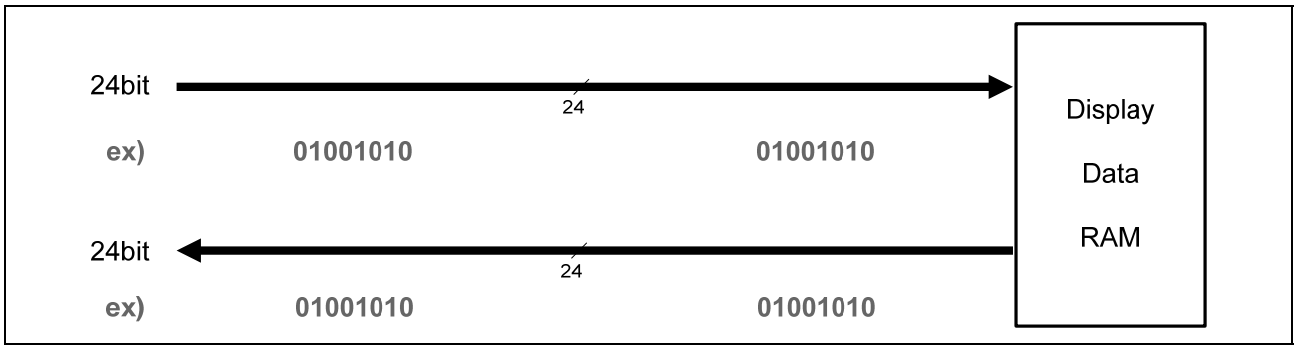


Figure 46. Case of 16M color mode (IPM=”100”)

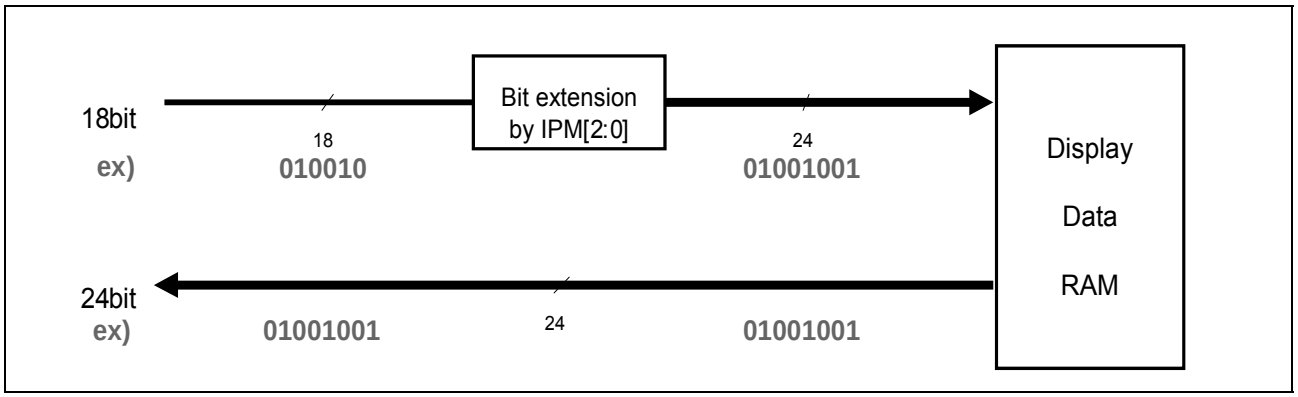


Figure 47. Case of 262K color mode (IPM=”100”)

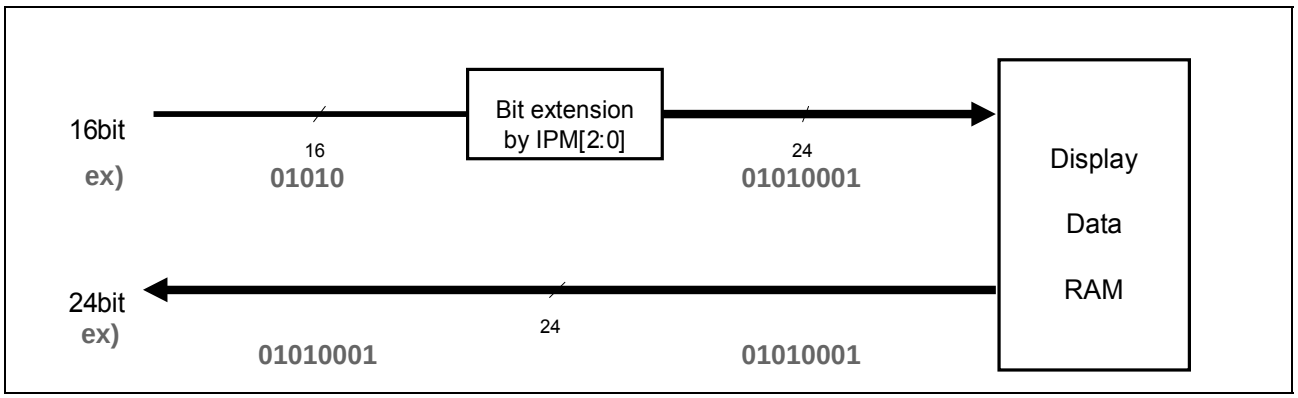


Figure 48. Case of 65K color mode (IPM=”100”)

3.2.2.2. Display data read sequence.

Regardless of color mode, output display data is 24bit.

24bit Interface

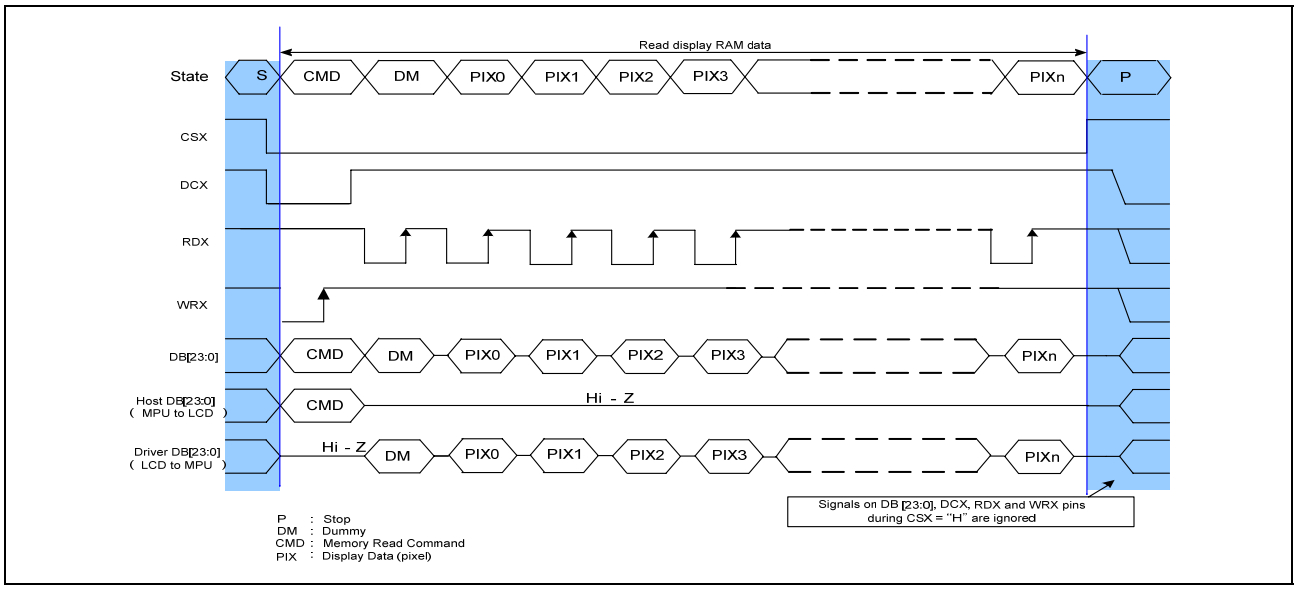


Figure 49. Display data read (24bit Interface)

8bit Interface

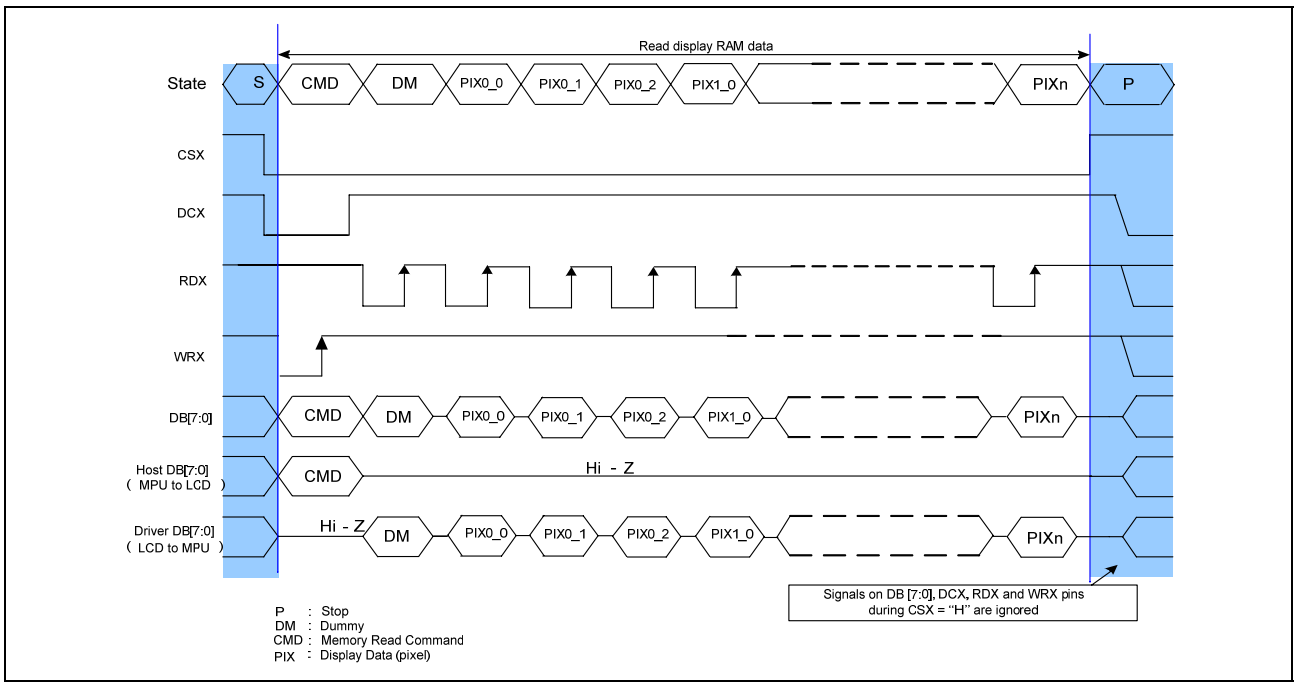


Figure 50. Display data read (8bit Interface)

16bit Interface

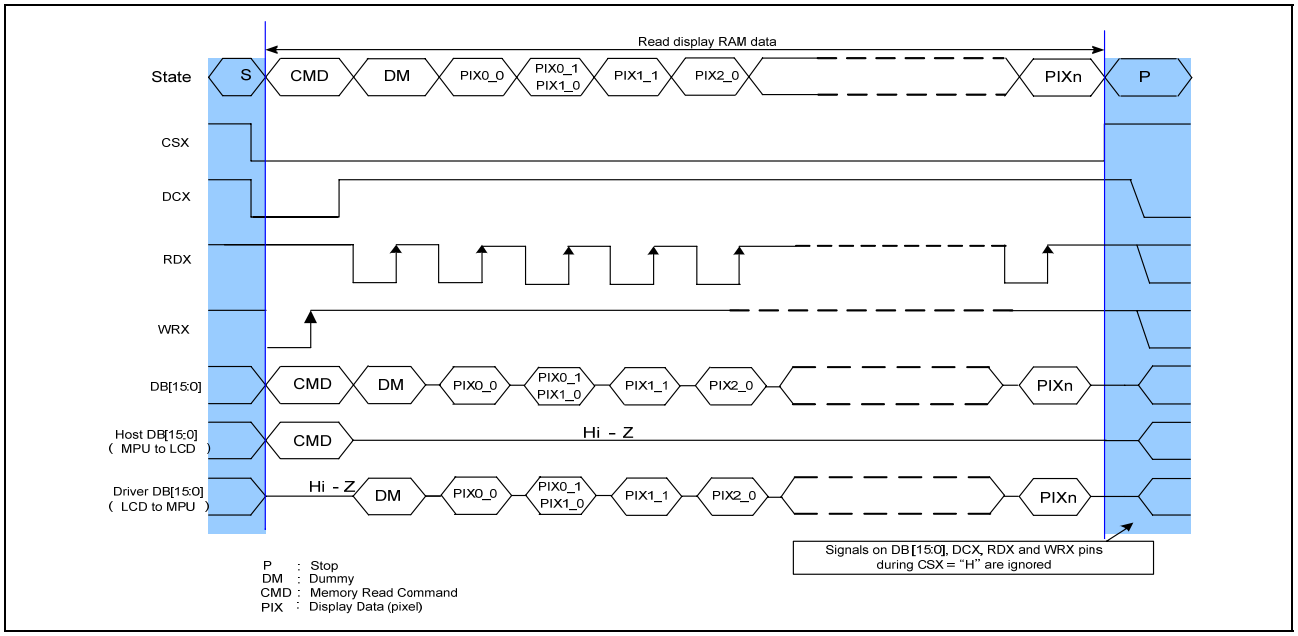


Figure 51. Display data read (16bit Interface: MDT=00)

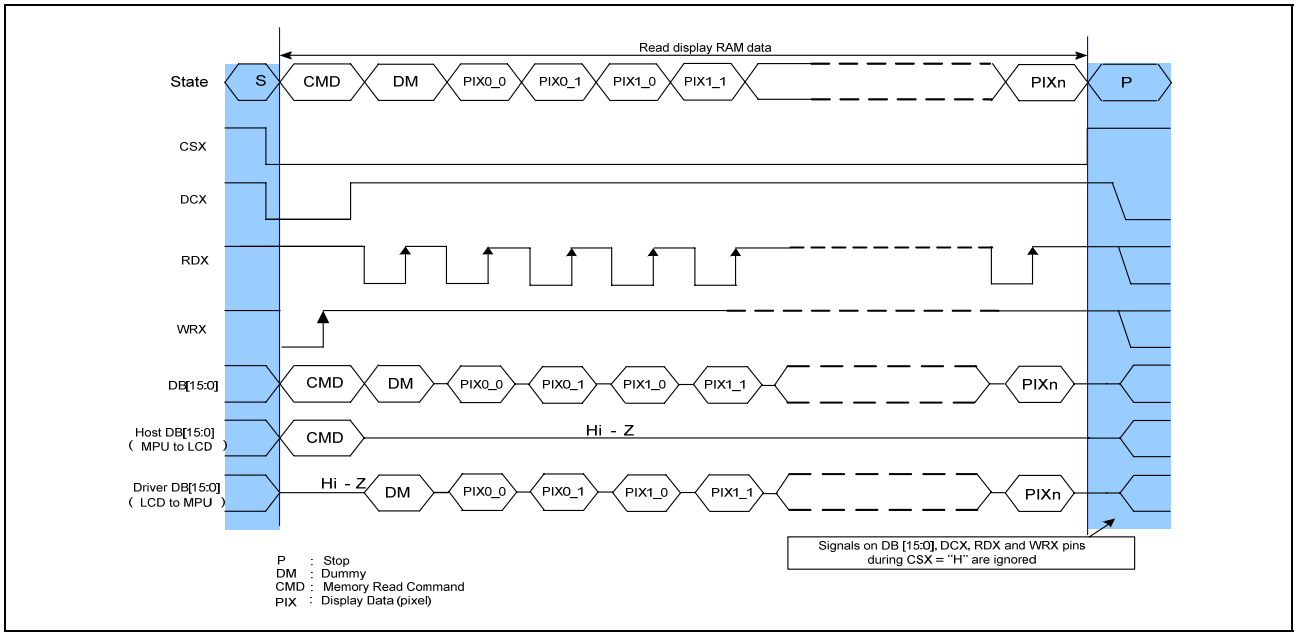


Figure 52. Display data read (16bit Interface: MDT=01)

Note. If MDT[1:0] register set to "10" or "11", data read sequence operate as MDT = 00.

9bit Interface

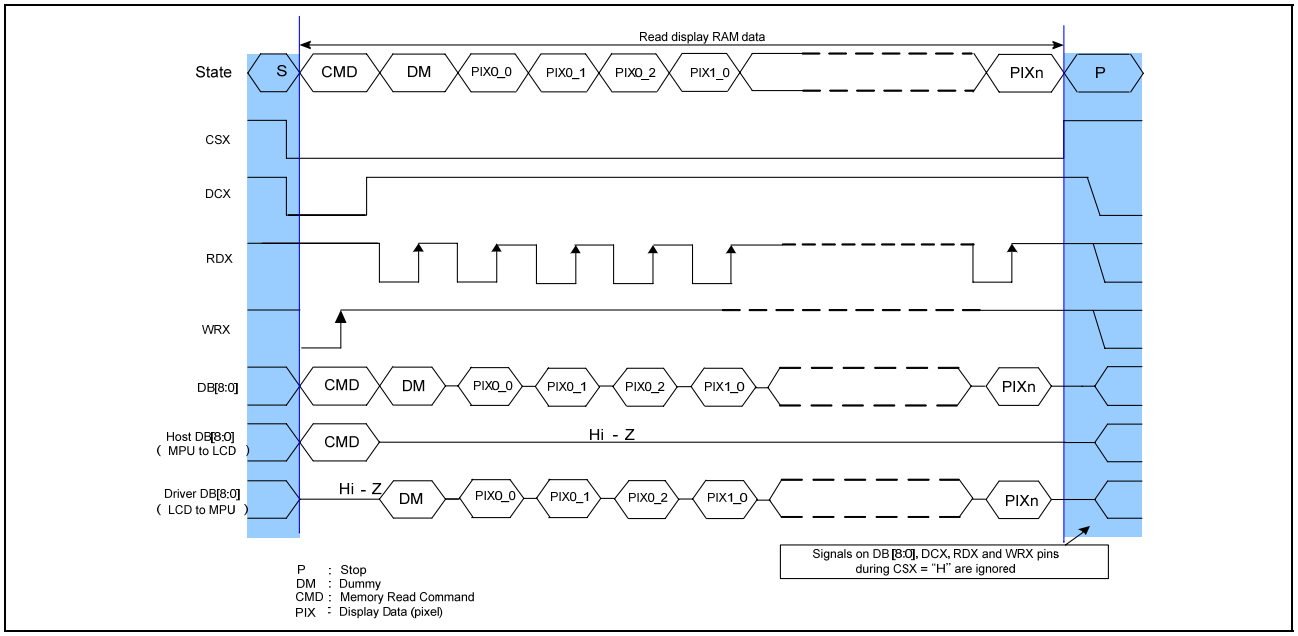


Figure 53. Display data read (9bit Interface: MDT=00)

Note. If MDT[1:0] register set to "01", "10" or "11", data read sequence operate as MDT = 00.

18bit Interface

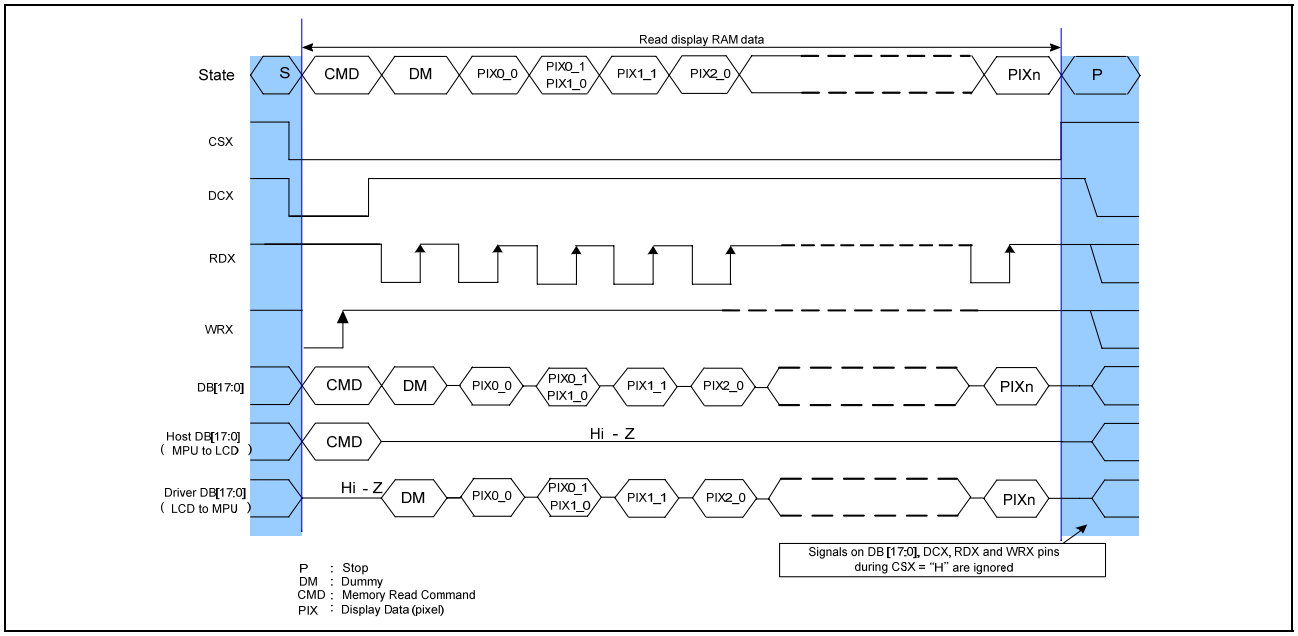


Figure 54. Display data read (18bit Interface: MDT=00)

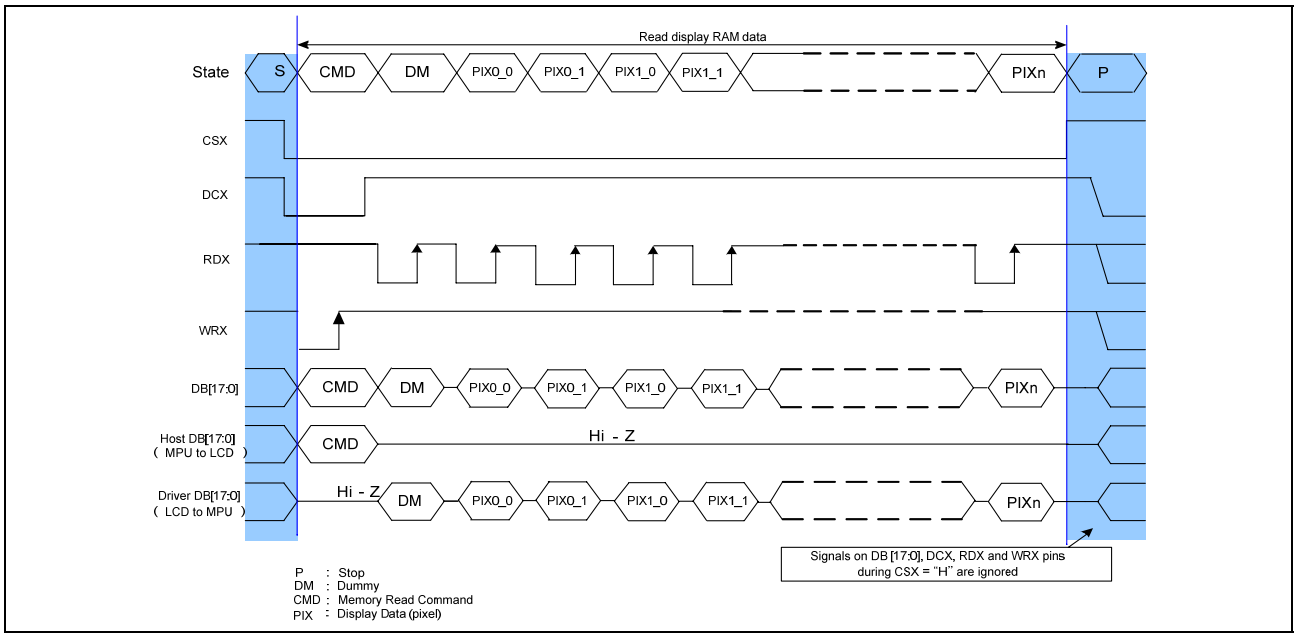


Figure 55. Display data read (18bit Interface: MDT=01)

Note. If MDT[1:0] register set to "10" or "11", data read sequence operate as MDT = 00.

3.2.3. 16M Color Mode

For the display data to be accessed in 16M color mode, it is necessary that 16M color mode be selected (B2 to B0: 111) using COLMOD command before writing/reading to or from the display data RAM. In this mode, the display data per pixel comprised of 8 bits for R, 8 bits for G and 8 bits for B is written to the display data RAM. When all of the data for one pixel (RGB) is prepared in the internal register, the MCU writes the data to the display data RAM. When the display data is read from the display data RAM after RAMRD command is issued, 1 byte of dummy read cycle is needed. For detail information of data read format, refer to section 3.2.2.

Table 34. 24-bit Parallel interface for 888 1/1 formats (MDT = 00)

count	0	1	2	…	239	240
D/CX	0	1	1	…	1	1
D23		0R7	1R7	…	238R7	239R7
D22		0R6	1R6	…	238R6	239R6
D21		0R5	1R5	…	238R5	239R5
D20		0R4	1R4	…	238R4	239R4
D19		0R3	1R3	…	238R3	239R3
D18		0R2	1R2	…	238R2	239R2
D17		0R1	1R1	…	238R1	239R1
D16		0R0	1R0	…	238R0	239R0
D15		0G7	1G7	…	238G7	239G7
D14		0G6	1G6	…	238G6	239G6
D13		0G5	1G5	…	238G5	239G5
D12		0G4	1G4	…	238G4	239G4
D11		0G3	1G3	…	238G3	239G3
D10		0G2	1G2	…	238G2	239G2
D9		0G1	1G1	…	238G1	239G1
D8		0G0	1G0	…	238G0	239G0
D7	C7	0B7	1B7	…	238B7	239B7
D6	C6	0B6	1B6	…	238B6	239B6
D5	C5	0B5	1B5	…	238B5	239B5
D4	C4	0B4	1B4	…	238B4	239B4
D3	C3	0B3	1B3	…	238B3	239B3
D2	C2	0B2	1B2	…	238B2	239B2
D1	C1	0B1	1B1	…	238B1	239B1
D0	C0	0B0	1B0	…	238B0	239B0

Table 35. 8-bit Parallel interface for 888 1/3 formats (MDT = 00)

count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D7	C7	0R7	0G7	0B7	…	239R7	239G7	239B7
D6	C6	0R6	0G6	0B6	…	239R6	239G6	239B6
D5	C5	0R5	0G2	0B5	…	239R5	239G5	239B5
D4	C4	0R4	0G1	0B4	…	239R4	239G4	239B4
D3	C3	0R3	0G0	0B3	…	239R3	239G3	239B3
D2	C2	0R2	0G2	0B2	…	239R2	239G2	239B2
D1	C1	0R1	0G1	0B1	…	239R1	239G1	239B1
D0	C0	0R0	0G0	0B0	…	239R0	239G0	239B0

Table 36. 16-bit Parallel interface for 888 2/3 formats (MDT = 00)

count	0	1	2	3	…	358	359	360
D/CX	0	1	1	1	…	1	1	1
D15		0R7	0B7	1G7	…	238R7	238B6	239G7
D14		0R6	0B6	1G6	…	238R6	238B5	239G6
D13		0R5	0B5	1G5	…	238R5	238B5	239G5
D12		0R4	0B4	1G4	…	238R4	238B4	239G4
D11		0R3	0B3	1G3	…	238R3	238B3	239G3
D10		0R2	0B2	1G2	…	238R2	238B2	239G2
D9		0R1	0B1	1G1	…	238R1	238B1	239G1
D8		0R0	0B0	1G0	…	238R0	238B0	239G0
D7	C7	0G7	1R7	1B7	…	238G7	239R7	239B7
D6	C6	0G6	1R6	1B6	…	238G6	239R6	239B6
D5	C5	0G5	1R5	1B5	…	238G5	239R5	239B5
D4	C4	0G4	1R4	1B4	…	238G4	239R4	239B4
D3	C3	0G3	1R3	1B3	…	238G3	239R3	239B3
D2	C2	0G2	1R2	1B2	…	238G2	239R2	239B2
D1	C1	0G1	1R1	1B1	…	238G1	239R1	239B1
D0	C0	0G0	1R0	1B0	…	238G0	239R0	239B0

Table 37. 16-bit Parallel interface for 888 1/2 formats (MDT = 01)

count	0	1	2	3	4	…	479	480
D/CX	0	1	1	1	1	…	1	1
D15		0R7	0B7	1R7	1B7	…	239R7	239B7
D14		0R6	0B6	1R6	1B6	…	239R6	239B6
D13		0R5	0B5	1R5	1B5	…	239R5	239B5
D12		0R4	0B4	1R4	1B4	…	239R4	239B4
D11		0R3	0B3	1R3	1B3	…	239R3	239B3
D10		0R2	0B2	1R2	1B2	…	239R2	239B2
D9		0R1	0B1	1R1	1B1	…	239R1	239B1
D8		0R0	0B0	1R0	1B0	…	239R0	239B0
D7	C7	0G7		1G7		…	239G7	
D6	C6	0G6		1G6		…	239G6	
D5	C5	0G5		1G5		…	239G5	
D4	C4	0G4		1G4		…	239G4	
D3	C3	0G3		1G3		…	239G3	
D2	C2	0G2		1G2		…	239G2	
D1	C1	0G1		1G1		…	239G1	
D0	C0	0G0		1G0		…	239G0	

Table 38. 9-bit Parallel Interface for 888 1/3 formats (MDT = 00)

count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D8								
D7	C7	0R7	0G7	0B7	…	239R7	239G7	239B7
D6	C6	0R6	0G6	0B6	…	239R6	239G6	239B6
D5	C5	0R5	0G2	0B5	…	239R5	239G5	239B5
D4	C4	0R4	0G1	0B4	…	239R4	239G4	239B4
z	C3	0R3	0G0	0B3	…	239R3	239G3	239B3
D2	C2	0R2	0G2	0B2	…	239R2	239G2	239B2
D1	C1	0R1	0G1	0B1	…	239R1	239G1	239B1
D0	C0	0R0	0G0	0B0	…	239R0	239G0	239B0

Table 39. 18-bit Parallel interface for 888 2/3 formats (MDT = 00)

count	0	1	2	3	…	358	359	360
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R7	0B7	1G7	…	238R7	238B6	239G7
D14		0R6	0B6	1G6	…	238R6	238B5	239G6
D13		0R5	0B5	1G5	…	238R5	238B5	239G5
D12		0R4	0B4	1G4	…	238R4	238B4	239G4
D11		0R3	0B3	1G3	…	238R3	238B3	239G3
D10		0R2	0B2	1G2	…	238R2	238B2	239G2
D9		0R1	0B1	1G1		238R1	238B1	239G1
D8		0R0	0B0	1G0		238R0	238B0	239G0
D7	C7	0G7	1R7	1B7	…	238G7	239R7	239B7
D6	C6	0G6	1R6	1B6	…	238G6	239R6	239B6
D5	C5	0G5	1R5	1B5	…	238G5	239R5	239B5
D4	C4	0G4	1R4	1B4	…	238G4	239R4	239B4
D3	C3	0G3	1R3	1B3	…	238G3	239R3	239B3
D2	C2	0G2	1R2	1B2	…	238G2	239R2	239B2
D1	C1	0G1	1R1	1B1	…	238G1	239R1	239B1
D0	C0	0G0	1R0	1B0		238G0	239R0	239B0

Table 40. 18-bit Parallel Interface for 888 1/2 formats (MDT = 01)

count	0	1	2	3	4	…	479	480
D/CX	0	1	1	1	1	…	1	1
D17						…		
D16						…		
D15		0R7	0B7	1R7	1B7	…	239R7	239B7
D14		0R6	0B6	1R6	1B6	…	239R6	239B6
D13		0R5	0B5	1R5	1B5	…	239R5	239B5
D12		0R4	0B4	1R4	1B4	…	239R4	239B4
D11		0R3	0B3	1R3	1B3	…	239R3	239B3
D10		0R2	0B2	1R2	1B2	…	239R2	239B2
D9		0R1	0B1	1R1	1B1		239R1	239B1
D8		0R0	0B0	1R0	1B0	…	239R0	239B0
D7	C7	0G7		1G7		…	239G7	
D6	C6	0G6		1G6		…	239G6	
D5	C5	0G5		1G5		…	239G5	
D4	C4	0G4		1G4		…	239G4	
D3	C3	0G3		1G3		…	239G3	
D2	C2	0G2		1G2		…	239G2	
D1	C1	0G1		1G1		…	239G1	
D0	C0	0G0		1G0			239G0	

3.2.4. 262k Color Mode

For the display data to be accessed in 262k color mode, it is necessary that 262k color mode be selected (B2 to B0: 110) using COLMOD command before writing/reading to or from the display data RAM. In this mode, the display data per pixel comprised of 6 bits for R, 6 bits for G and 6 bits for B is written to the display data RAM. When all of the data for one pixel (RGB) is prepared in the internal register, the MCU writes the data to the display data RAM. When the display data is read from the display data RAM after RAMRD command is issued, 1 byte of dummy read cycle is needed. For detail information of data read format, refer to section 3.2.2.

Table 41. 24-bit Parallel interface for 666 1/1 formats (MDT = 00)

count	0	1	2	…	239	240
D/CX	0	1	1	…	1	1
D23				…		
D22				…		
D21				…		
D20				…		
D19				…		
D18				…		
D17		0R5	1R5	…	238R5	239R5
D16		0R4	1R4	…	238R4	239R4
D15		0R3	1R3	…	238R3	239R3
D14		0R2	1R2	…	238R2	239R2
D13		0R1	1R1	…	238R1	239R1
D12		0R0	1R0	…	238R0	239R0
D11		0G5	1G5	…	238G5	239G5
D10		0G4	1G4	…	238G4	239G4
D9		0G3	1G3	…	238G3	239G3
D8		0G2	1G2	…	238G2	239G2
D7	C7	0G1	1G1	…	238G1	239G1
D6	C6	0G0	1G0	…	238G0	239G0
D5	C5	0B5	1B5	…	238B5	239B5
D4	C4	0B4	1B4		238B4	239B4
D3	C3	0B3	1B3		238B3	239B3
D2	C2	0B2	1B2	…	238B2	239B2
D1	C1	0B1	1B1	…	238B1	239B1
D0	C0	0B0	1B0	…	238B0	239B0

Table 42. 8-bit Parallel interface for 666 1/3 formats (MDT = 00)

count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D7	C7				…			
D6	C6				…			
D5	C5	0R5	0G5	0B5	…	239R5	239G5	239B5
D4	C4	0R4	0G4	0B4	…	239R4	239G4	239B4
D3	C3	0R3	0G3	0B3	…	239R3	239G3	239B3
D2	C2	0R2	0G2	0B2	…	239R2	239G2	239B2
D1	C1	0R1	0G1	0B1	…	239R1	239G1	239B1
D0	C0	0R0	0G0	0B0	…	239R0	239G0	239B0

Table 43. 16-bit Parallel interface for 666 2/3 formats (MDT = 00)

count	0	1	2		…	358	359	360
D/CX	0	1	1		…	1	1	1
D15					…			
D14					…			
D13					…			
D12					…			
D11		0R5	0B5	1G5	…	238R5	238B5	239G5
D10		0R4	0B4	1G4	…	238R4	238B4	239G4
D9		0R3	0B3	1G3	…	238R3	238B3	239G3
D8		0R2	0B2	1G2	…	238R2	238B2	239G2
D7	C7	0R1	0B1	1G1	…	238R1	238B1	239G1
D6	C6	0R0	0B0	1G0	…	238R0	238B0	239G0
D5	C5	0G5	1R5	1B5	…	238G5	239R5	239B5
D4	C4	0G4	1R4	1B4	…	238G4	239R4	239B4
D3	C3	0G3	1R3	1B3	…	238G3	239R3	239B3
D2	C2	0G2	1R2	1B2	…	238G2	239R2	239B2
D1	C1	0G1	1R1	1B1	…	238G1	239R1	239B1
D0	C0	0G0	1R0	1B0	…	238G0	239R0	239B0

Table 44. 16-bit Parallel interface for 666 1/2 formats (MDT = 01)

count	0	1	2	3	4	…	479	480
D/CX	0	1	1	1	1	…	1	1
D15						…		
D14						…		
D13						…		
D12						…		
D11		0R5	0B5	1R5	1B5	…	239R5	239B5
D10		0R4	0B4	1R4	1B4	…	239R4	239B4
D9		0R3	0B3	1R3	1B3	…	239R3	239B3
D8		0R2	0B2	1R2	1B2	…	239R2	239B2
D7	C7	0R1	0B1	1R1	1B1	…	239R1	239B1
D6	C6	0R0	0B0	1R0	1B0	…	239R0	239B0
D5	C5	0G5		1G5		…	239G5	
D4	C4	0G4		1G4		…	239G4	
D3	C3	0G3		1G3		…	239G3	
D2	C2	0G2		1G2		…	239G2	
D1	C1	0G1		1G1		…	239G1	
D0	C0	0G0		1G0		…	239G0	

Table 45. 16-bit Parallel interface for 666 1/2 formats (MDT = 10)

count	0	1	2	3	4	…	479	480
D/CX	0	1	1	1	1	…	1	1
D15		0R5	0B1	1R5	1B1	…	239R5	239B1
D14		0R4	0B0	1R4	1B0	…	239R4	239B0
D13		0R3		1R3		…	239R3	
D12		0R2		1R2		…	239R2	
D11		0R1		1R1		…	239R1	
D10		0R0		1R0		…	239R0	
D9		0G5		1G5		…	239G5	
D8		0G4		1G4		…	239G4	
D7	C7	0G3		1G3		…	239G3	
D6	C6	0G2		1G2		…	239G2	
D5	C5	0G1		1G1		…	239G1	
D4	C4	0G0		1G0		…	239G0	
D3	C3	0B5		1B5		…	239B5	
D2	C2	0B4		1B4		…	239B4	
D1	C1	0B3		1B3		…	239B3	
D0	C0	0B2		1B2		…	239B2	

Table 46. 16-bit Parallel interface for 666 1/2 formats (MDT = 11)

count	0	1	2	3	4	…	479	480
D/CX	0	1	1	1	1	…	1	1
D15			0R3		1R3	…		239R3
D14			0R2		1R2	…		239R2
D13			0R1		1R1	…		239R1
D12			0R0		1R0	…		239R0
D11			0G5		1G5	…		239G5
D10			0G4		1G4	…		239G4
D9			0G3		1G3	…		239G3
D8			0G2		1G2	…		239G2
D7	C7		0G1		1G1	…		239G1
D6	C6		0G0		1G0	…		239G0
D5	C5		0B5		1B5	…		239B5
D4	C4		0B4		1B4	…		239B4
D3	C3		0B3		1B3	…		239B3
D2	C2		0B2		1B2	…		239B2
D1	C1	0R5	0B1	1R5	1B1	…	239R5	239B1
D0	C0	0R4	0B0	1R4	1B0	…	239R4	239B0

Table 47. 9-bit Parallel interface for 666 1/2 formats (MDT = 00)

count	0	1	2	3	4	…	479	480
D/CX	0	1	1	1	1	…	1	1
D8		0R5	0G2	1R5	1G2	…	239R5	239G2
D7	C7	0R4	0G1	1R4	1G1	…	239R4	239G1
D6	C6	0R3	0G0	1R3	1G0	…	239R3	239G0
D5	C5	0R2	0B5	1R2	1B5	…	239R2	239B5
D4	C4	0R1	0B4	1R1	1B4	…	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	239G5	239B1
D0	C0	0G3	0B0	1G3	1B0	…	239G4	239B0

Table 48. 9-bit Parallel interface for 666 1/3 formats (MDT = 01)

count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D8					…			
D7	C7				…			
D6	C6				…			
D5	C5	0R5	0G5	0B5	…	239R5	239G5	239B5
D4	C4	0R4	0G4	0B4	…	239R4	239G5	239B4
D3	C3	0R3	0G3	0B3	…	239R3	239G4	239B3
D2	C2	0R2	0G2	0B2	…	239R2	239G2	239B2
D1	C1	0R1	0G1	0B1	…	239R1	239G1	239B1
D0	C0	0R0	0G0	0B0	…	239R0	239G0	239B0

Table 49. 18-bit Parallel interface for 666 1/1 formats (MDT = 00)

count	0	1	2	…	239	240
D/CX	0	1	1	…	1	1
D17		0R5	1R5	…	238R5	239R5
D16		0R4	1R4	…	238R4	239R4
D15		0R3	1R3	…	238R3	239R3
D14		0R2	1R2	…	238R2	239R2
D13		0R1	1R1	…	238R1	239R1
D12		0R0	1R0	…	238R0	239R0
D11		0G5	1G5	…	238G5	239G5
D10		0G4	1G4	…	238G4	239G4
D9		0G3	1G3	…	238G3	239G3
D8		0G2	1G2	…	238G2	239G2
D7	C7	0G1	1G1	…	238G1	239G1
D6	C6	0G0	1G0	…	238G0	239G0
D5	C5	0B5	1B5	…	238B5	239B5
D4	C4	0B4	1B4	…	238B4	239B4
D3	C3	0B3	1B3	…	238B3	239B3
D2	C2	0B2	1B2	…	238B2	239B2
D1	C1	0B1	1B1	…	238B1	239B1
D0	C0	0B0	1B0	…	238B0	239B0

3.2.5. 65k Color Mode

For the display data to be accessed in 65k color mode, it is necessary that 65k color mode be selected (B2 to B0: 101) using COLMOD command before writing or reading to or from the display data RAM. In this mode, the display data per pixel comprised of 5 bits for R, 6 bits for G and 5 bits for B is written to the display data RAM. When all of the data for one pixel (RGB) is prepared in the internal register, the MCU writes the data to the display data RAM. When the display data is read from the display data RAM after RAMRD command is issued, 1 byte of dummy read cycle is needed. For detail information of data read format, refer to section 3.2.2.

Table 50. 24-bit Parallel interface type Ⅰ for 565 1/1 formats (MDT = 00)

count	0	1	2	…	239	240
D/CX	0	1	1	…	1	1
D23						
D22						
D21						
D20						
D19						
D18						
D17						
D16						
D15		0R4	1R4	…	238R4	239R4
D14		0R3	1R3	…	238R3	239R3
D13		0R2	1R2	…	238R2	239R2
D12		0R1	1R1	…	238R1	239R1
D11		0R0	1R0	…	238R0	239R0
D10		0G5	1G5	…	238G5	239G5
D9		0G4	1G4	…	238G4	239G4
D8		0G3	1G3	…	238G3	239G3
D7	C7	0G2	1G2	…	238G2	239G2
D6	C6	0G1	1G1	…	238G1	239G1
D5	C5	0G0	1G0	…	238G0	239G0
D4	C4	0B4	1B4	…	238B4	239B4
D3	C3	0B3	1B3	…	238B3	239B3
D2	C2	0B2	1B2	…	238B2	239B2
D1	C1	0B1	1B1	…	238B1	239B1
D0	C0	0B0	1B0	…	238B0	239B0

Table 51. 8-bit Parallel interface for 565 1/2 formats (MDT = 00)

count	0	1	2	3	4	…	359	480
D/CX	0	1	1	1	1	…	1	1
D7	C7	0R4	0G2	1R4	1G2	…	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	239G3	239B0

Table 52. 16-bit Parallel interface for 565 1/1 formats (MDT = 00)

count	0	1	2	…	239	240
D/CX	0	1	1	…	1	1
D15		0R4	1R4	…	238R4	239R4
D14		0R3	1R3	…	238R3	239R3
D13		0R2	1R2	…	238R2	239R2
D12		0R1	1R1	…	238R1	239R1
D11		0R0	1R0	…	238R0	239R0
D10		0G5	1G5	…	238G5	239G5
D9		0G4	1G4	…	238G4	239G4
D8		0G3	1G3	…	238G3	239G3
D7	C7	0G2	1G2	…	238G2	239G2
D6	C6	0G1	1G1	…	238G1	239G1
D5	C5	0G0	1G0	…	238G0	239G0
D4	C4	0B4	1B4	…	238B4	239B4
D3	C3	0B3	1B3	…	238B3	239B3
D2	C2	0B2	1B2	…	238B2	239B2
D1	C1	0B1	1B1	…	238B1	239B1
D0	C0	0B0	1B0	…	238B0	239B0

Table 53. 9-bit Parallel interface for 565 1/2 formats (MDT = 00)

count	0	1	2	3	4	…	359	480
D/CX	0	1	1	1	1	…	1	1
D8						…		
D7	C7	0R4	0G2	1R4	1G2	…	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0		239G3	239B0

Table 54. 18-bit Parallel interface for 565 1/1 formats (MDT = 00)

count	0	1	2	…	239	240
D/CX	0	1	1	…	1	1
D17						
D16						
D15		0R4	1R4	…	238R4	239R4
D14		0R3	1R3	…	238R3	239R3
D13		0R2	1R2	…	238R2	239R2
D12		0R1	1R1	…	238R1	239R1
D11		0R0	1R0	…	238R0	239R0
D10		0G5	1G5	…	238G5	239G5
D9		0G4	1G4	…	238G4	239G4
D8		0G3	1G3	…	238G3	239G3
D7	C7	0G2	1G2	…	238G2	239G2
D6	C6	0G1	1G1	…	238G1	239G1
D5	C5	0G0	1G0	…	238G0	239G0
D4	C4	0B4	1B4	…	238B4	239B4
D3	C3	0B3	1B3	…	238B3	239B3
D2	C2	0B2	1B2	…	238B2	239B2
D1	C1	0B1	1B1	…	238B1	239B1
D0	C0	0B0	1B0	…	238B0	239B0

3.3. RGB INTERFACE

3.3.1. Motion Picture Display

S6D04D1 incorporates RGB interface to display motion pictures and GRAM to store data for display.

The RGB interface is performed in synchronization with VSYNC, HSYNC, and DOTCLK.

In the period between the completion of displaying one frame data and the next VSYNC signal, the display status will remain in front porch period.

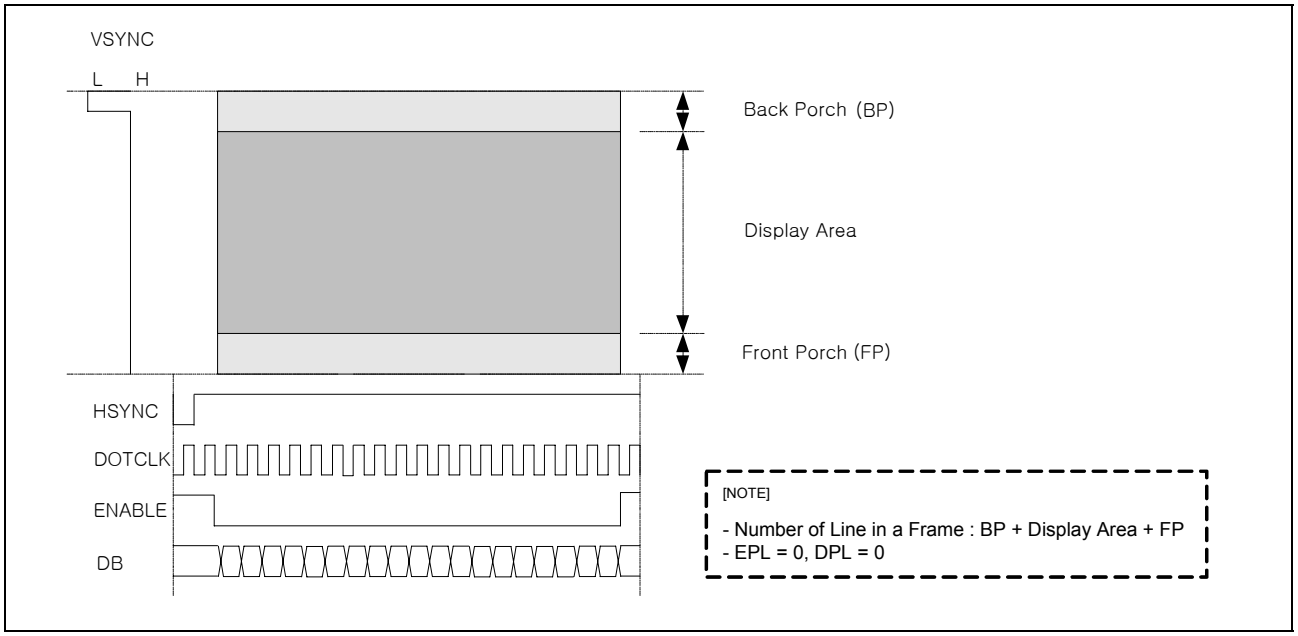


Figure 56. RGB interface

Note. For RGB interface, VSYNC, HSYNC, DOTCLK should be supplied at much higher resolution than that of panel.

There are five timing conditions for RGB Interface that is determined according to RIM, COLMOD and each condition is described below.

Table 55. RGB Interface mode selection

RIM	COLMOD[6:4]	RGB Interface Mode
0	111 (16M color)	24- bit RGB interface (1 transfer/pixel)
	110 (262k color)	18- bit RGB interface (1 transfer/pixel)
	101 (65k color)	16- bit RGB interface (1 transfer/pixel)
1	111 (16M color)	8- bit RGB interface (3 transfer/pixel)
	110 (262k color)	6- bit RGB interface (3 transfer/pixel)

3.3.2. 24-bit RGB Interface

3.3.2.1. Bit Assignment

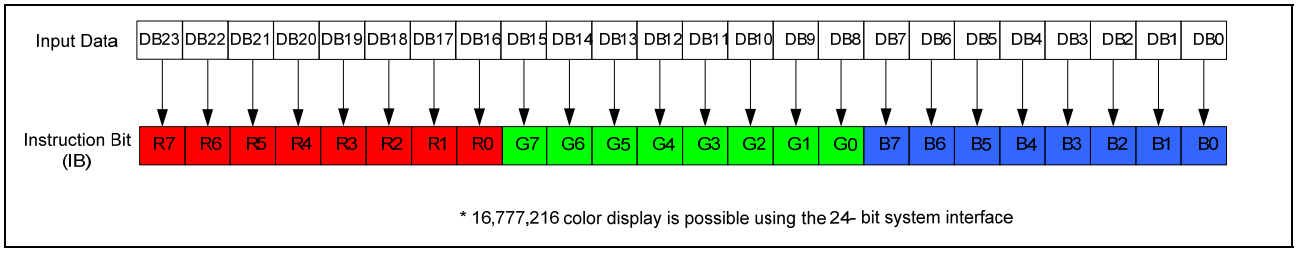


Figure 57. Bit assignment of GRAM data on 24bit RGB interface

3.3.2.2. Timing Diagram

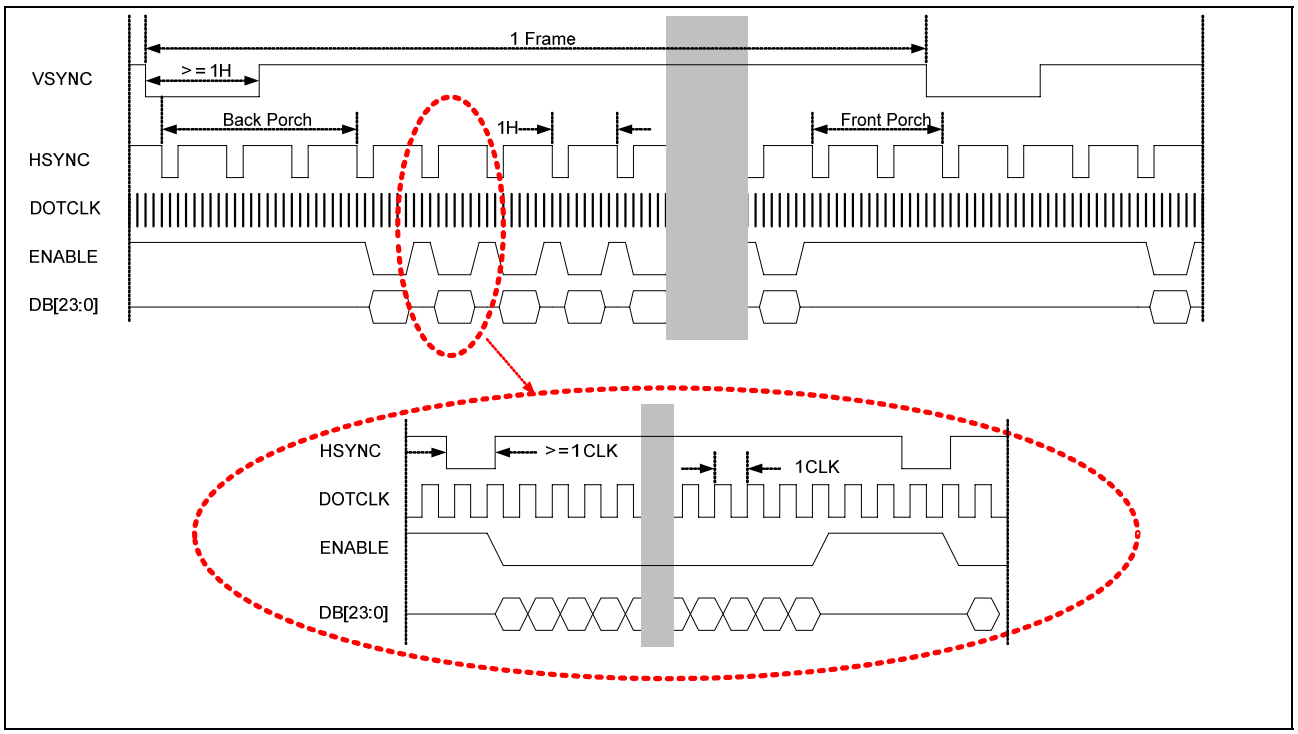


Figure 58. Timing diagram of 24bit RGB interface

Note. The number of DOTCLK for 1H period must be bigger than 260.

3.3.3. 18-bit RGB Interface

3.3.3.1. Bit Assignment

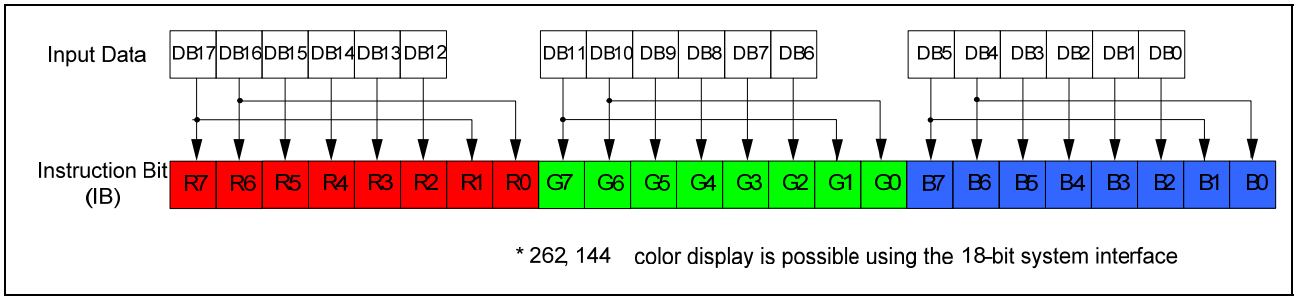


Figure 59. Bit assignment of GRAM data on 18bit RGB interface

3.3.3.2. Timing Diagram

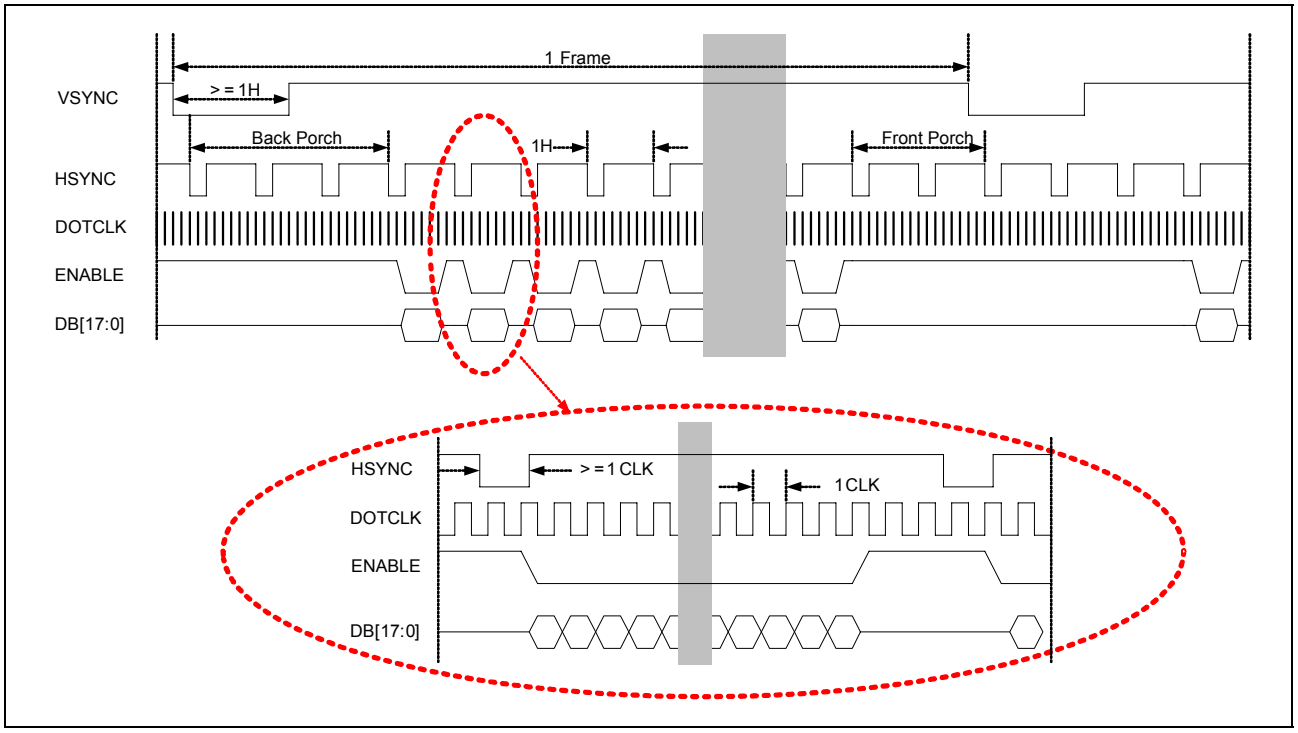


Figure 60. Timing diagram of 18bit RGB interface

Note. The number of DOTCLK for 1H period must be bigger than 260.

3.3.4. 16-bit RGB Interface

3.3.4.1. Bit Assignment

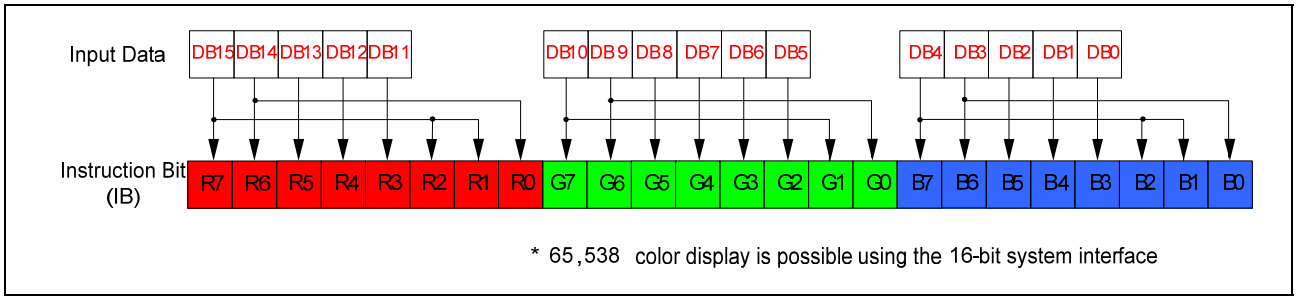


Figure 61. Bit assignment of GRAM data on 16bit RGB interface

3.3.4.2. Timing Diagram

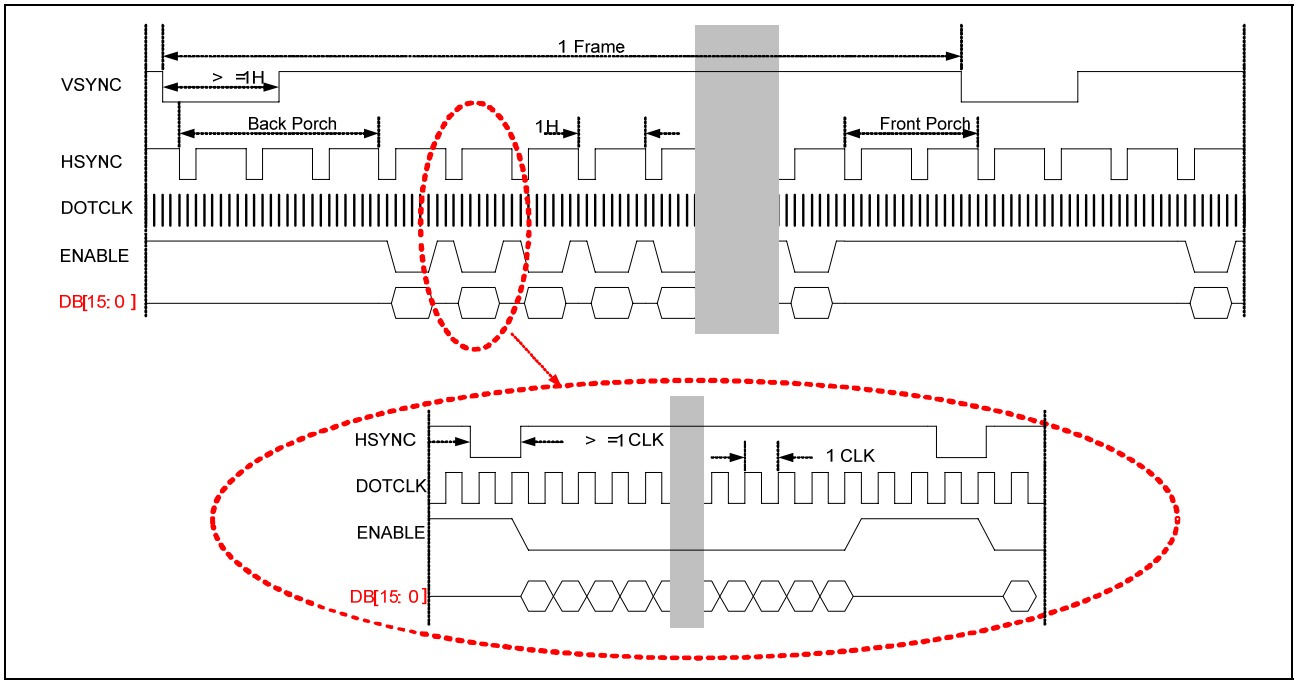


Figure 62. Timing diagram of 16bit RGB interface

Note. The number of DOTCLK for 1H period must be bigger than 260.

3.3.5. 8-bit RGB Interface

In order to transfer data on 8bit RGB Interface there should be three transfers.

3.3.5.1. Bit Assignment

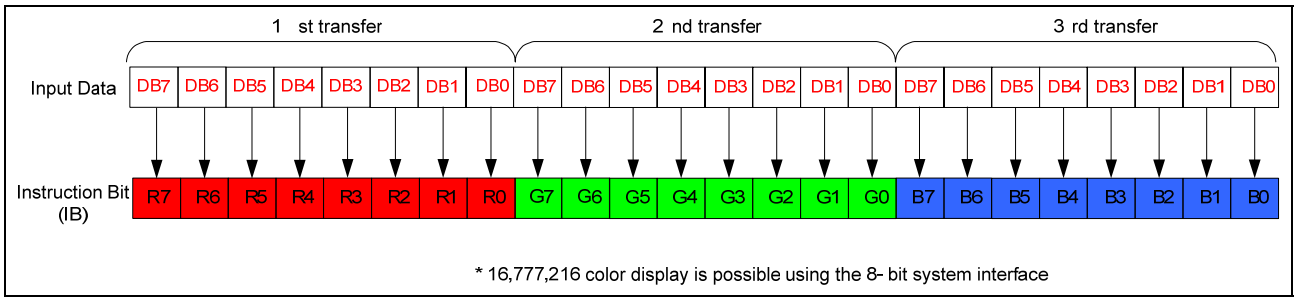


Figure 63. Bit assignment of GRAM data on 8bit RGB interface

3.3.5.2. Timing Diagram

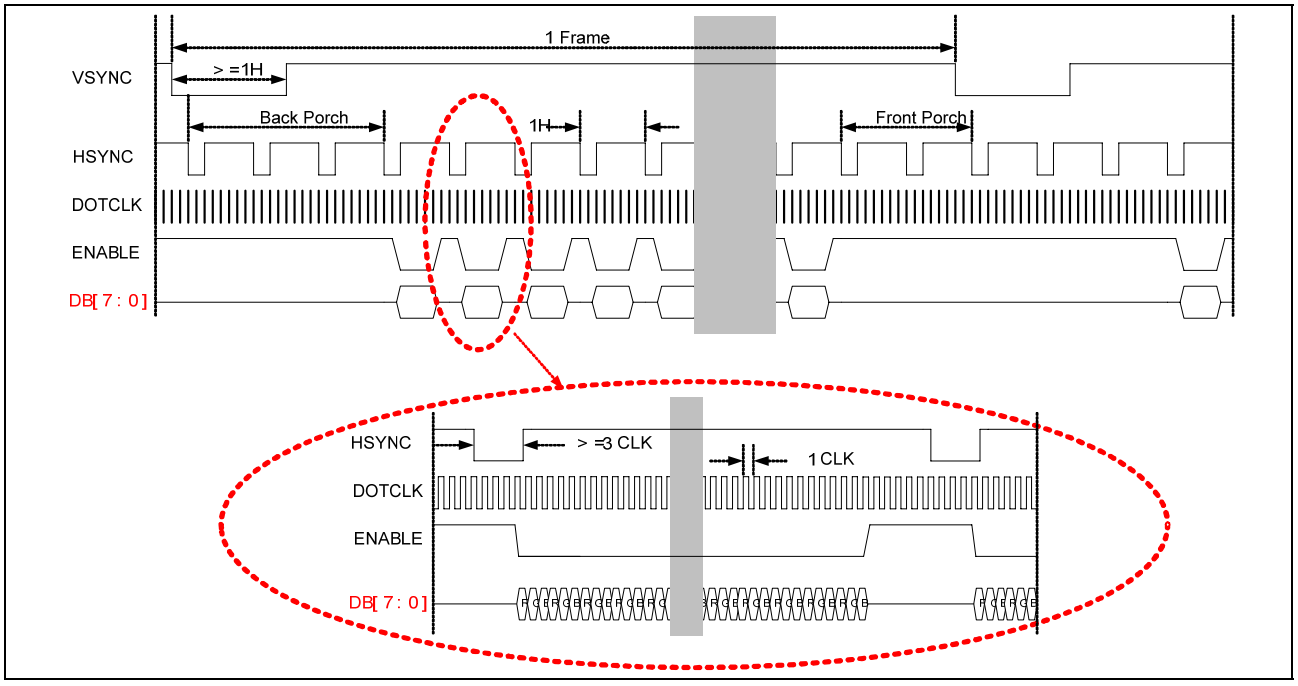


Figure 64. Timing diagram of 8-bit RGB interface

Note1. Three clocks are regarded as one clock for transfer when data is transferred in 8-bit interface.

VSYNC, HSYNC, ENABLE, DOTCLK, and DB[7:0] should be transferred in units of three clocks.

Note2. The number of DOTCLK for 1H period must be bigger than (260x3).

3.3.5.3. Transfer Synchronization

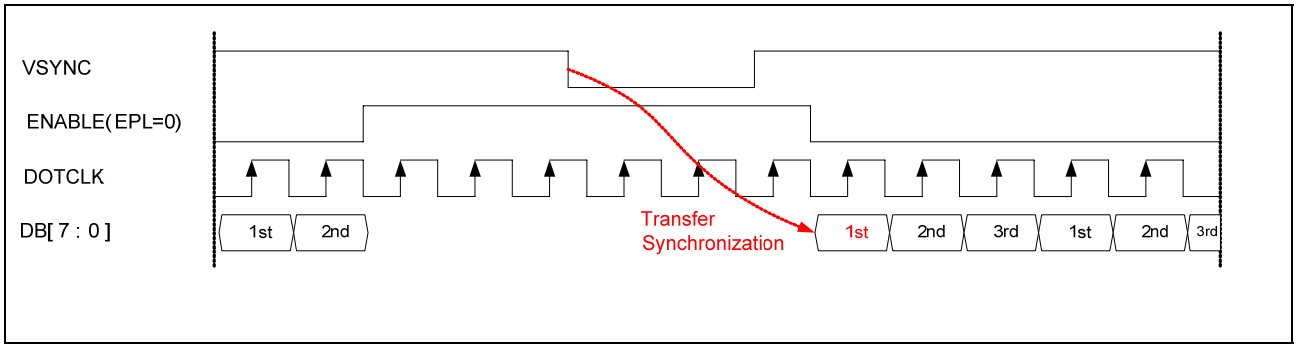


Figure 65. Transfer synchronization function in 8-bit RGB interface mode

Note. The figure above shows Transfer Synchronization functions for 8bit RGB Interface. S6D04D1 has a transfer counter internally to count 1st, 2nd and 3rd data transfer of 8bit RGB Interface. The transfer counter is reset on the falling edge of VSYNC and enters the 1st data transmission state. Transfer mismatch can be corrected at every VSYNC signal assertion. In this method, when data is consecutively transferred in for displaying motion pictures, the effect of transfer mismatch will be reduced and recovered by normal operation. The display is operated in units of three DOTCLKs. When DOTCLK is not input in units of pixels, clock mismatch occurs and the frame, which is operated, and the next frame are not displayed correctly.

3.3.6. 6-bit RGB Interface

In order to transfer data on 6bit RGB Interface there should be three transfers.

3.3.6.1. Bit Assignment

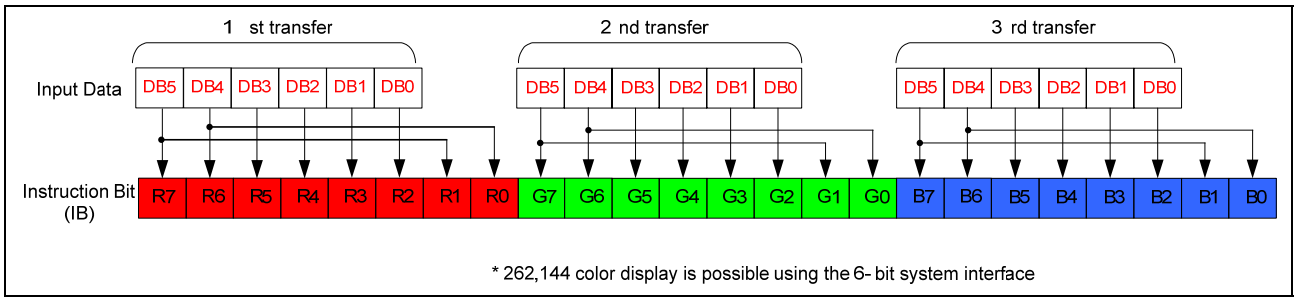


Figure 66. Bit assignment of GRAM data on 6bit RGB interface

3.3.6.2. Timing Diagram

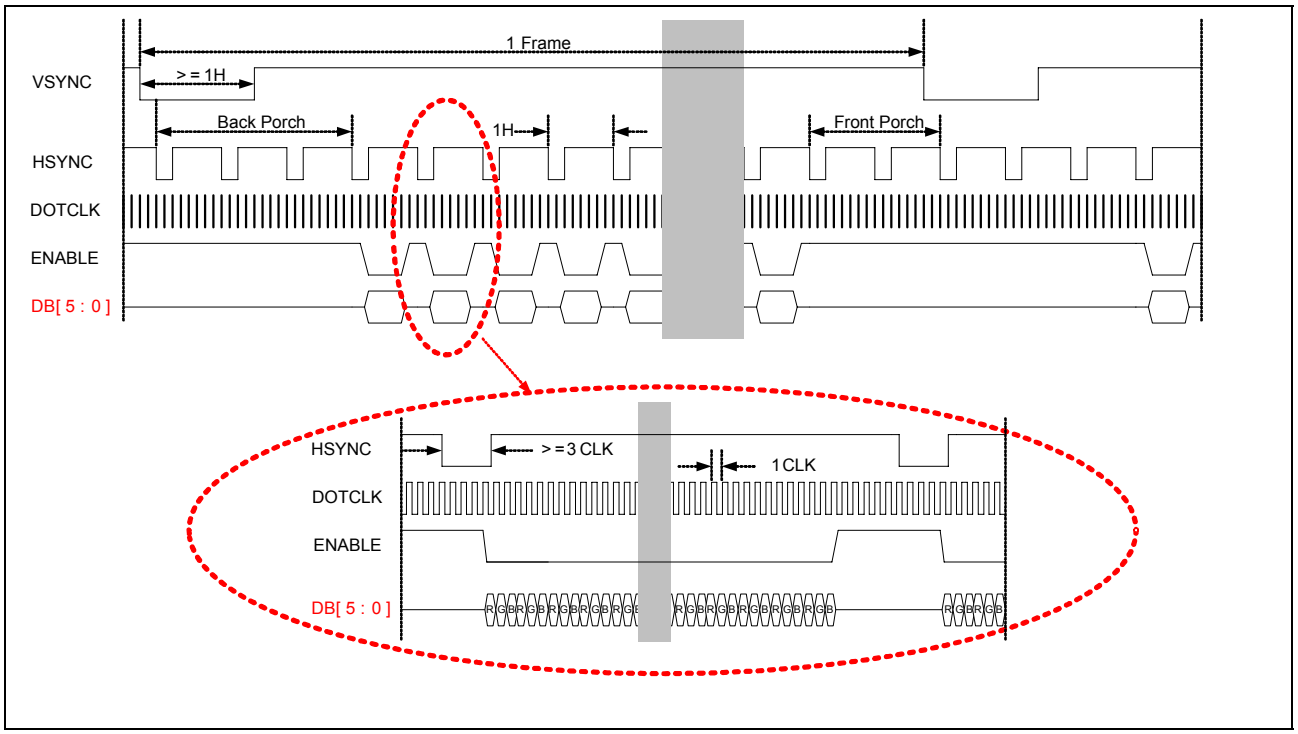


Figure 67. Timing diagram of 6bit RGB interface

Note1. Three clocks are regarded as one clock for transfer when data is transferred in 6-bit interface.

VSYNC, HSYNC, ENABLE, DOTCLK, and DB[5:0] should be transferred in units of three clocks.

Note2. The number of DOTCLK for 1H period must be bigger than (260x3).

3.3.6.3. Transfer Synchronization

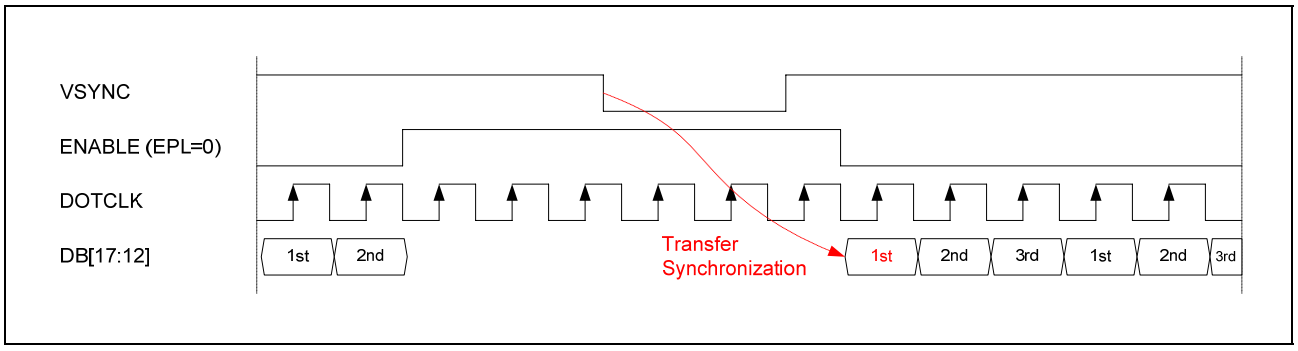


Figure 68. Transfer synchronization function in 6-bit RGB interface mode

Note. The figure above shows Transfer Synchronization functions for 6bit RGB Interface. S6D04D1 has a transfer counter internally to count 1st, 2nd and 3rd data transfer of 6bit RGB Interface. The transfer counter is reset on the falling edge of VSYNC and enters the 1st data transmission state. Transfer mismatch can be corrected at every VSYNC signal assertion. In this method, when data is consecutively transferred in for displaying motion pictures, the effect of transfer mismatch will be reduced and recovered by normal operation. The display is operated in units of three DOTCLKs. When DOTCLK is not input in units of pixels, clock mismatch occurs and the frame, which is operated, and the next frame are not displayed correctly.

3.3.7. Transition Sequences between Display Modes

Transitions between Internal Clock Operation mode and External Clock Operation mode should follow the mode transition sequence shown below.

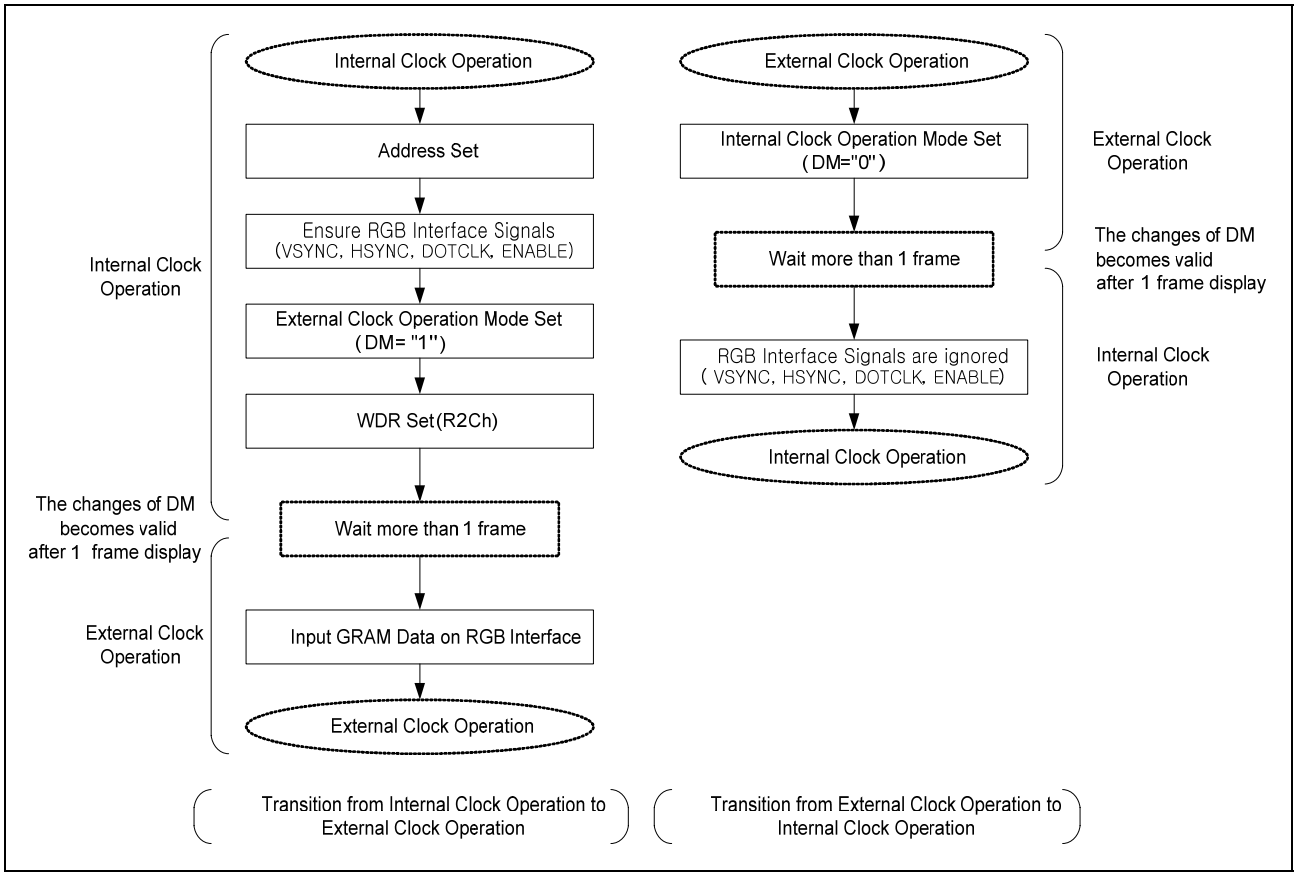


Figure 69. Transition between Internal clock operation mode and external clock operation mode

3.4. VSYNC INTERFACE

The S6D04D1 incorporates VSYNC interface as external interface for motion picture display.

When the VSYNC interface is selected, internal operation is normally synchronized with internal clock except operation related to frame synchronization: It is synchronized with the VSYNC signal. The data for display are written to GRAM via conventional system interface. There are some limitations on the timing and methods for writing to GRAM in VSYNC interface.

The S6D04D1 incorporates VSYNC interface, which enables motion pictures to be displayed with only the conventional system interface and the frame synchronization signal (VSYNC). This interface requires minimal changes from the conventional system to display motion pictures.

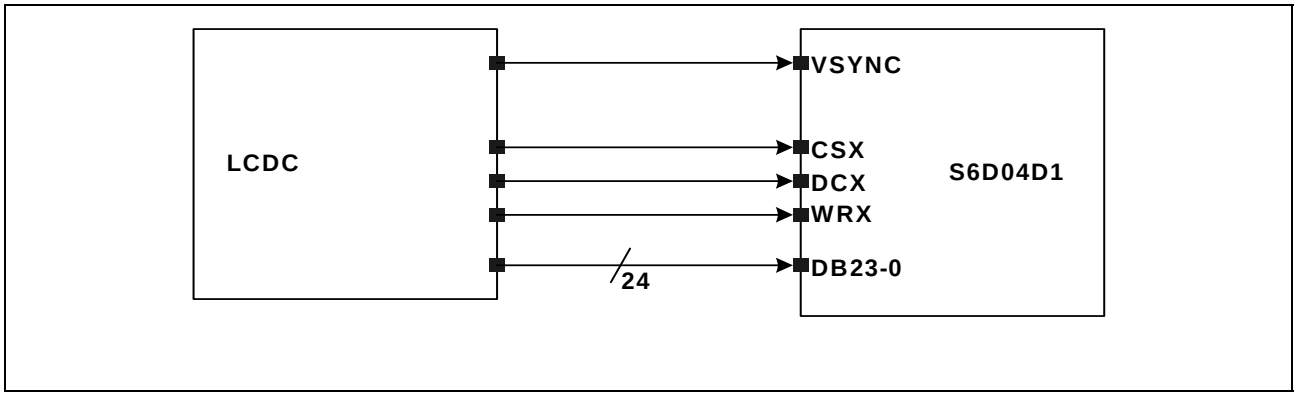


Figure 70. VSYNC interface (example: 24bit interface)

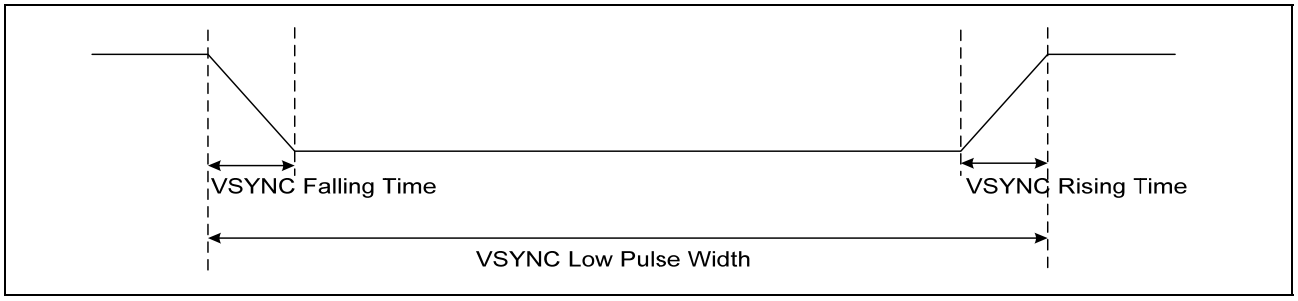


Figure 71. VSYNC signal timing

Table 56. AC characteristics of VSYNC signal

Parameter	min	max	unit
VSYNC Falling Time	-	15	ns
VSYNC Rising Time	-	15	ns
VSYNC Low Pulse Width	2-Horizontal Display Time	-	-

When VSM=”1”, VSYNC interface is available. In this interface the internal display operation is synchronized with VSYNC. Data for display is written to RAM via the system interface with higher speed than for internal display operation. This method enables flicker-free display of motion pictures with the conventional interface.

Display operation can be achieved by using the internal clock generated by the internal oscillator and the VSYNC input. Because all the data for display is written to RAM, only the data to be rewritten is transferred. This method reduces the amount of data transferred during motion picture display operation.

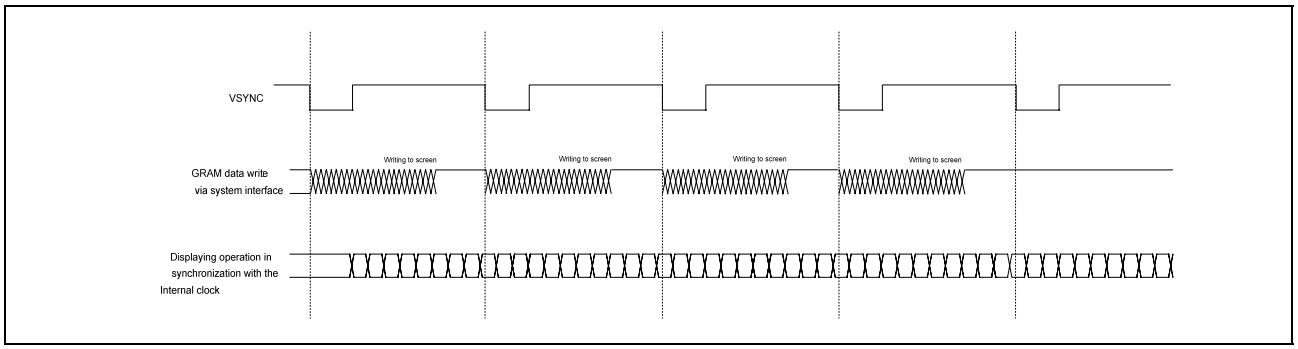


Figure 72. Motion picture data transfer via VSYNC interface

VSYNC interface requires taking the minimum speed for RAM writing via the system interface and the frequency of the internal clock into consideration. RAM writing should be performed with higher speed than the result obtained from the calculation shown below.

Internal clock frequency (fosc) [Hz] = 13.9MHz

= Frame freq. (Display raster-row (432) + Front porch (VFP) + Back porch (VBP)) X RTN X CRTN X Fluctuation

Minimum speed for RAM writing [Hz]

> 240 X Display raster-row (432) / {((Back porch (VBP) + Display raster-row (432) – Margin) X RTN X CRTN) / 13.9MHz}

Note. when RAM writing does not start immediately after the falling edge of VSYNC, the time between the falling edge of VSYNC and the RAM writing start timing must also be considered.

An example is shown below.

Example

Display size	240RGB X 432 raster-rows
Back/Front porch	14 lines/2 lines (VBP=0001101/VFP=0000010)
OSC Frequency	13.9MHz fix
RTN , CRTN	22

Internal clock frequency is 13.9MHz. It is a fixed value.

Minimum speed for RAM writing [Hz] > 240 X 432 / {((14 + 432 – 2) lines X 22 X 22 clock) / 13.9MHz} = 6.71MHz

Note1. In this case RAM writing starts immediately after the falling edge of VSYNC.

Note2. The margin for display raster-row should be two raster-rows or more at the completion of RAM writing for one frame.

Therefore, when RAM writing starting immediately after the falling edge of VSYNC is performed at 6.71 MHz or more, the data for display can be rewritten before display operation starts. This means that flicker-free display operation is achieved.

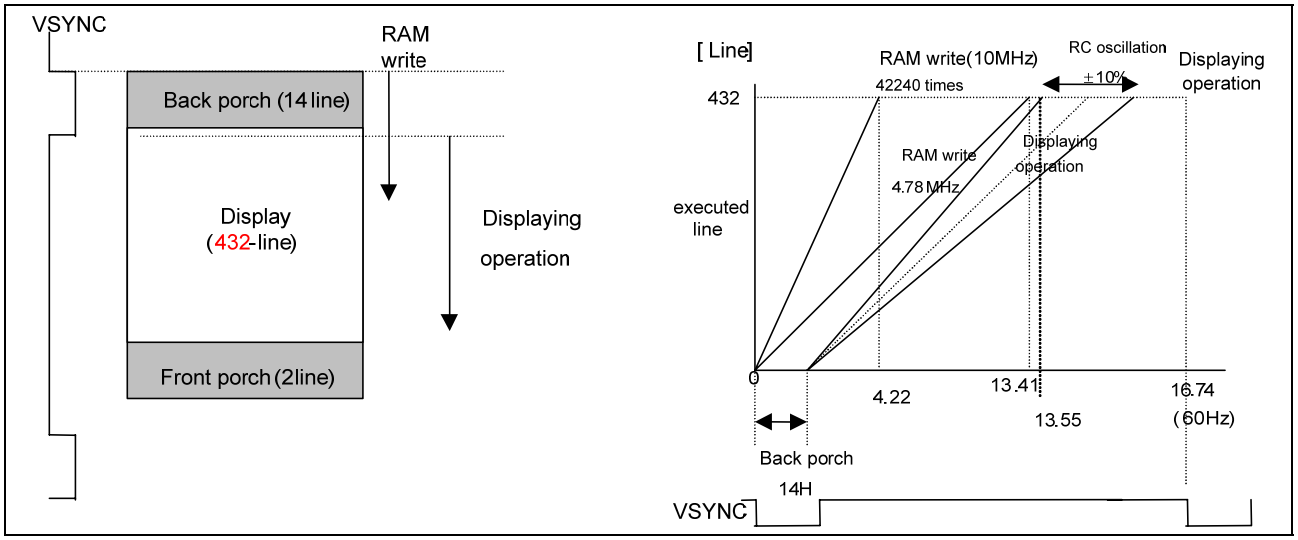


Figure 73. Operation for VSYNC interface

3.4.1. Usage on VSYNC interface

1. The Example above is a calculated value. Please keep in mind that a margin for these factors is also needed. Because the variation of the internal oscillator requires a consideration.

2. The Example above is a calculated value of rewriting the whole screen. A limitation of the motion picture area generates a margin for the RAM write speed.

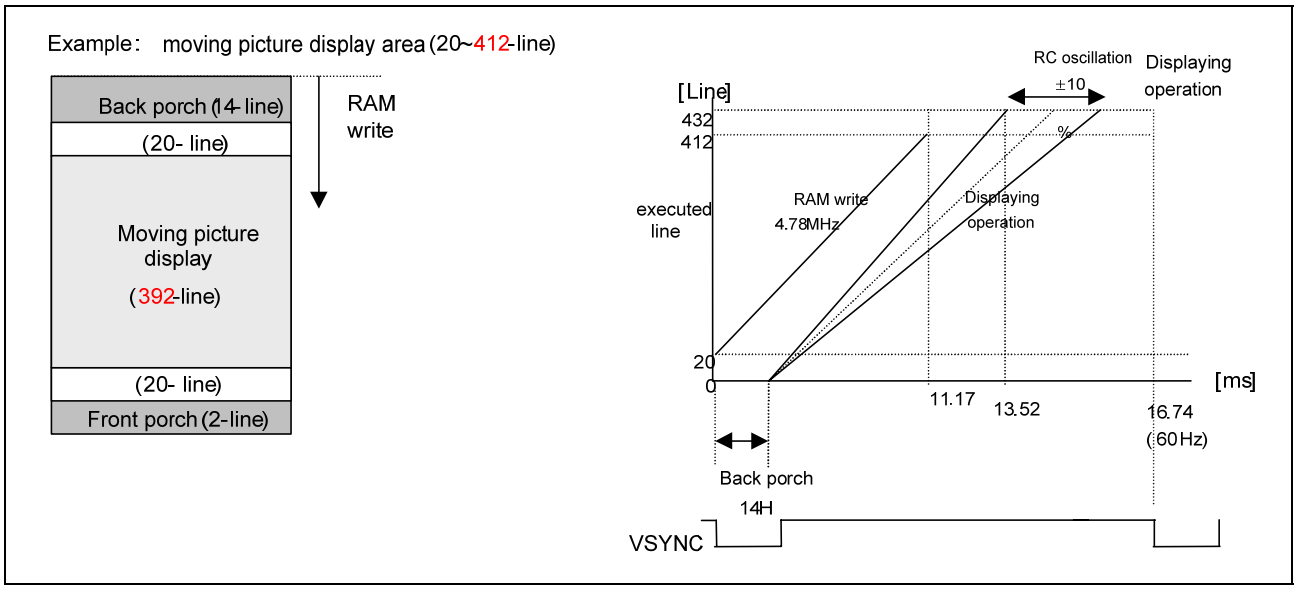


Figure 74. Limitation of motion picture area

3. During the period between the completion of displaying one frame data and the next VSYNC signal, the display will remain front porch period.

4. Transition between the internal operating clock mode (VSM="1") and VSYNC interface mode will be valid after the completion of the screen, which is displayed when the instruction is set.

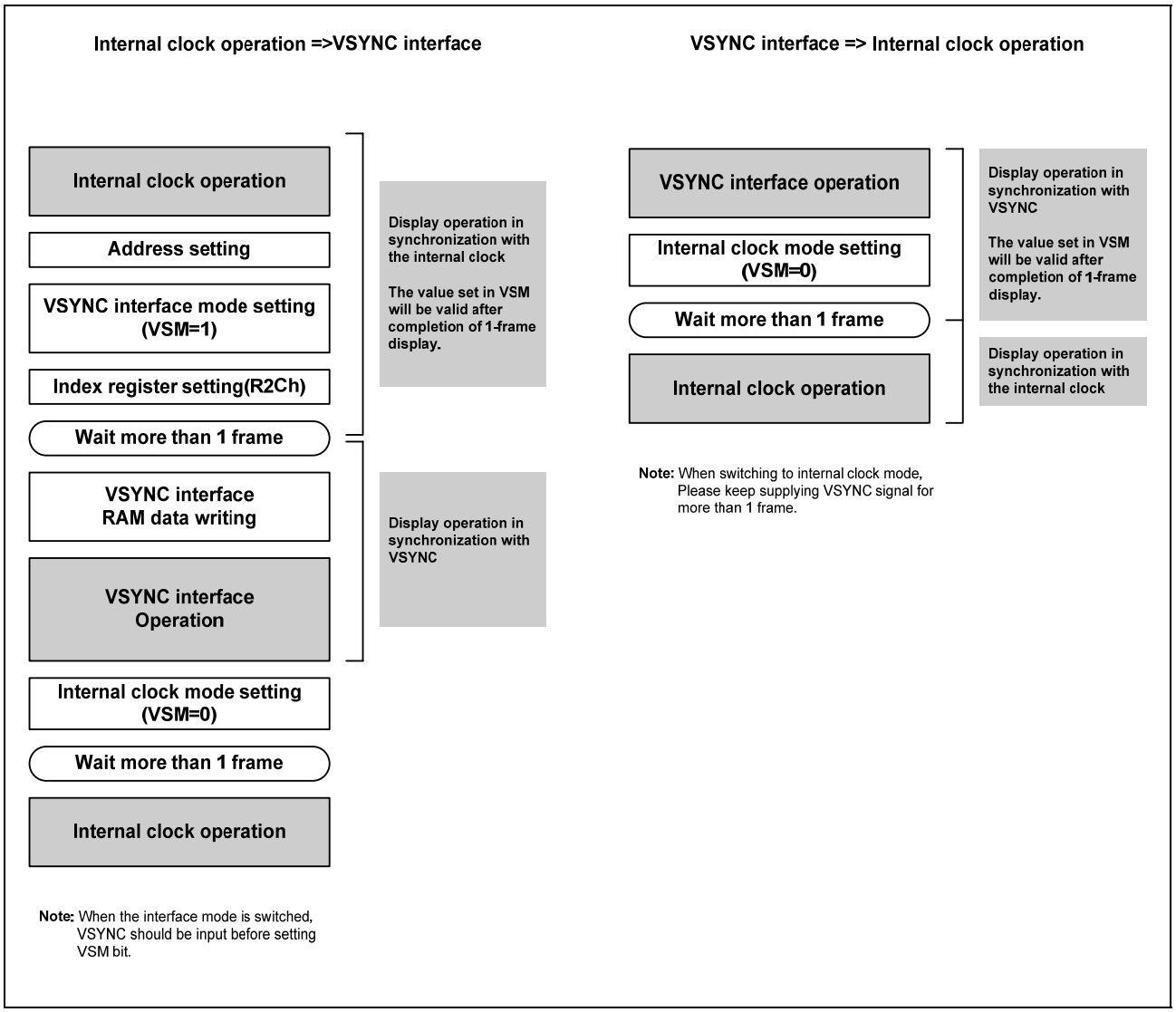


Figure 75. Transition between the internal operating clock mode and VSYNC interface mode

5. Partial display and vertical scroll functions are not available on VSYNC interface mode.

6. The VSYNC interface is performed by the method above.

3.5. MDDI(MOBILE DISPLAY DIGITAL INTERFACE)

3.5.1. Introduction to MDDI

The S6D04D1 supports MDDI(Mobile Display Digital Interface). The pjysical layer of MDDI is based on a high-speed, differential serial interface. Both command and image data transfer can be achieved with MDDI.

MDDI host & Client are linked by Data and STB line. Through Data line, either command or image data is transferred from MDDI host to MDDI client, and vice versa. Data is transferred by packet unit.

Through STB line, strobe signal is transferred. When the link is in "FORWORD direction", data is transferred from host to client; in "REVERSE direction", client transfers data to MDDI host.

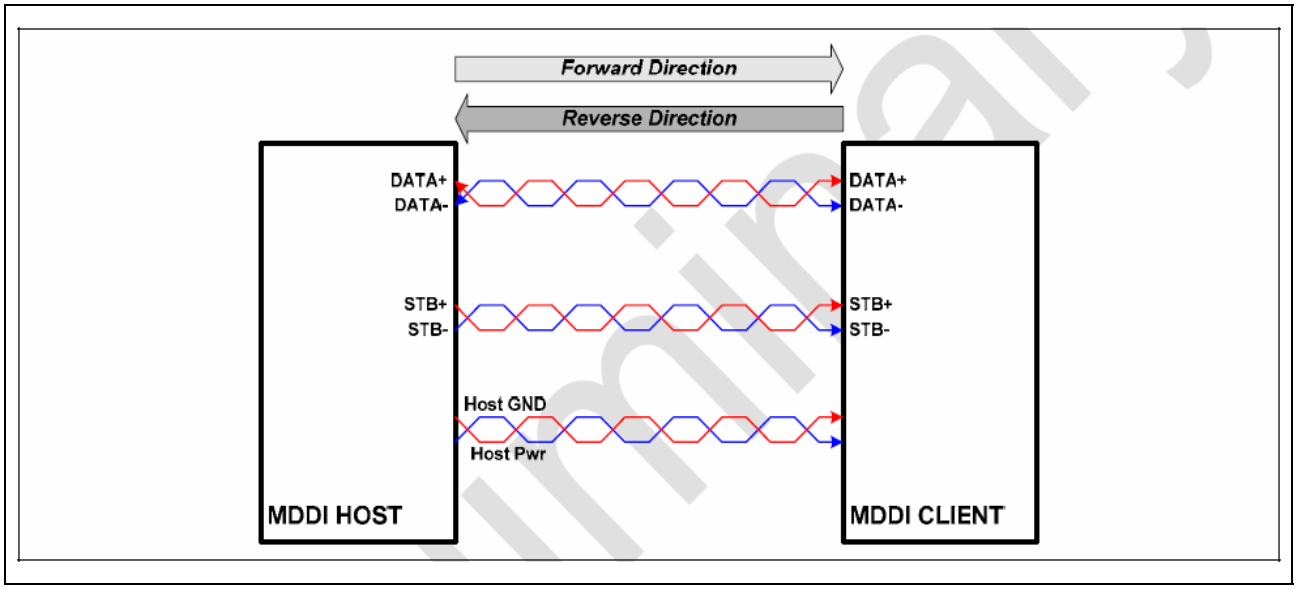


Figure 76. Physical connection of MDDI host and client

3.5.2. Data-STB Encoding

Data is encoded using a DATA-STB method. Data signal is bi-directional over a pair of differential cable while STB signal in uni-directional over a pair of differential cable driven by a host as shown in following Figure.Figure below illustrates how the data sequence “11_1000_1011” is transmitted using DATA-STB encoding.

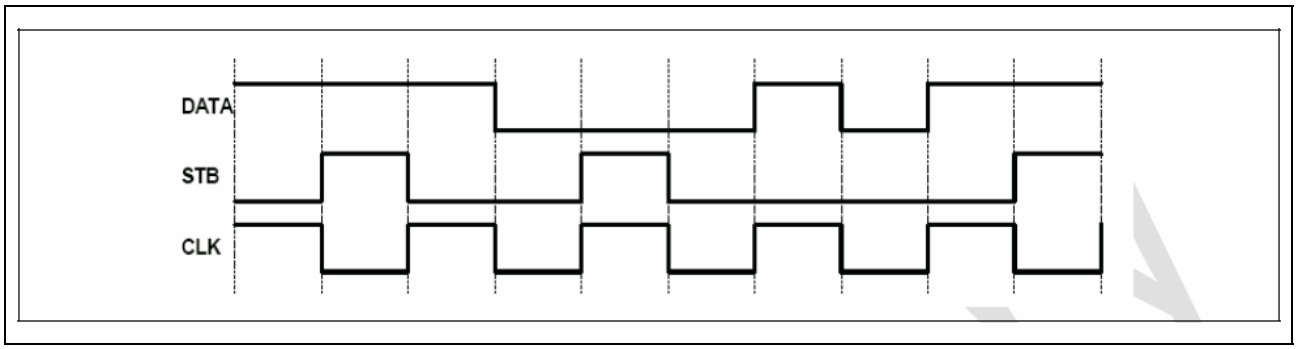


Figure 77. Data-STB encoding

The Following figure shows a sample circuit to generate DATA and STB from input data, and then recover the input data from DATA and STB.

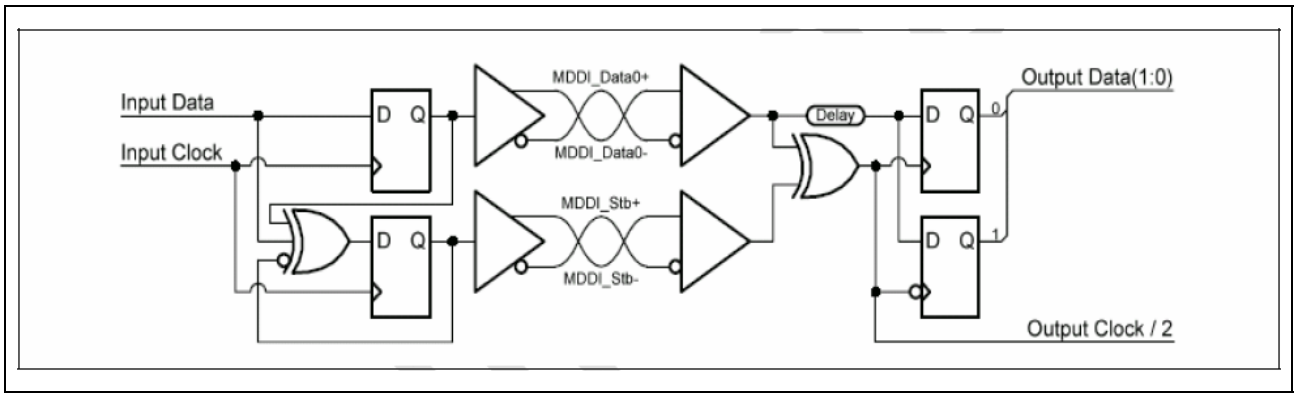


Figure 78. Data / STB generation & recovery circuit

3.5.3. MDDI Data & STB

The Data(MDP/MDN) and STB(MSP/MSN) signals are always operated in a differential mode to maximize noise immunity. Each differential pair is parallel-terminated with the characteristic impedance of the cable. All parallel-terminations are in the client device. Figure below illustrates the configuration of the drivers, recivers, and terminations.

The driver of each signal pair has a differential current output. While receving MDDI packets. The MDDI_DATA and MDDI_STB pairs use a conventional differential receiver with a differencial voltage threshold of zero volts. In the hibernation state, the driver outputs are disabled and the parallel termination resistors pull the differential voltage on each signal pair to zero volts. During hibernation, a special receiver on the MDDI_DATA paris has an offset input differential voltage threshold of positive 125mV, which cause the hibernation line reciver interpret the un-driven signal pair as logic-zero level.

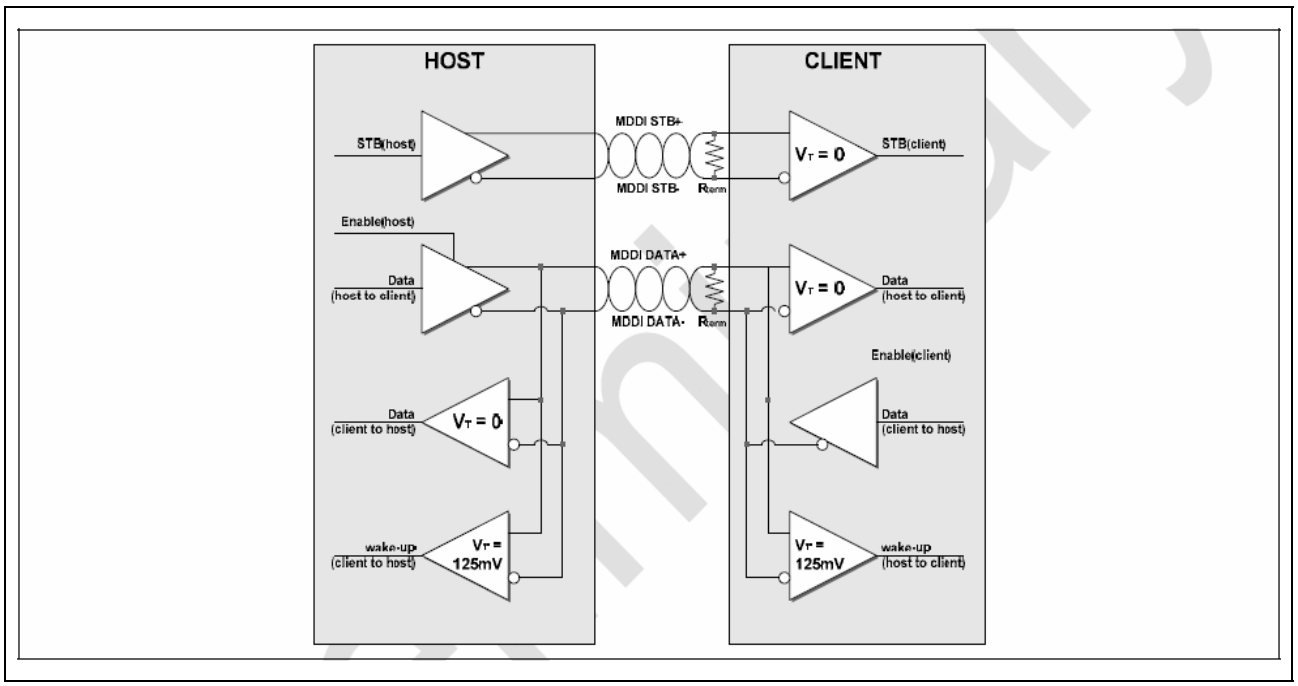


Figure 79. Differential connection between host and client

3.5.4. MDDI Packet

MDDI transfer data in a packet format. MDDI host can generate and send packets.

In S6D04D1, several packet format are supported. Packets are transferred from MDDI host to client(forward direction); but reverse encapsulation packet is transferred from MDDI client to host(reverce direction).

A number of packets, started by sub-frame header packet, construct 1 sub frame.

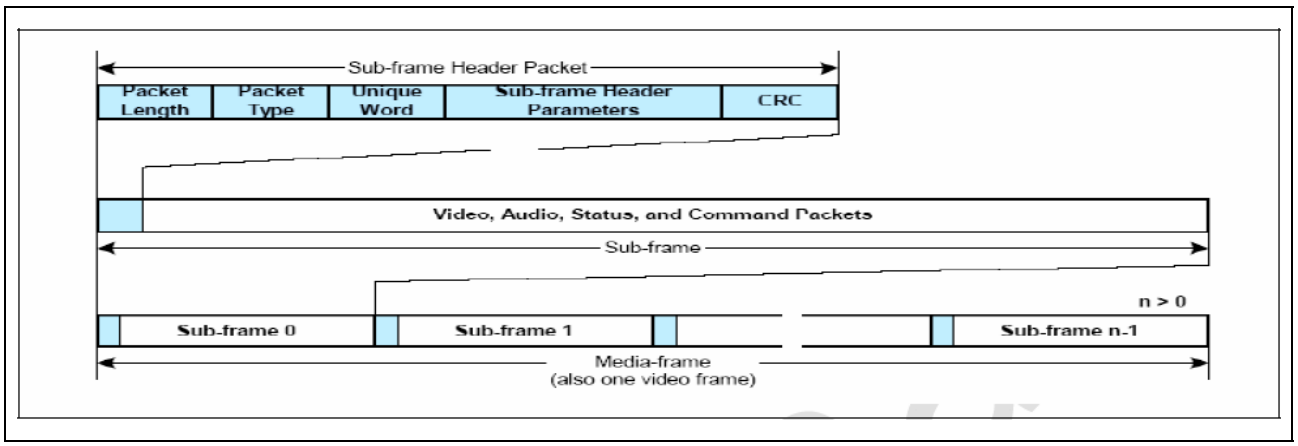


Figure 80. MDDI packet structure

Refer to MDDI packet structure, sub-frame header packet is placed in front of a sub-frame, and some sub-frame construct media-frame together.

Table 57. Types of packets which are supported in S6D04D1.

Packet	Function	Direction
Sub-frame header packet	Header of each sub frame	Forward
Register access packet	Register setting	Forward
Video stream packet	Video data transfer	Forward
Filler packet	Fill empty packet space	Forward
Reverse link encapsulation packet	Reverse data packet	Reverse
Round-trip delay measurement packet	Host->client->host delay check	Forward / Reverse
Client capability packet	Capability of client check	Reverse
Client request and status packet	Information about client status	Reverse
Link shutdown packet	End of frame	Forward

Sub-Frame header packet

packet length	packet type = 3bffh	unique word = 005ah	reserved1	sub-frame length	protocol version	sub-frame conut	media frame count	CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	2 bytes	4 bytes	2 bytes

packet length : packet length not including packet length block
packet type : packet type (sub-frame header packet is 3bffh)
unique word : Identify "This packet is sub-frame header packet"
reserved1 : not used (set zero)
sub-frame length : specifies number of bytes per sub-frame
protocol version : set all zero
sub-frame count : specifies number of sub-frame header packets
mddi frame count : specifies number of media frames
CRC : error check

Figure 81. Sub-frame header packet structure

Register access packet

packet length	packet type = 146	bClient ID	Read / Write Info	Register Address	Paramter CRC	Register Data List	Register Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	Packet Length -14byte	2 bytes

packet length : packet length not including packet length block
packet type : packet type (Register Access packet is 146 (decimal))
bClient ID : set to all zero
Read / Write Info : to write register value , bits [15:14] = " 00 "
to request register value , bits[15: 14] = " 10 "
bits [13 :0] refer to VESA SPEC
Register Address : Register address is written here
Parameter CRC : To check error from packet length to register address
Register Data List : A list of 4byte register data values to be written to LDI
CRC : To error check register data list
※ Basis of Register Data List is 4-byte unit. Therefore, When Register Parameter is not Multiply of 4, Remainder bits must fill by 0

000000FFh
Register Data list

Figure 82. Register access packet structure

Video Stream Packet

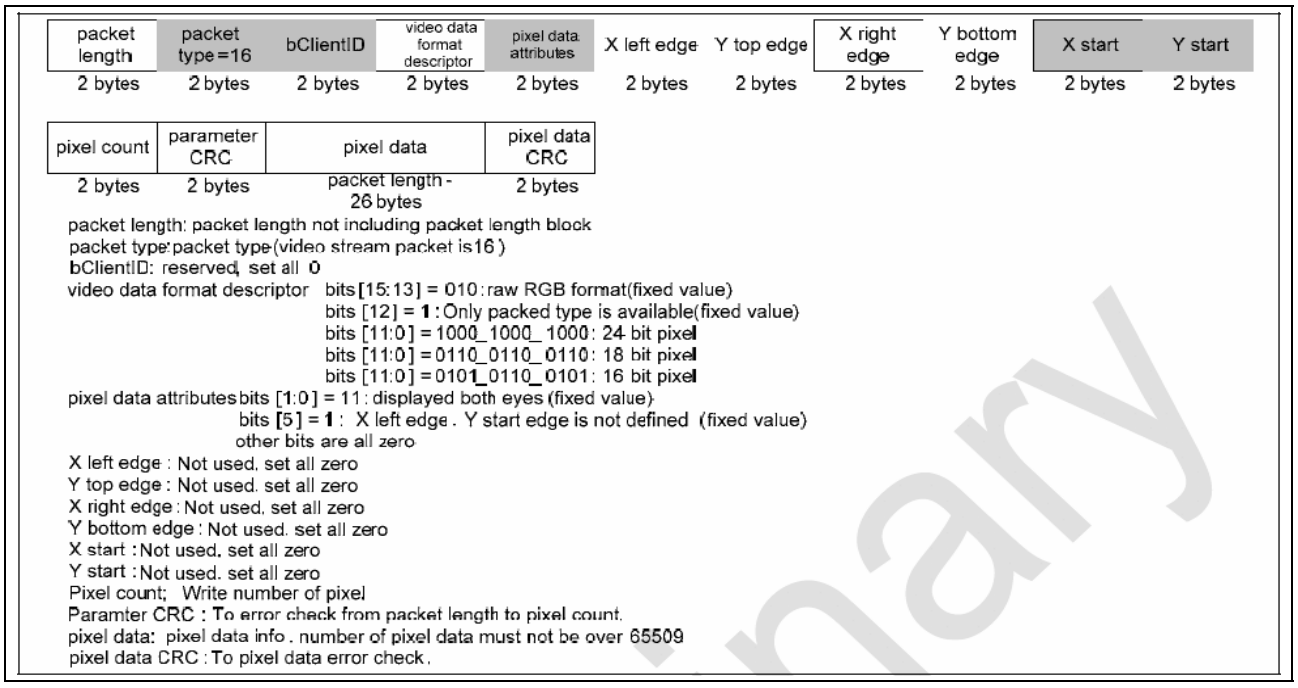


Figure 83. Video system packet structure

Filler packet

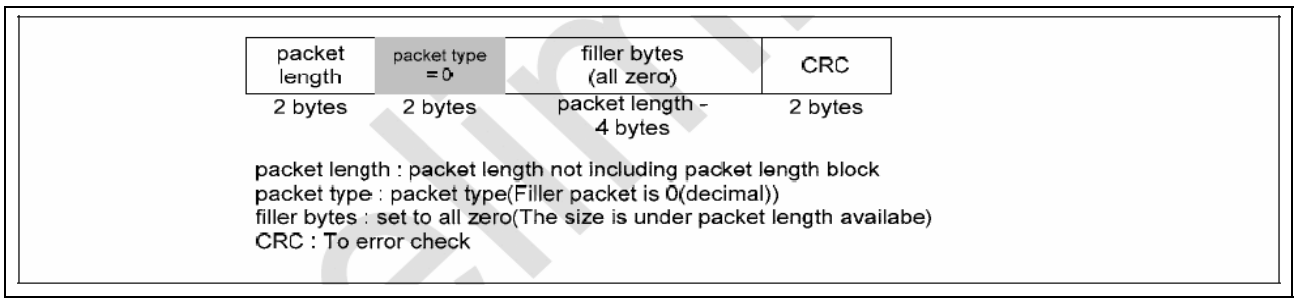


Figure 84. Filler packet structure

Link shutdown packet

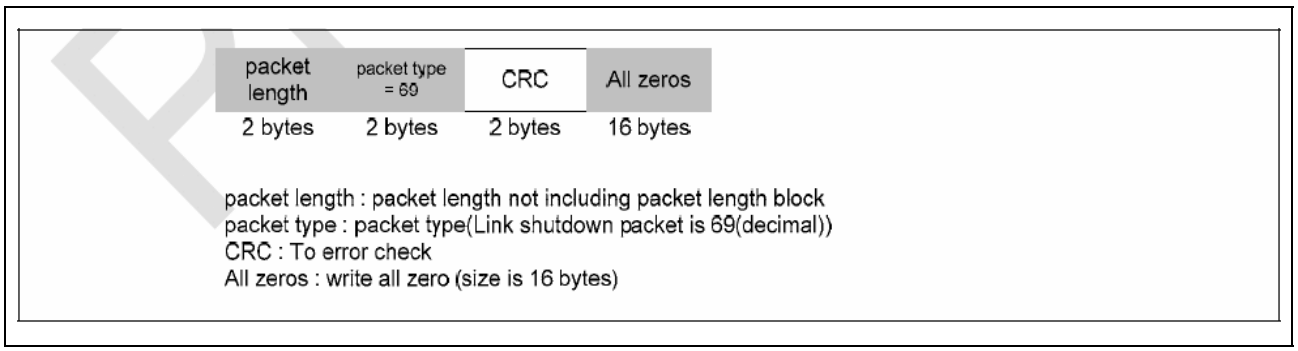


Figure 85. Link shutdown packet structure

: fixed value

For more information about MDDI packet, refer to VESA MDDI spec.

3.5.5. Panel Control

S6D04D1 supports video stream packet for memory write and register access packet for register write/read. Foll owings are some examples of memory and register write/read sequence.

3.5.5.1. Writing Video Data to Memory Sequence

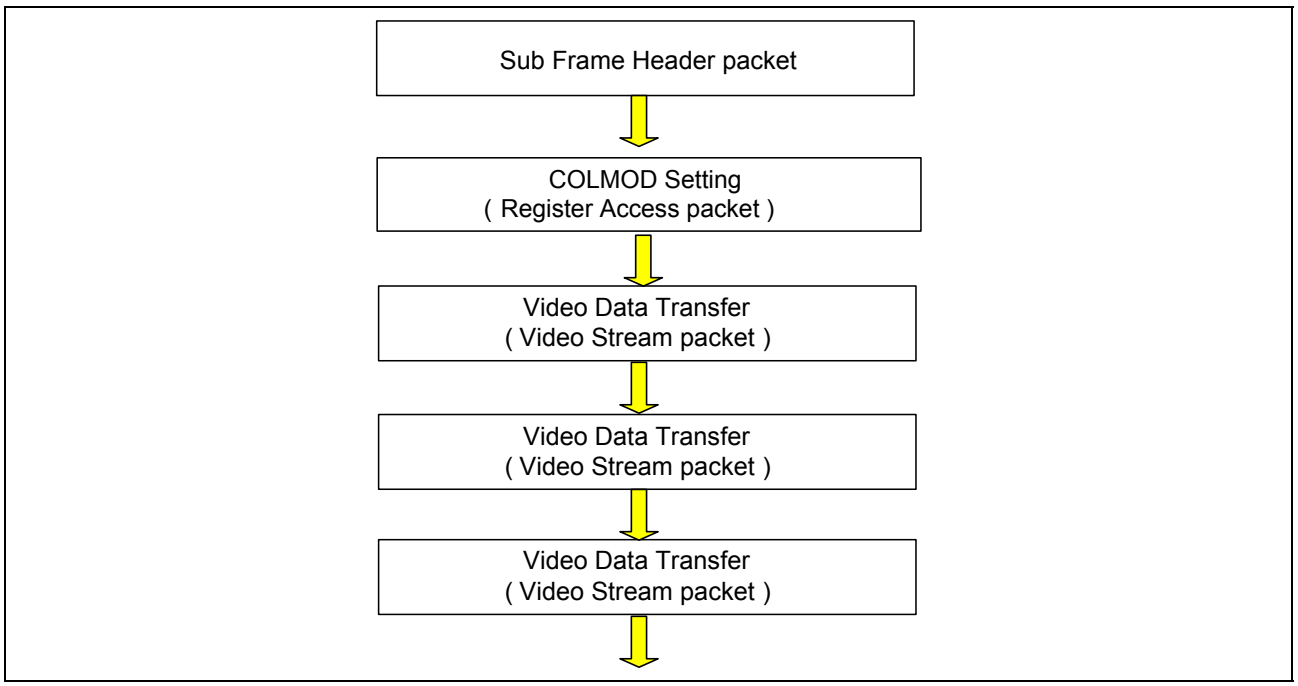


Figure 86. Writing video data to memory sequence

Table 58. COLMOD setting in MDDI

Video data format descriptor[11:0]	COLMOD[2:0]
1000_1000_1000	111 (16M color)
0110_0110_0110	110 (262k color)
0101_0110_0101	101 (65k color)

Note: If user want to transfer 888(24bit) video data, Set COLMOD[2:0]=”111” prior to Video Stream Packet

3.5.5.2. Writing Register Sequence

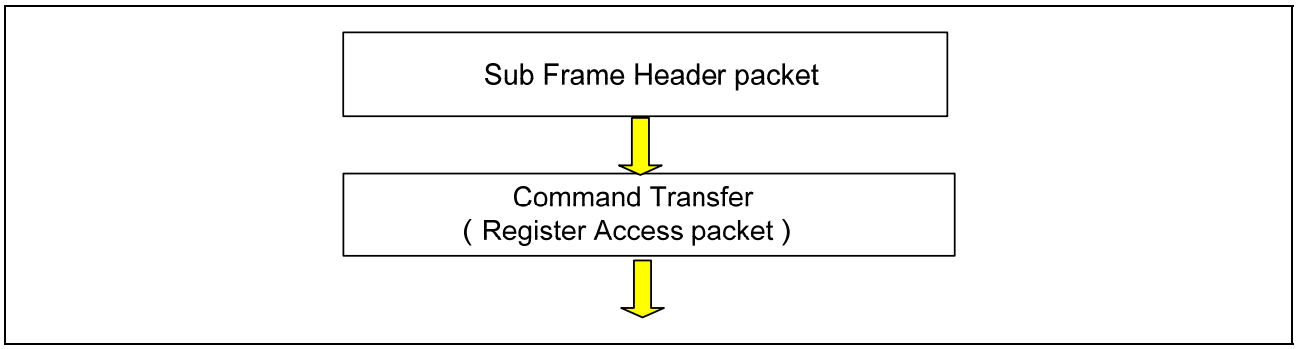


Figure 87. Writing register sequence

3.5.5.3. Reading Video Data from Memory Sequence

In order to read a pixel data from memory(readable one pixel only), the following sequence should be programmed. Memory read command (2EH) is followed by reverse encapsulation packet. DDI transmits video pixel data through encapsulation packet. Please refer to VESA spec for detailed description.

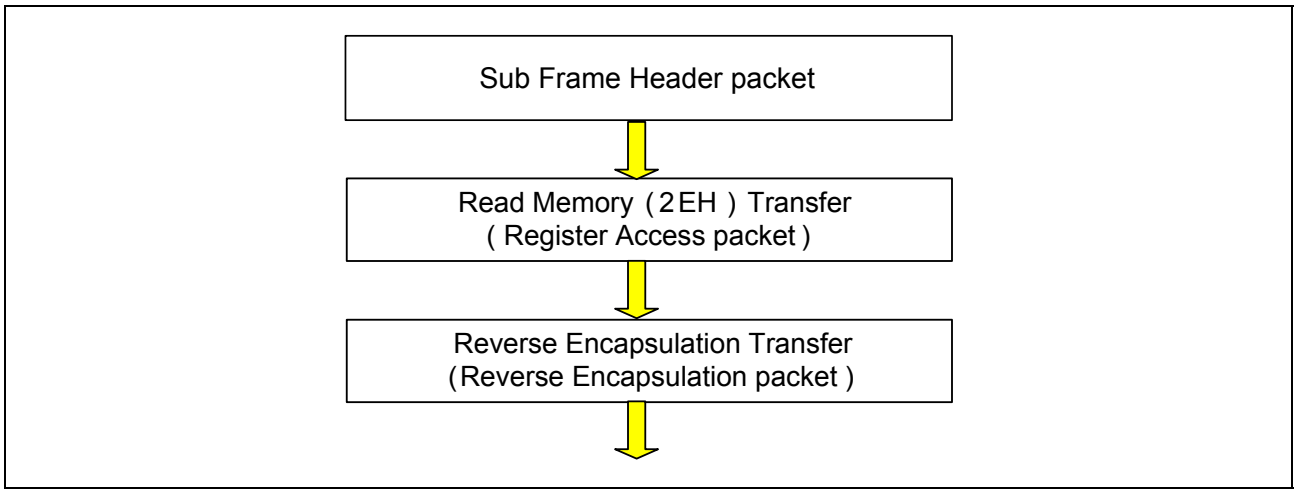


Figure 88. Reading video data from memory sequence

3.5.5.4. Reading Register Sequence

In order to read registers, the following sequence should be programmed. Register read command is followed by reverse encapsulation packet. DDI transmits register data through encapsulation packet. Please refer to VESA spec for detailed description.

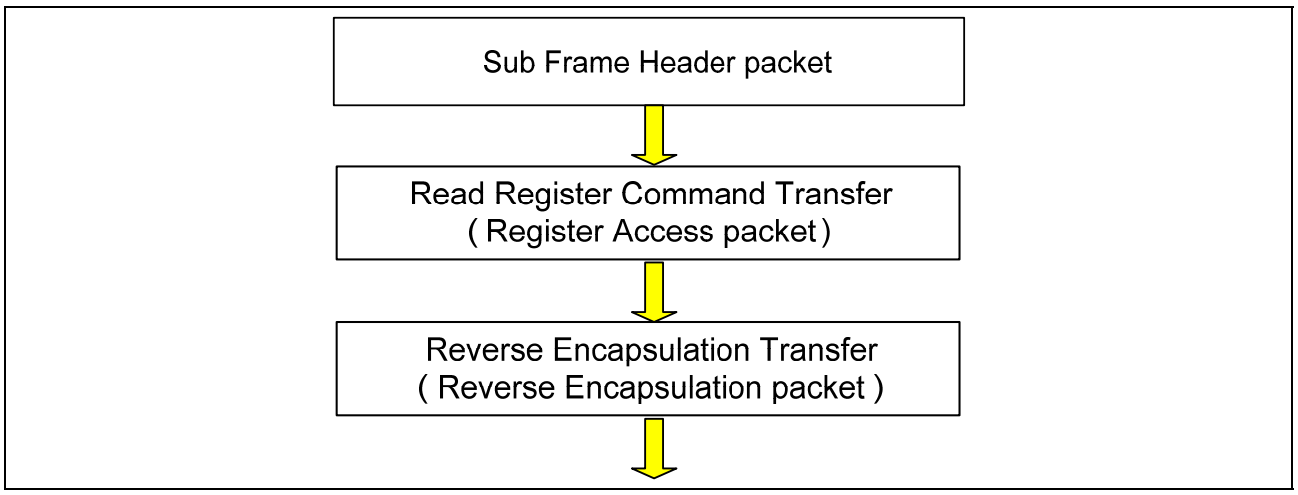


Figure 89. Reading register sequence

Note. Only Level 1 Registers are readable in MDDI.

Note. Not only level1 register (ex. D5h)

3.5.6. Tearing-less Display

In S6D04D1, the matching between data writes timing and written data display timing is important. If timing is mismatched, tearing effect can occur.

To avoid display tearing effect, two possible ways are suggested.

First case is that data write is slower than speed of displaying written data. In this case, data write speed is not critical, but current consumption in interface will be increased because data transfer time is long. Data write time is selected widely in this case.

Other case is that data write is faster than speed of displaying written data. In this case, data update speed is very high so that transfer time is to avoid data scan conflicts with data update.

The following figures describe some example to avoid display tearing phenomenon.

A. Display speed is slower than data write.

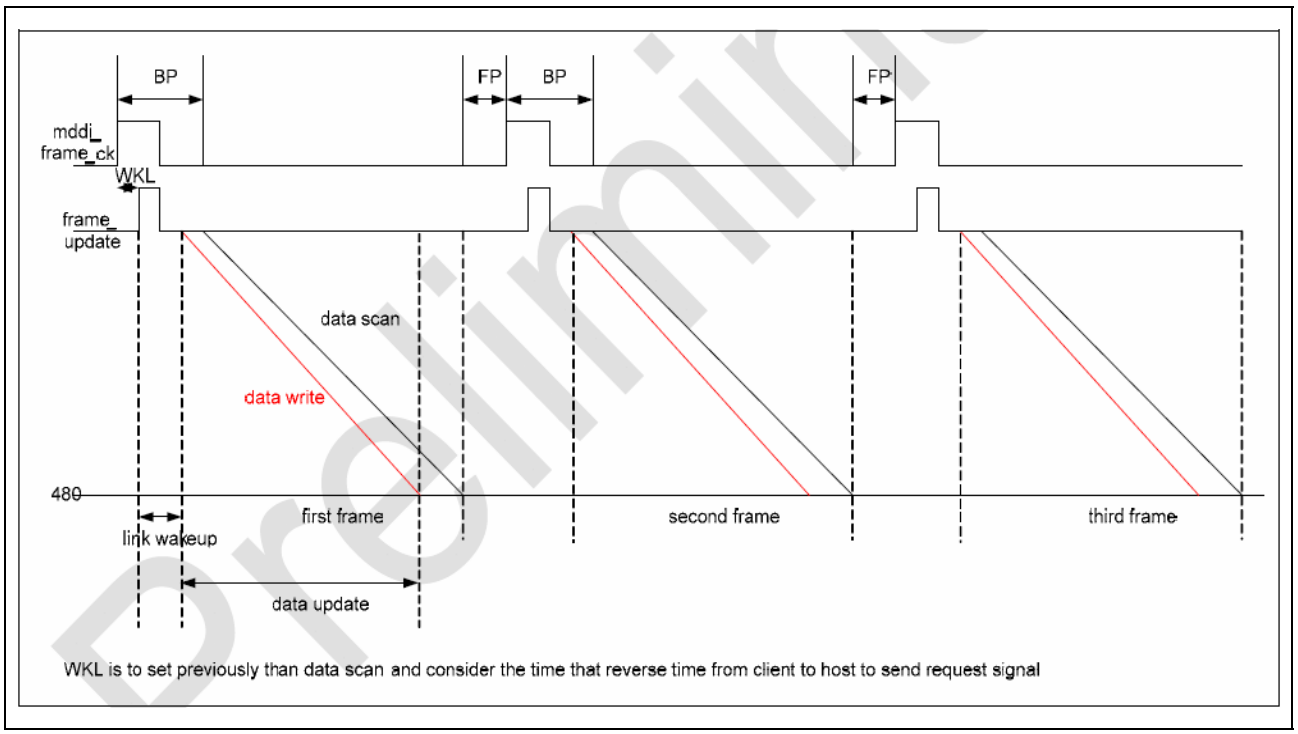


Figure 90. Tearing-less display: data write speed is faster then display

B. Display speed is faster than data write.

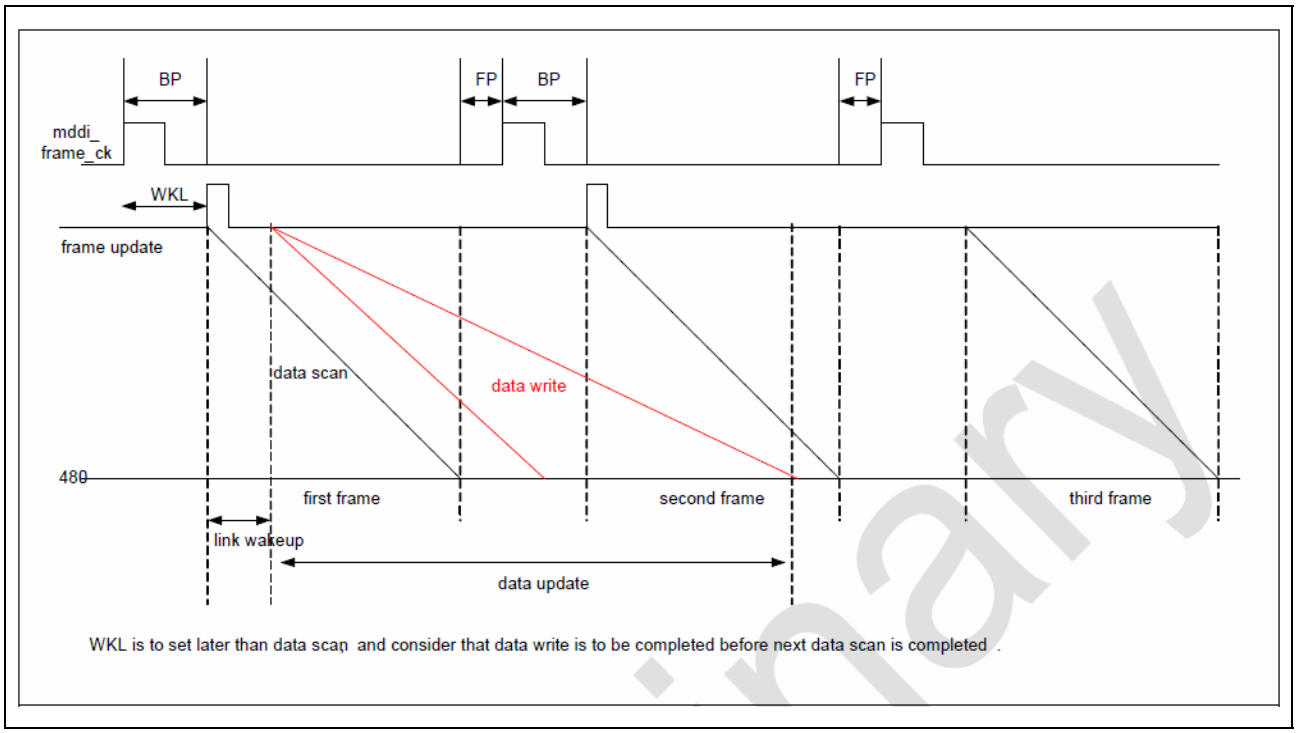


Figure 91. Tearing-less display: display speed is faster than data write

3.5.7. Hibernation / Wake-up

S6D04D1 support hibernation mode to save interface power consumption. MDDI link can enter the hibernation state quickly and wake up from hibernation quickly. This allows the system to force MDDI link into hibernation frequently to save power consumption.

During hibernation mode, the hi-speed transmitters and recivers are disabled and low-speed & low-power receivers are enabled in order detect wake-up sequence.

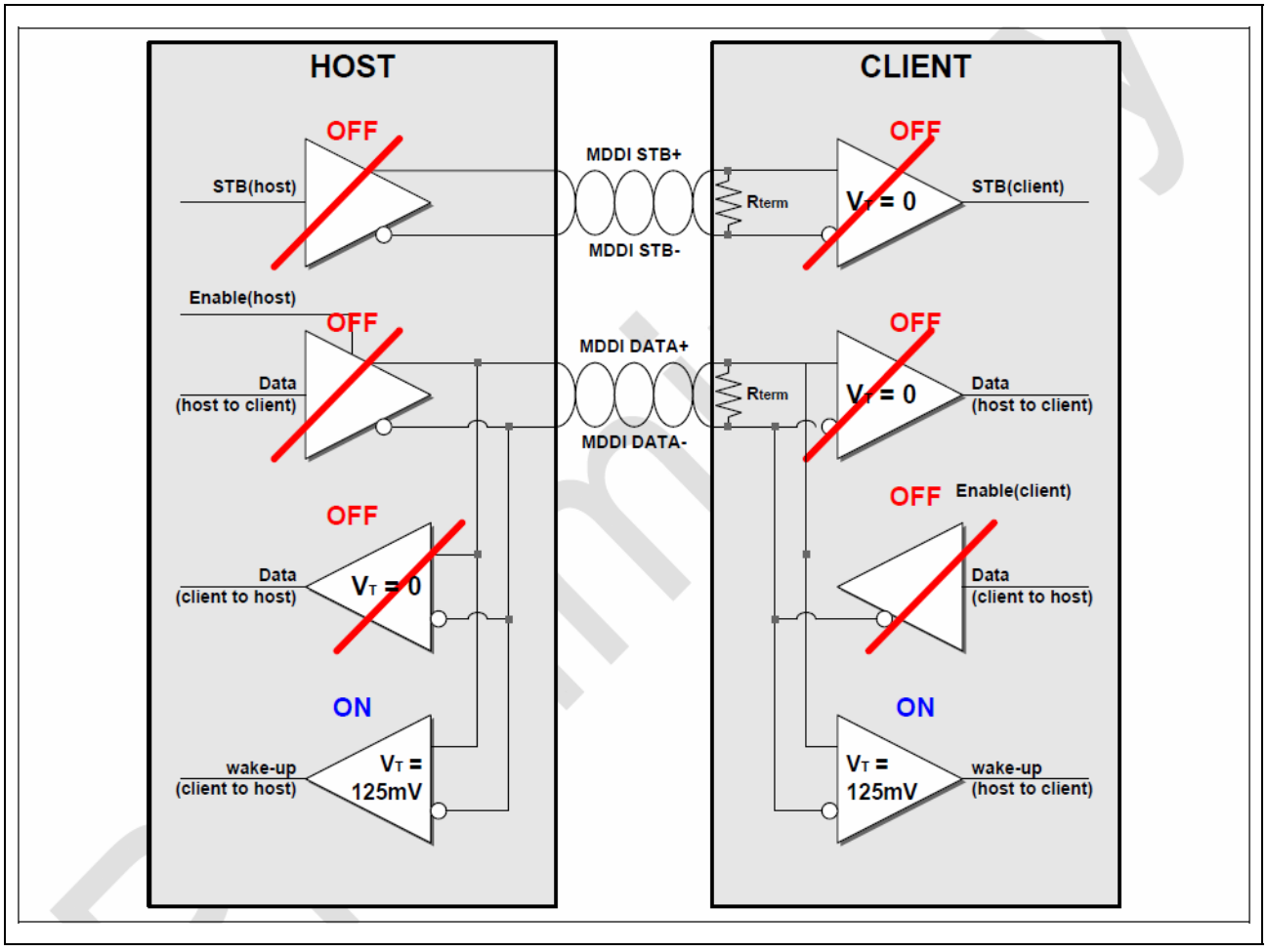


Figure 92. MDDI transceiver / receiver state in hibernation

When the link wakes up from hibernation, the host and client exchange a sequence of pulses. These pulses can be detected using low-speed, low-power receivers that concume only a fraction of the current of the differential receivers required to receive the signals at the maximum link operationg speed.

Either the client or the host can wake up the link; Host-initiated link wakeup.

3.5.8. MDDI Link Wake-up Procedure

A. Host-initiated link Wake-up Procedure

The simple case of host-initiated wake-up is described below without contention from the client trying to wake up at the same time. The following sequence of events is illustrated in the following figure.

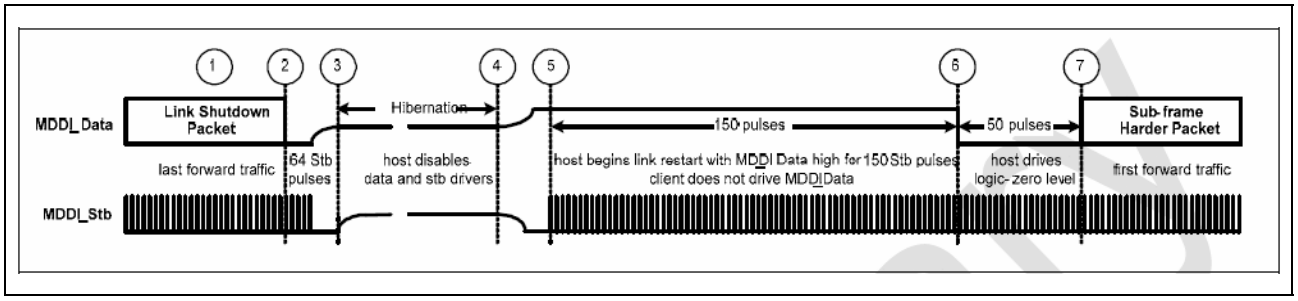


Figure 93. Host-Initiated link wake-up sequence

1. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.

2. Following the CRC of the Link Shutdown Packet the host toggle MDDI_STB for 64 cycles to allow processing in the client to finish before it stops MDDI_STB from toggling which stops the recovered clock in the client device. Also during this interval the host initially sets MDDI_DATA to a logic_zero level, and then disables the MDDI_DATA output in the range of 16 to 48 MDDI_STB cycles(including output disable propagation delays) after the CRC.
It may be desirable for the client to place its high-speed receivers for MDDI_DATA and MDDI_STB into a low power state any time after 48 MDDI_STB cycles after the CRC and before point 3.

3. The host enters the low-power hibernation state by disabling the MDDI_DATA and MDDI_STB drivers and by placing the host controller into a low-powre hibernation state.
It is also allowable for MDDI_STB to be driven to logic_zero level or to continue toggling during hibernation.
The client is also in the low-power hibernation state.

4. After a while, the host begins the link restart sequence by enabling the MDDI_DATA and MDDI_STB driver outpus. The host driver MDDI_DATA to a logic-one level and MDDI_STB to logic-zero level for at least the time it takes for the drivers to fully enable their outputs.
The host shall wait at least 200 nsec after MDDI_DATA reaches a valid logic-one level and MDDI_STB reaches a valid logic-zero level before driving pulses on MDDI_STB. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_STB. The client first detects the wake-up pulse using a low-power differential receiver having a +125mV input offset voltage.

5. The host drivers are fully enabled and MDDI_DATA is being driver to a logic-one level. The host begins to toggle MDDI_STB in a manner consistent with having logic-zero level on MDDI_DATA for duration of 150 MDDI_STB sysles.

6. The host drivers MDDI_DATA to logic-zero level for 50 MDDI_STB cycles. The client begins to look for the Sub-frame header Packet after MDDI_DATA is at logic-zero level for 40 MDDI_STB cycles.

7. The host begins to transmit data on the forward link by sending a Sub-frame Header Packet. Beginning at point 7. The MDDI host generates MDDI_STB based on the logic level on MDDI_DATA so that proper data-strobe encoding commences from point 7.

B. Client-initiated link Wake-up Procedure

An example of a typical client-initiated service request event with no contention is illustrated in the following figure.

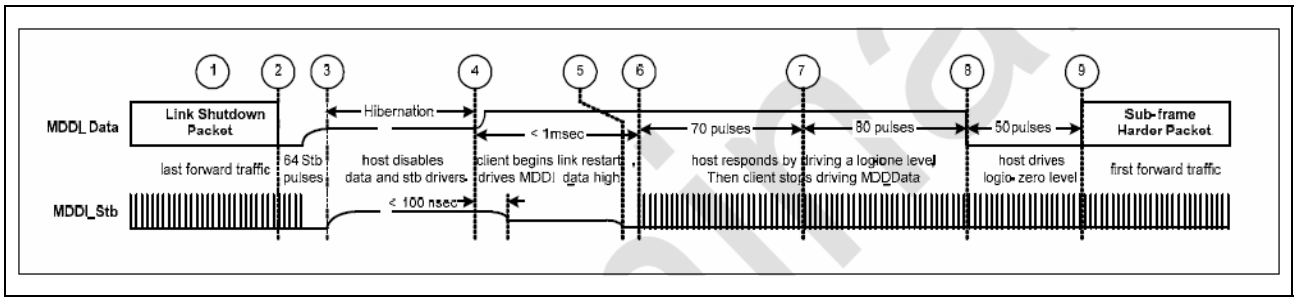


Figure 94. Client-Initiated link wake-up sequence

The Detailed description for labeled events are as follows;

1. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.

2. Following the CRC of the Link Shutdown Packet the host toggles MDDI_STB for 64 cycles to allow processing in the client to finish before it stops MDDI_STB from toggling which stops the recovered clock in the client device. Also during this interval the host initially sets MDDI_DATA to a logic_zero level, and then disables the MDDI_DATA output in the range of 16 to 48 MDDI_STB cycles(including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_DATA and MDDI_STB into a low power state any time after 48 MDDI_STB cycles after the CRC and before point 3.

3. The host enters the low-power hibernation state by disabling the MDDI_DATA and MDDI_STB drivers and by placing the host controller into a low-powre hibernation state.
It is also allowable for MDDI_STB to be driven to logic_zero level or to continue toggling during hibernation. The client is also in the low-power hibernation state.

4. After a while, the client begins the link restart sequence by enabling the MDDI_STB receiver and also enabling an offset in its MDDI_STB receiver to guarantee the state of the received version of MDDI_STB is a logical-zero level in the client before the host enables its MDDI_STB driver. The client will need to enable the offset in MDDI_STB immediately before enabling its MDDI_STB receiver to ensure that MDDI_STB receiver in the client is always receiving a valid differential signal and to prevent erroneous received signals from propagation into the client. After that, the client enables its MDDI_DATA driver while driving MDDI_DATA to a logic-one level. It is allowed for MDDI_DATA and MDDI_STB to be enabled simultaneously if the time to enable the offset and enable the standard MDDI_STB differential receiver is less than 200 nsec.

5. Within 1 msec the host recognaizes the service request pulse, and the host begins the link restart sequence by enabling the MDDI_DATA and MDDI_STB driver output. The host drivers MDDI_DATA to a logic-one level and MDDI_STB to a logic-zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200 nsec after MDDI_DATA reaches a valid logic-one level and MDDI_STB reaches a valid fully-driven logic-zero level before diving pulses on MDDI_TSB. This gives the client sufficient time to prepare to receive higi-speed pulses on MDDI_STB.

6. The host begins outputting pulses on MDDI_STB and shall keep MDDI_DATA at a logic-one level for a total duration of 150 MDDI_STB pulses through point 8. The host generates MDDI_STB in a manner consistent with sending a logical-zero level on MDDI_DATA. When the client recognaizes the first pulse on MDDI_STB it shall disable the offset in its MDDI_STB receiver.

7. The client continues to drive MDDI_DATA to a logic-one level for 70 MDDI_STB pulses, and the client disables its MDDI_DATA driver at point 7. The host continues to drive MDDI_DATA to a logic-one level for duration of 80 additional MDDI_STB pulses, and at point 8 drivers MDDI_DATA to logic-zero level.

8. The host drivers MDDI_DATA to logic-zero level for 50 MDDI_STB cycles. The client begins to look for the Sub-frame header Packet after MDDI_DATA is at logic-zero level for 40 MDDI_STB cycles.

9. After asserting MDDI_DATA to logic-zero level and driving MDDI_STB for duration of 50 MDDI_STB pulses the host begins to transmit data on the forward link at point 9 by sending a Sub-frame Header Packet.
The client begins to look for the Sub-frame Header Packet after MDDI_DATA is at logic-zero level for 40 MDDI_STB cycles.

3.5.9. Client-Lnitiated Link Wake-up

S6D04D1 supports VSYNC based Link client-initiated link wake-up. As client-initiated wake-up action is executed in hibernation state only, the register for each wake-up have to be set before link shutdown.

A. VSYNC Based Link Wake-up

In display-ON state, when the IC finishes displaying all internal GRAM data, data request must be transferred to MDDI host for new video data. As MDDI link is usually in hibernation for reducing interface power consumption, MDDI link wake-up must be done before internal GRAM update. In that case, client initiated link wake-up can be used as data request.

When VSYNC based link wake-up register(E0h: VWAKE_EN) is set, client iniitiated wake-up is executed in synchronization with the vertical-sync signal which generated in S6D04D1. Using VSYNC based link wake-up, tearing-less display can be accomplished if interface speed and wake-up time is well known.

The following figure shows detailed timing for VSYNC based link wake-up.

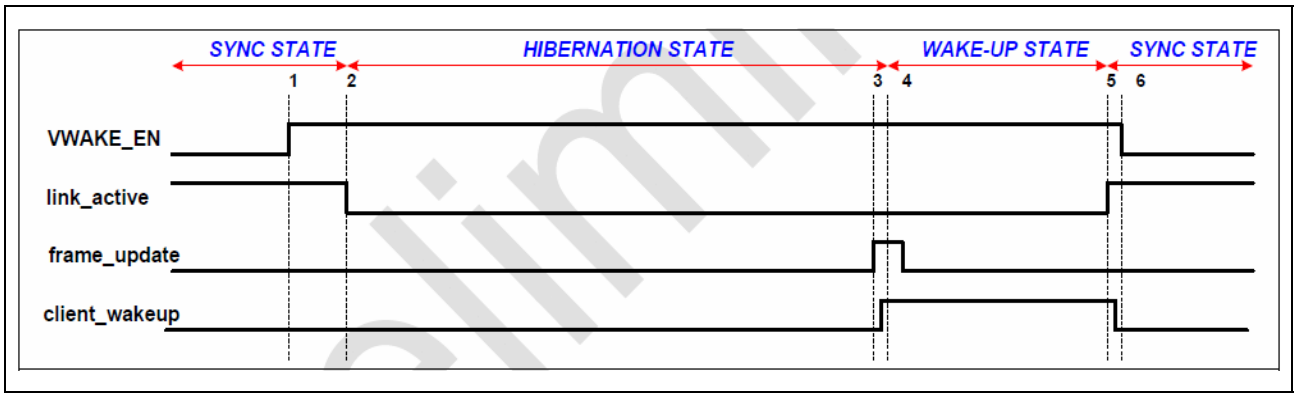


Figure 95. VSYNC based link wake-up procedure

The detailed description for labeled events as follows:

1. MDDI host writes to the VSYNC based link wakeup register to enable a wake-up based on internal vertical-sync signal.

2. Link_active gose low when the host puts in the link into hibernation after no more data needs to be sent to the S6D04D1.

3. Frame_update, the internal vertical-sync signal goes high indicating that update pointer has wrapped around and is now reading from the begining of the frame buffer. Link wake-up can be set using WKF and WKL(E1h) registers. WKF specifies the number of frame before wake-up; WKL specifies the number of lines before wake-up.

4. Client_wakeup input to the MDDI client goes high to start the client initiated link wake-up.

5. Link_active goes high after the host brings the link out of hibernation.

6. After link wake-up, client_wakeup signal and the VWAKE_EN register are cleared automatically.

3.5.10. MDDI Operation

In MDDI, 6 oparetion modes are available. The following table describes 6 modes.

Table 59. MDDI operation modes

STATE	OSC	Booster Circuit	Internal Logic Status	MDDI I/O	Wake-up by
INIT_HIBER	OFF	Disable	Dispaly OFF Internal Logic ON MDDI Link hibernation	Hibernation driver ON	Host-Initiated
WAIT	OFF	Disable	Dispaly OFF Internal Logic ON MDDI Link in SYNC	Standard driver ON	-
NORMAL	ON	Enable	Dispaly ON Internal Logic ON MDDI Link SYNC	Standard driver ON	-
SLEEP	OFF	Disable	Dispaly OFF Internal Logic ON MDDI Link SYNC	Standard driver ON	-
HIBER	ON	Enable	Dispaly ON Internal Logic ON MDDI Link hibernation	Hibernation driver ON	Host-Initiated Client-Initiated (VSYNC)
STOP	OFF	Disable	Dispaly OFF Internal Logic ON MDDI Link OFF	Driver All OFF	RESET

INIT_HIBER: Initial status when external power is connected to the IC. In this state, internal oscillator is OFF, and MDDI link is hibernation state. As no command or signal is applied to the IC except RESET input and booster circuit is OFF, and internal logic is ON.

WAIT: After the wake-up sequence, the IC is in WAIT state. MDDI link is in SYNC, and internal logic is ON, and booster is still OFF because no other register access or video stream packet is transferred to the IC.

NORMAL: MDDI link, booster circuit, and internal logic circuit is ON. Register access or Video data transfer is available in NORMAL state.

HIBER: When no more video data update is needed, MDDI link is in hibernation so that interface power can be reduced. Internal booster & logic circuits are still operating. MDDI link wakeup will be accomplished when VSYNC wakeup register is set before hibernation.

SLEEP: This state is set by register access. Booster is OFF, but MDDI link and internal logic have to be in SYNC because the IC must receive commands for power save or normal operation.

STOP: STOP state is set by MDDI_SLP register access(E0h). In this state, MDDI link, internal oscillator, Booster are all OFF and internal logic is still ON. To release STOP state, input reset signal. After reset, status is INIT_HIBER state.

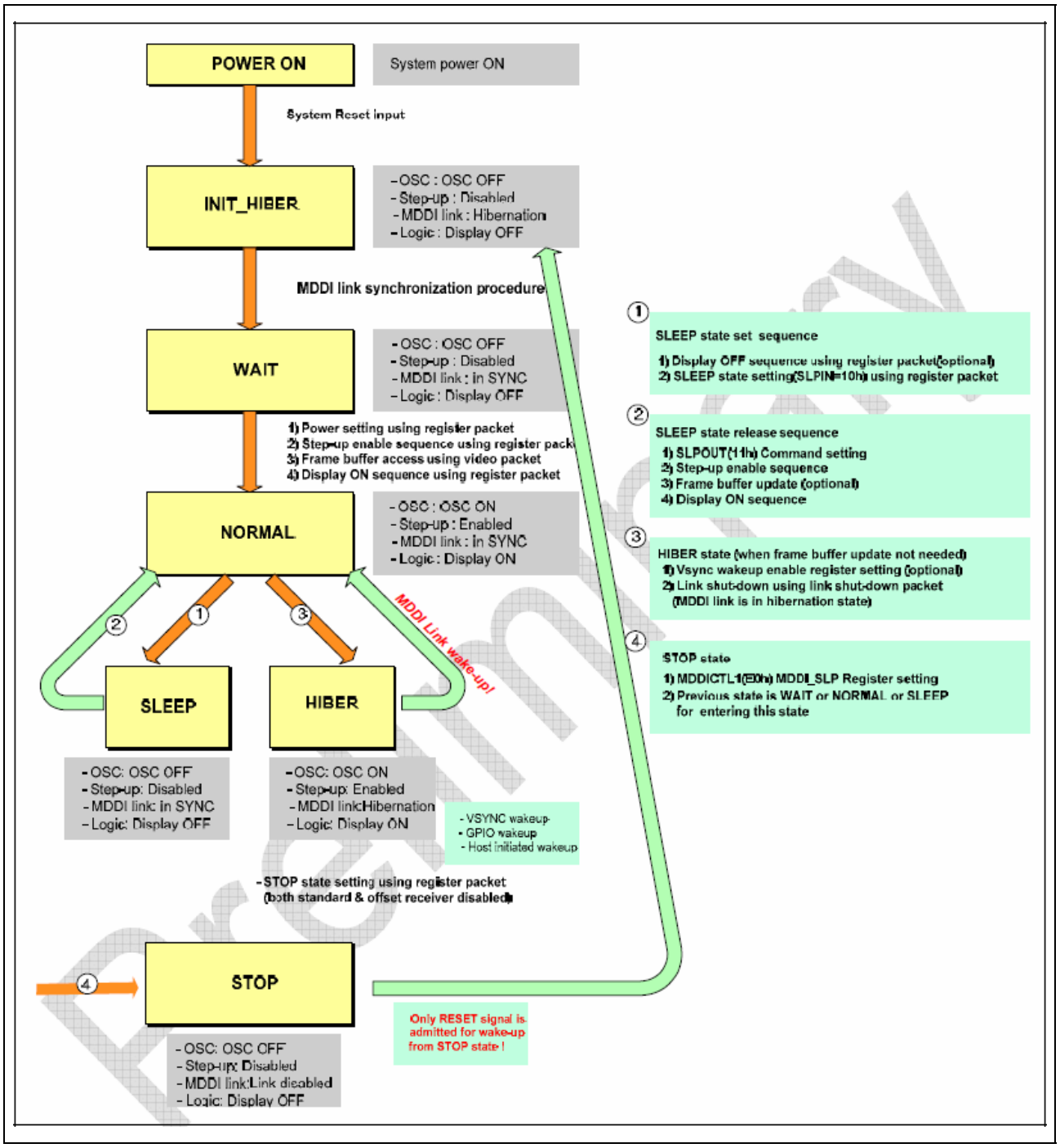


Figure 96. Operating state in MDDI mode

CHAPTER 4

FUNCTIONAL DESCRIPTION

4 FUNCTIONAL DESCRIPTION

4.1. POWER

4.1.1. Power ON / OFF sequence

VDD3 and VCI can be applied in any order.

VDD3 and VCI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and VDD3 must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDD3 or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note. There will be damage to the display module if the power sequences are not met.

There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

There will be no abnormal visible effects on the display between the end of Power On Sequence and before the reception of Sleep Out command. Same is the case between receiving Sleep In command and Power Off Sequence.

If RESX line is not held stable by host during Power On Sequence, it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise, function is not guaranteed.

The power on/off sequence is illustrated in the next pages.

4.1.1.1. Case-1 RESX line is held High or Unstable by Host at Power On

If RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and VDD3 have been applied – otherwise, correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

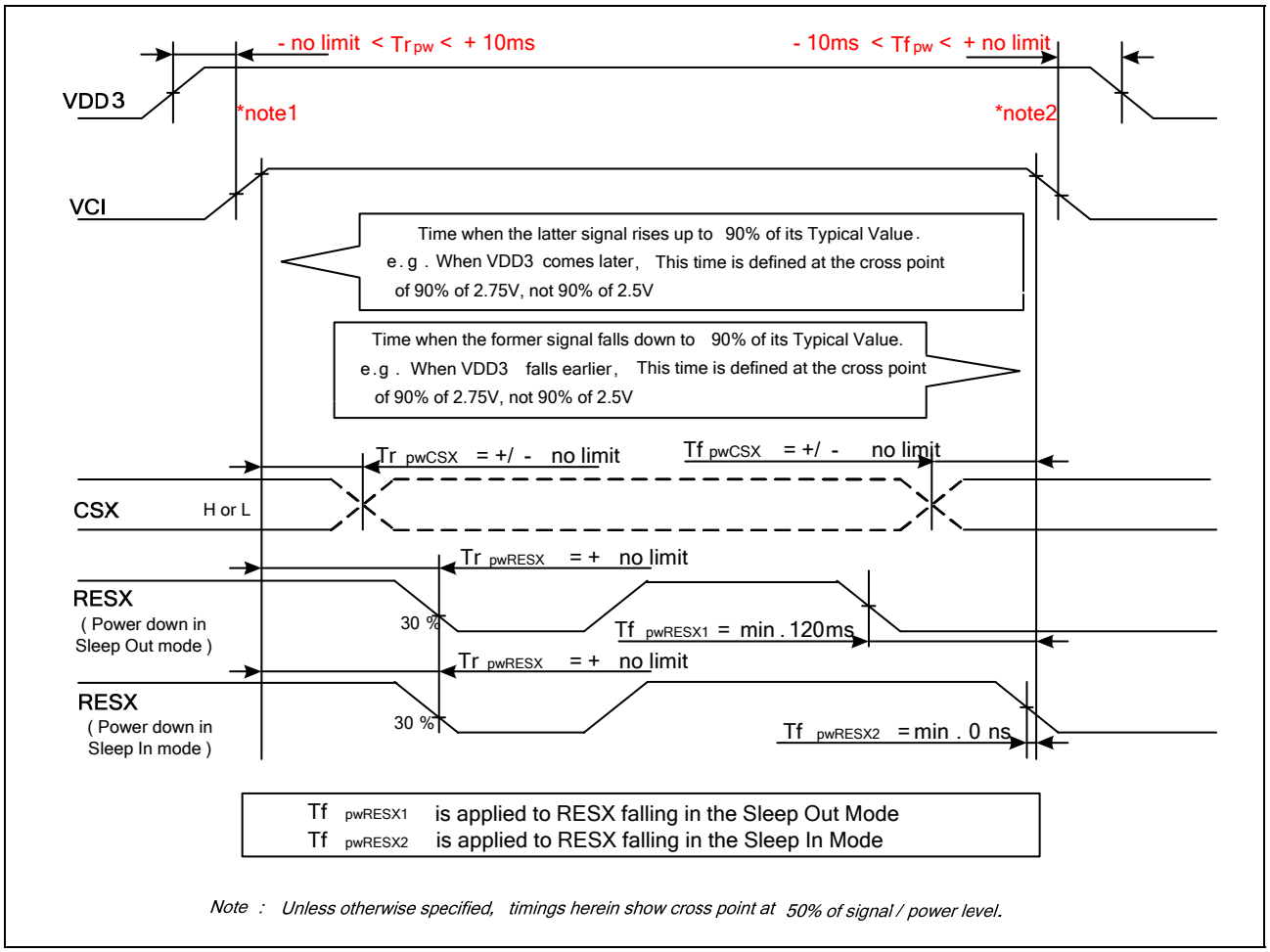


Figure 97. RESX line is held high or unstable by host at power on

Note1. In case that VCI comes first, VDD3 should be applied & settled within 10ms after VCI is applied.

Note2. In case that VCI disappears first, VDD3 should also be turned off within 10ms after VCI is off.

4.1.1.2. Case-2 RESX line is held Low by Host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10μsec after both VCI and VDD3 have been applied

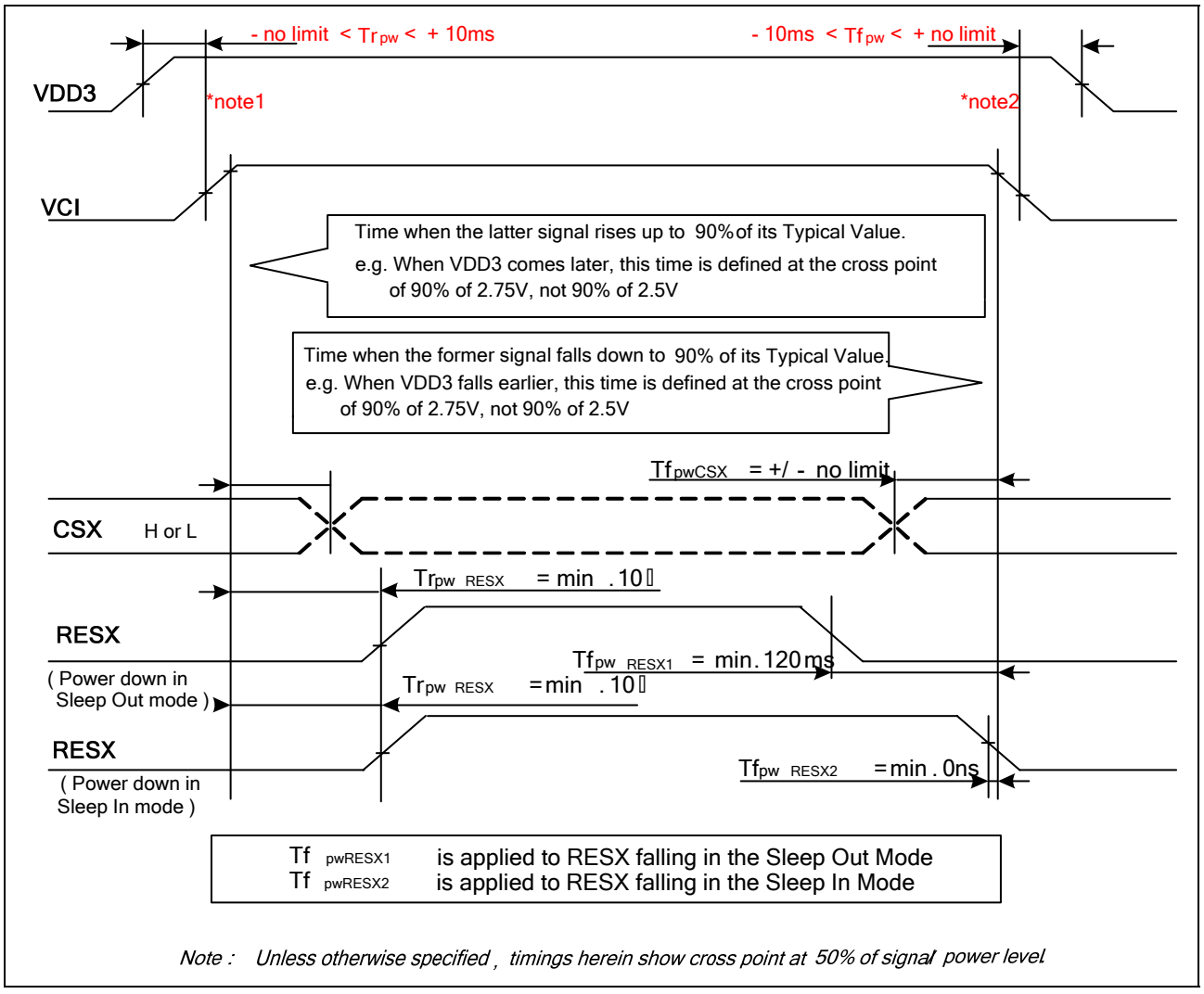


Figure 98. RESX line is held low by host at power on

Note1. In case that VCI comes first, VDD3 should be applied & settled within 10ms after VCI is applied.

Note2. In case that VCI disappears first, VDD3 should also be turned off within 10ms after VCI is off.

4.1.2. Abrupt Power Off

The abrupt power-off represents a situation where, for e.g., a battery is removed without the expected power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an abrupt power-off, the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until “Power-On Sequence” powers it up.

4.1.3. Power Levels

S6D04D1 supports 6 types of power-consumption modes. Each mode is described as follows:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out
In this mode, the display is able to show maximum 16,777,216 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out
In this mode, part of the display is used with maximum 16,777,216 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out
In this mode, the full display area is used but with 8 colors,

4. Partial Mode On, Idle Mode On, Sleep Out
In this mode, part of the display is used but with 8 colors

5. Sleep In Mode
In this mode, the booster, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDD3 power supply. Contents of the memory are safe.

6. Power Off Mode.
In this mode, both VCI and VDD3 are removed

Note. Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

4.1.4. Power Flow Chart for Different Power Modes

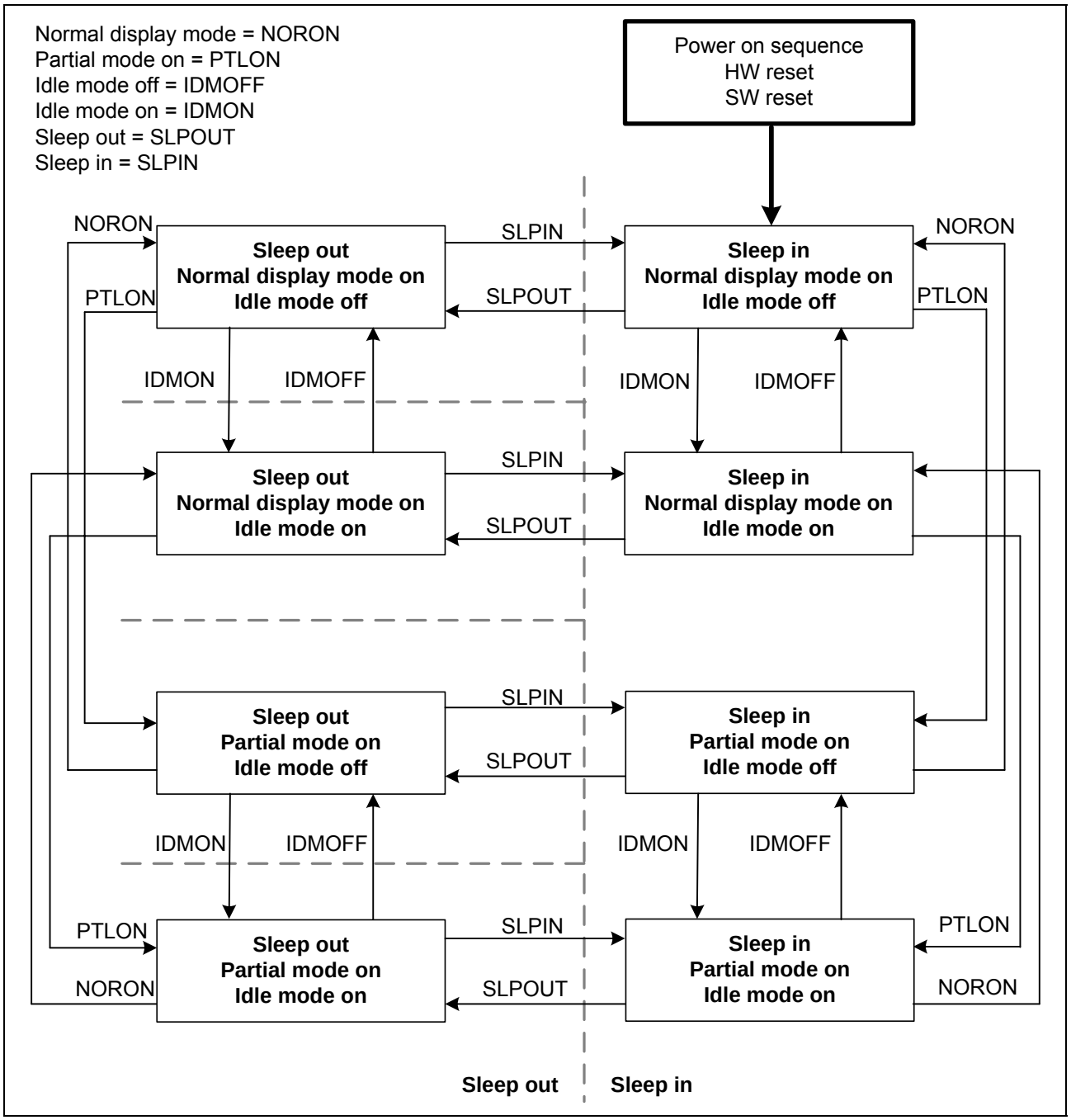


Figure 99. Power-on flowchart for various power modes

Note1.There is no abnormal visual effect when there is a change from one power mode to another power mode.

Note2.There is no limitation, which is not specified by this spec, when there is a change from one power mode to another power mode

4.1.5. Power Supply

The following figure shows a configuration of the voltage generation circuit of S6D04D1. The booster circuit consists of booster circuits 1 to 3. Booster circuit1 doubles input voltage supplied from VCI1 for AVDD level. Booster circuit2 makes 2.5, 3 or 3.5 times AVDD level for VGH level, and makes -1.5, -2 or -2.5 times AVDD level for VGL level. Booster circuit3 reverses the VCI1 level with respect to VSS to generate VCL level. These Booster circuits generate power supplies AVDD, VGH, VGL, and VCL. Reference voltages such as GVDD, VCOMH and VCOML are generated with VREF from the voltage adjustment circuit. Connect VCOM to the TFT panel.

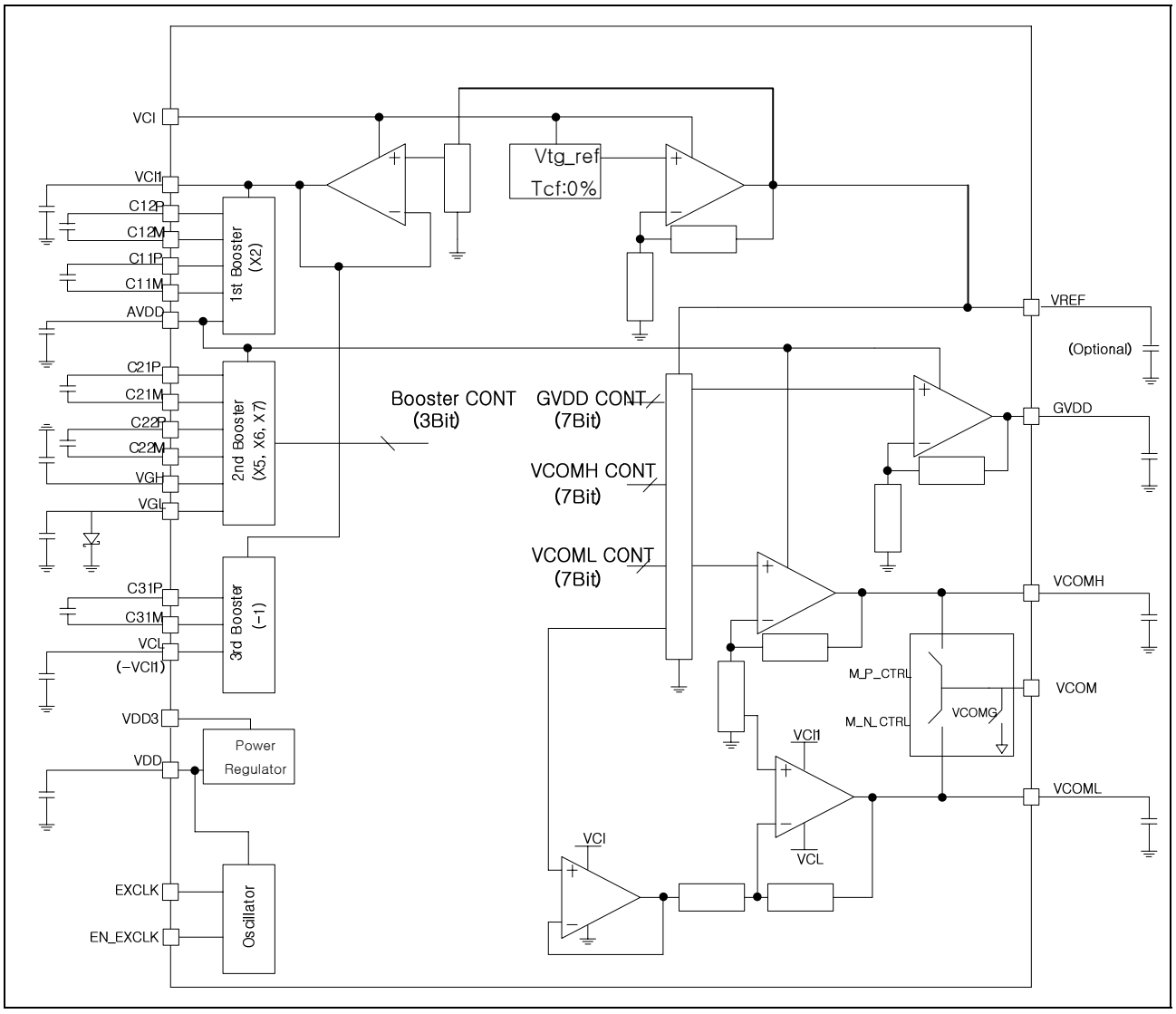


Figure 100. Configuration of the internal power-supply circuit

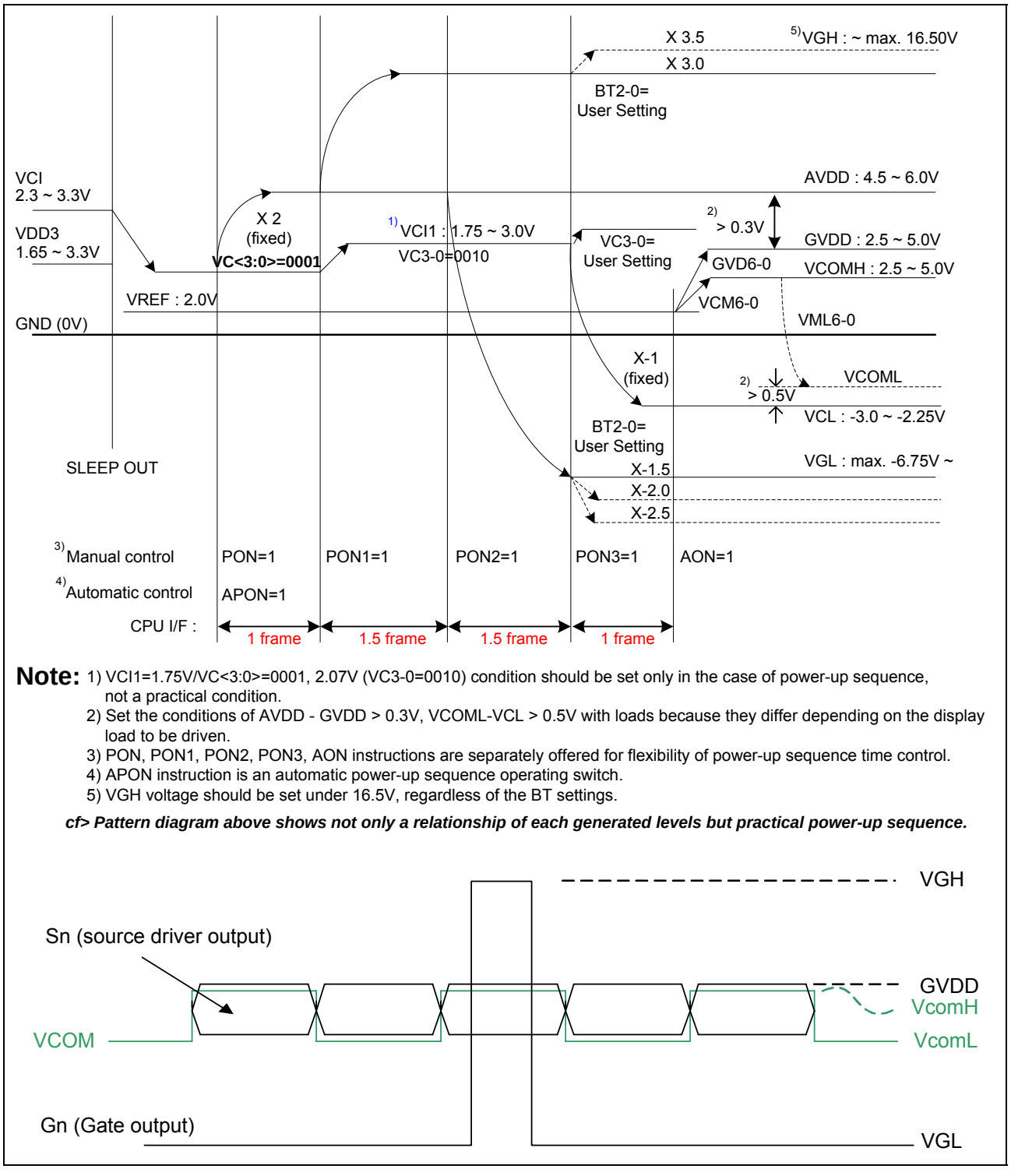
Note. Use the 1uF capacitor.

Schottky diode between VGL and VSS is positively necessary for making the circuitry latch-up free.

The Capacitor between VREF and VSS may be used in the case of occurring fluctuation in VCOM swing level.

4.1.6. Pattern Diagrams for Voltage Setting

The following figure shows a pattern diagram for the voltage setting and an example of waveforms.



Note: 1) VCI1=1.75V/VC<3:0>=0001, 2.07V (VC3-0=0010) condition should be set only in the case of power-up sequence, not a practical condition.
2) Set the conditions of AVDD - GVDD > 0.3V, VCOML-VCL > 0.5V with loads because they differ depending on the display load to be driven.
3) PON, PON1, PON2, PON3, AON instructions are separately offered for flexibility of power-up sequence time control.
4) APON instruction is an automatic power-up sequence operating switch.
5) VGH voltage should be set under 16.5V, regardless of the BT settings.

cf> Pattern diagram above shows not only a relationship of each generated levels but practical power-up sequence.

Figure 101. Power-up pattern diagram & an example of source/VCOM waveforms

4.1.7. Set up Flow of Power

Apply the power in a sequential way as shown in the following figure. The settling time of the oscillation circuit, booster1/2/3 circuits, and operational amplifier depends on the external resistance or capacitance value.

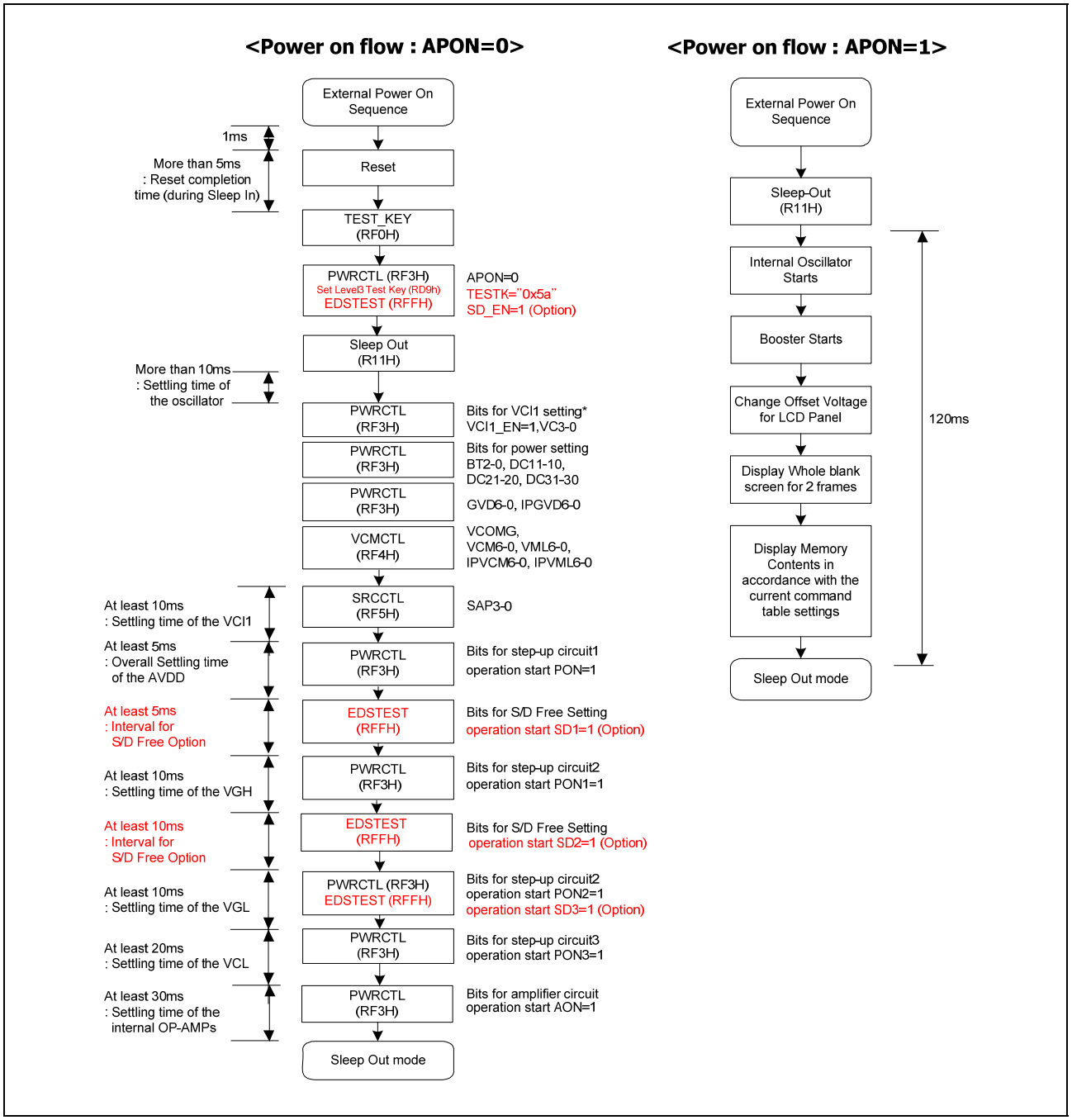


Figure 102. Setup flow of power

Note. The VCI1 voltage level is set to the user setting value when a PON3 value is high for latch-up free sequence

When PON3 = 0 : VCI1 = 1.75V after SLPOUT, 2.07V after PON1=1

When PON3 = 1 : VCI1 = User setting value (VC3-0)

Power on flow (APON=0): manual power-up sequence by register setting.

Power on flow (APON=1): automatic power-up sequence.

4.1.8. Deep-Standby Sequence

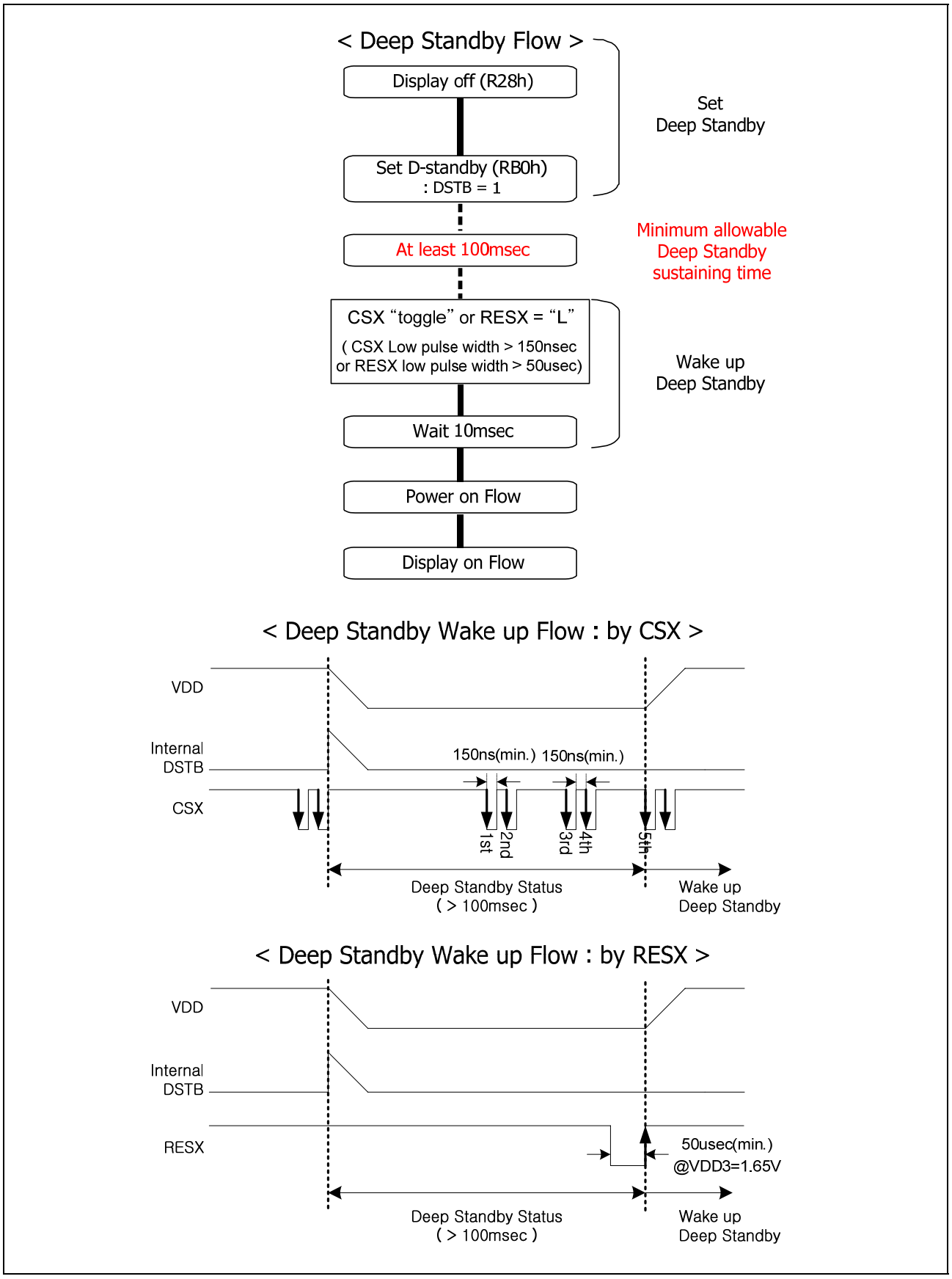


Figure 103. Deep-Standby Sequence

4.1.9. Voltage Regulation Function

The S6D04D1 has an internal voltage regulator. By the use of this function, unexpected damages on internal logic circuit can be avoided. Furthermore, low power consumption can also be obtained. Detailed function description and applicable configuration are described in the following diagram.

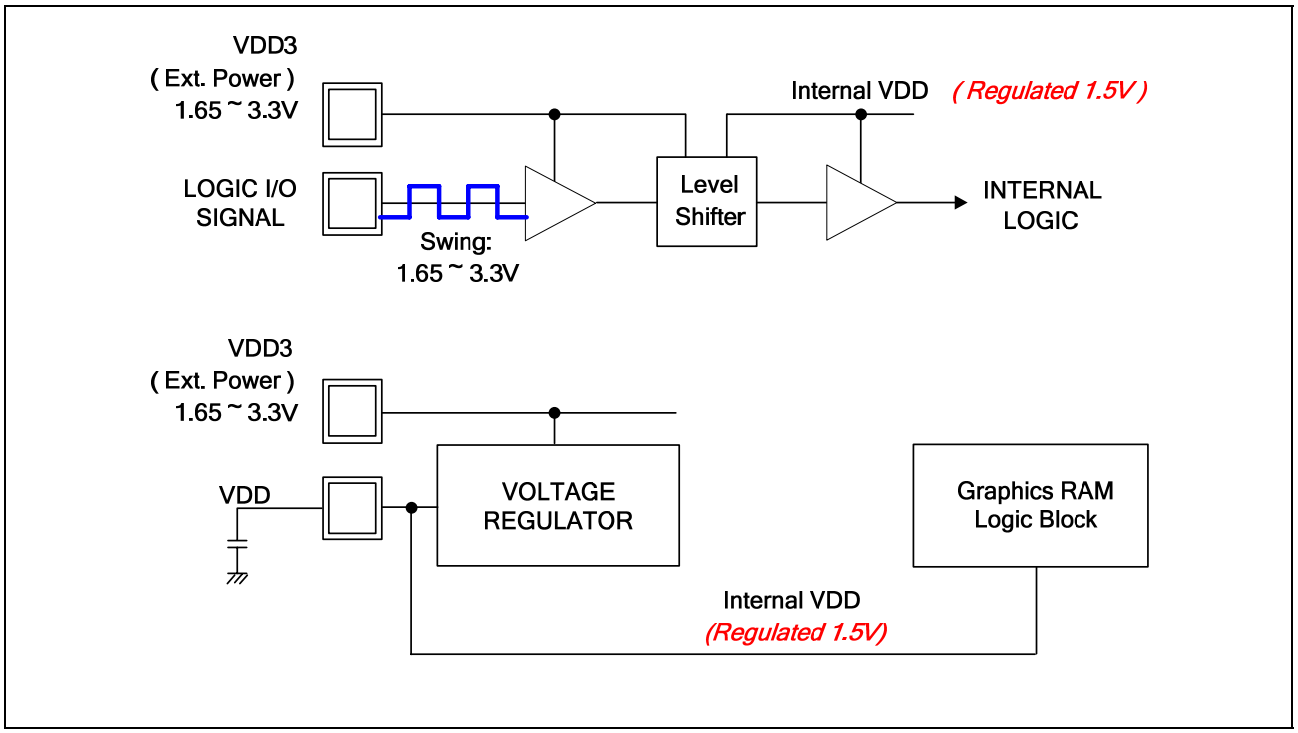


Figure 104. Voltage regulation function

4.2. SOURCE

4.2.1. Source Driver

The liquid crystal display source driver circuit consists of 720 drivers (S1 to S720).

Display pattern data is latched when 720-bit data has arrived. Then the latched data enables the source drivers to output to expected voltage level. The SS bit can change the shift direction of 720-bit data by selecting an appropriate direction for the device-mounted configuration. When less than 720 sources are required, the unused source outputs should be left open.

4.2.2. Gamma Adjustment Function

S6D04D1 provides the gamma adjustment function to display 16,777,216 colors simultaneously for each R/G/B color. The gamma adjustment executed by the high/ mid/ low level adjustment registers determines 13 grayscale reference levels. Furthermore, since the high-level adjustment register, mid-level adjustment register and the low-level adjustment register have the positive polarities and negative polarities, you can adjust them to match LCD panel and a gamma for each R/G/B color, respectively..

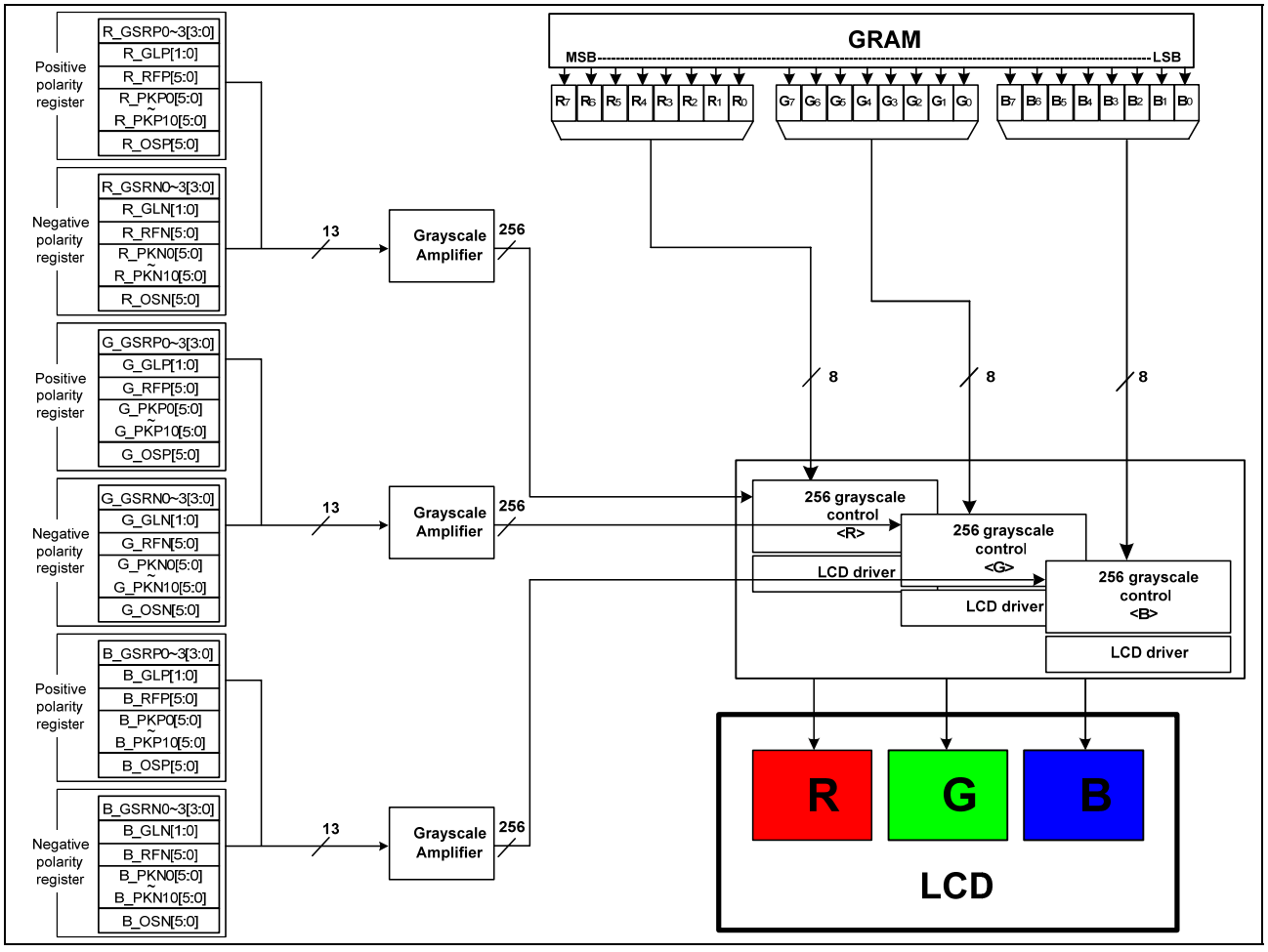


Figure 105. Block diagram of gamma adjustment function

4.2.3. Gamma Curve

4.2.3.1. Gamma Curve

Gamma Curve, applies the function. $y = x^{2.2}$

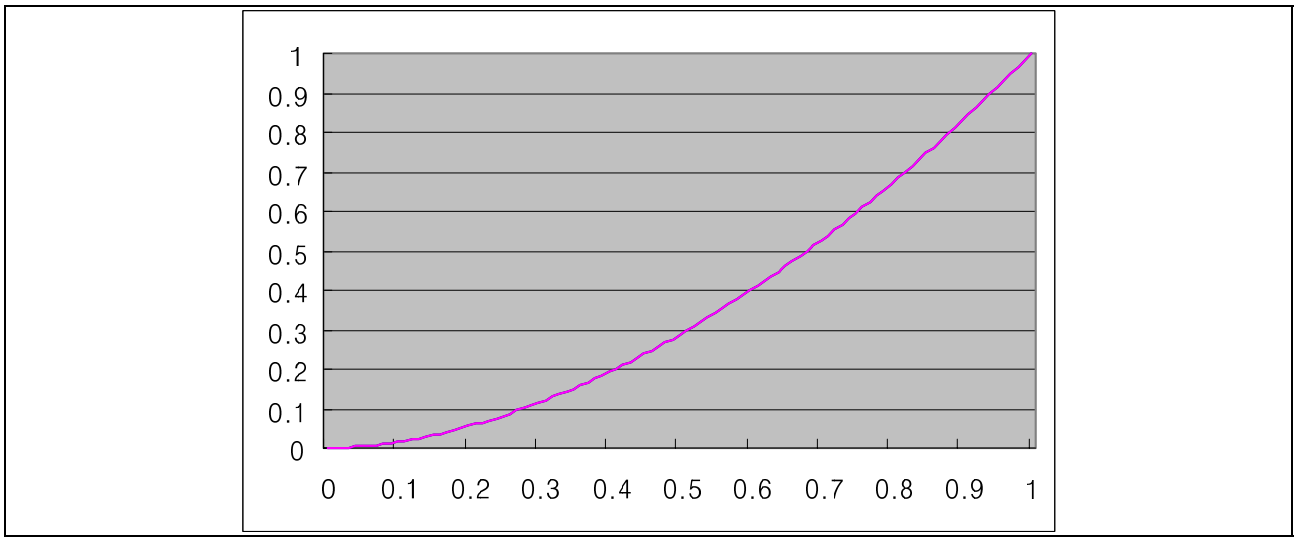


Figure 106. Gamma $y = x^{2.2}$

4.2.4. Structure of Grayscale Amplifier

The structure of grayscale amplifier is shown as below. The 13 voltage levels (VIN0-VIN12) between GVDD and VGS are determined by the reference adjustment register, the amplitude adjustment resister, the x-axis symmetric adjustment register, the micro-adjustment register and the gray-shift register. Each level is split into 256 levels again by the internal ladder resistor network. As a result, grayscale amplifier generates 256 voltage levels ranging from V0 to V255.

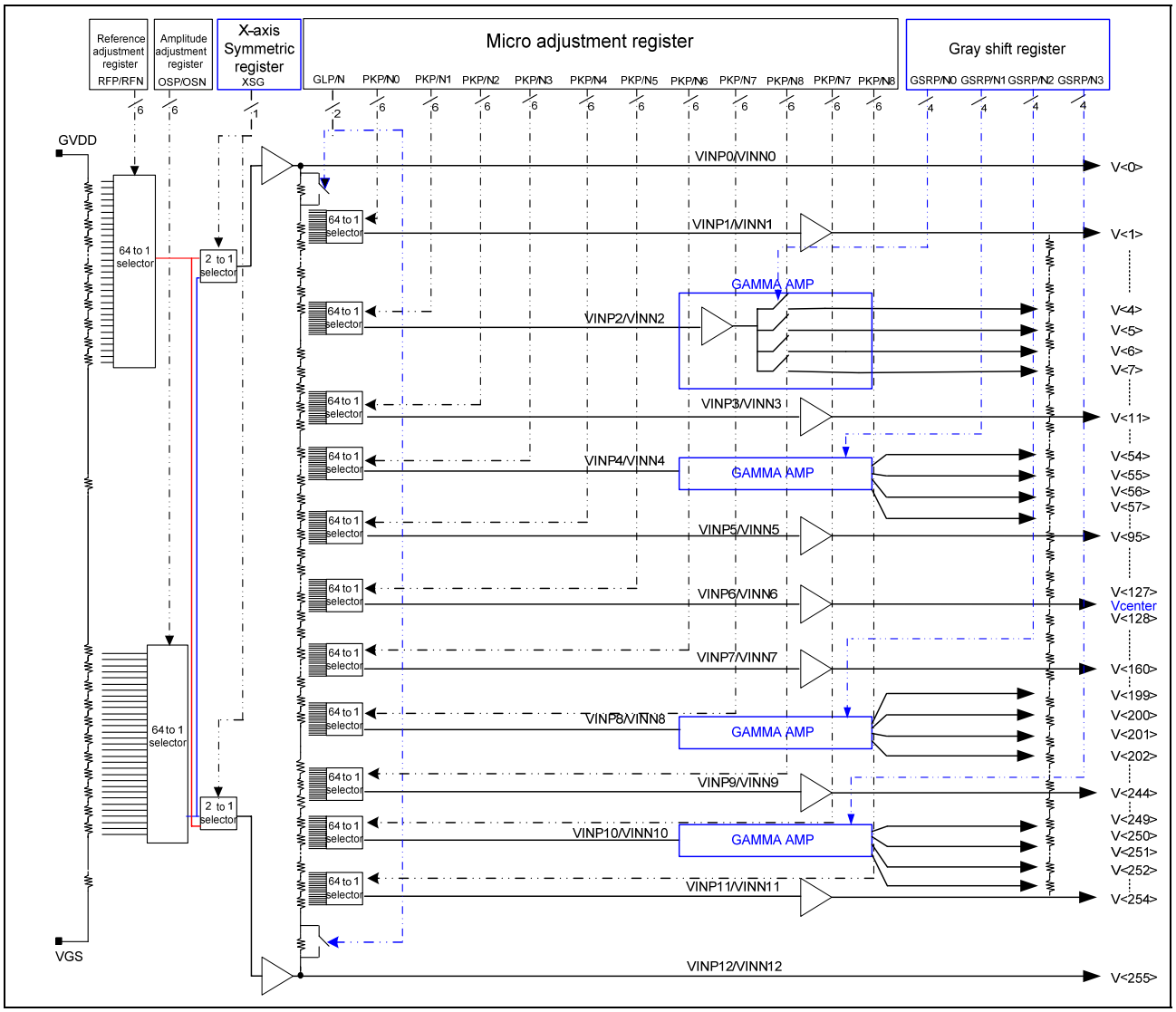


Figure 107. Structure of gray scale amplifier

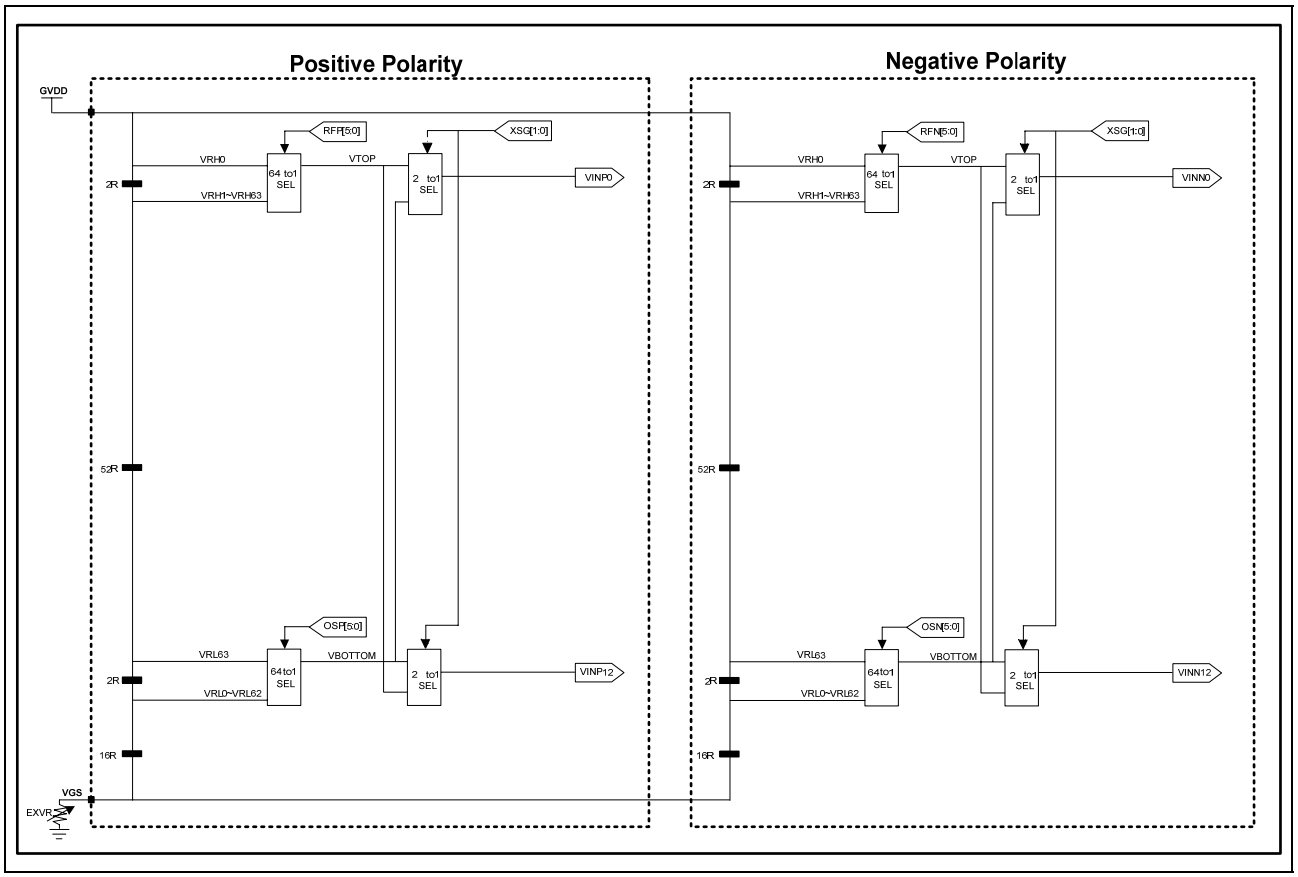


Figure 108. Structure of resistor ladder network 1.

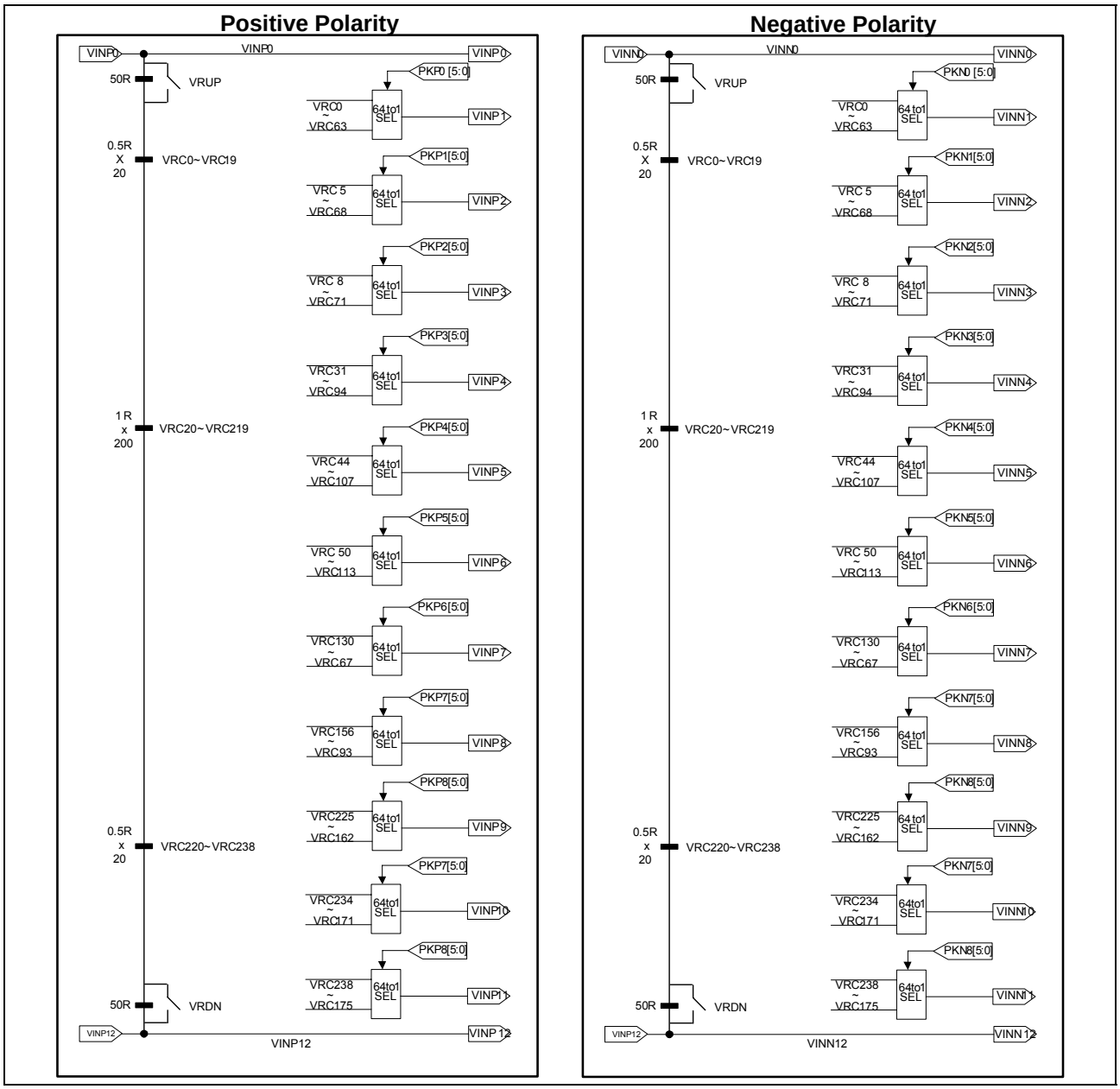


Figure 109. Structure of resistor ladder network 2.

4.2.5. Gamma Adjustment Register

This block has registers to set up the grayscale voltage according to the gamma specification of the LCD panel. These registers can independently set up the positive/negative polarities. There are 4 types of register groups to adjust the amplitude on the grayscale characteristics of the grayscale voltage, and R/G/B gamma adjustment registers are separated. The following figures indicate the operation of each adjustment registers.

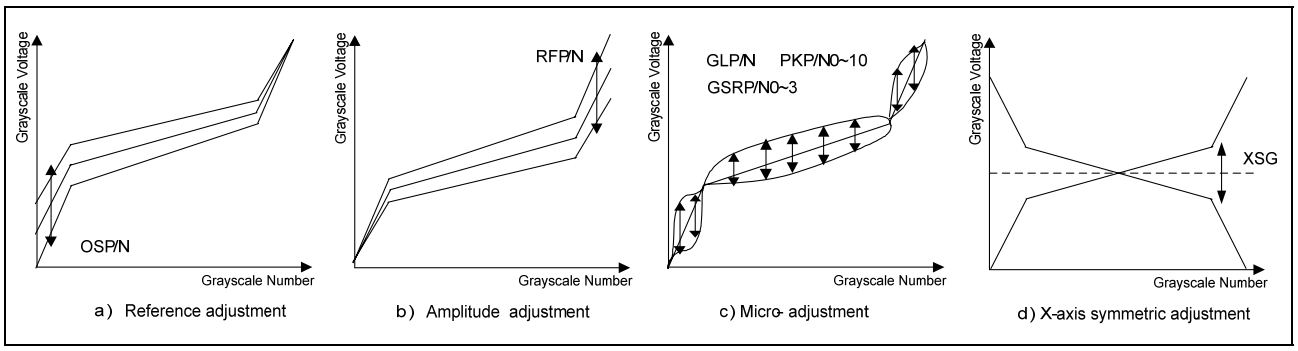


Figure 110. The operation of adjusting register

4.2.5.1. Reference adjustment register

The Reference adjustment register is used to adjust the reference of the grayscale voltage. To accomplish the adjustment, it controls the VINP12/VINN12 voltage level by 64 to 1 selector towards the 64-leveled reference voltage generated from the resistor ladder between GVDD and VGS.

4.2.5.2. Amplitude adjustment register

The Amplitude adjustment register is to adjust the amplitude of the grayscale voltage. To accomplish the adjustment, it controls the VINP0/VINN0 voltage level by 64 to 1 selector towards the 64-leveled reference voltage generated from the resistor ladder between GVDD and VGS.

4.2.5.3. Micro-adjustment register

The Micro adjustment register is employed to make subtle adjustment to the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 64 to 1 selector towards the 64-leveled reference voltage generated from the resistor ladder. Also, there is an independent register on the positive/negative polarities as well as other adjustment registers.

4.2.5.4. Gray shift register

The Gray shift register is employed to make subtle adjustment to the grayscale voltage level. To accomplish the adjustment, it controls 4 point reference voltage level by the switch. Also, there is an independent register on the positive/negative polarities as well as other adjustment registers

4.2.5.5. X-axis symmetric adjustment register

The X-axis symmetric adjustment register is to adjust X-axis symmetric of the grayscale voltage. This register can be detailedly explained with NGF register selection. 1st case; when XSG=0 and NGF=0, Vp<N>+Vn<N>=Vp<0>+Vn<0> and gamma symmetric axis is (Vp<0>+Vn<0>)/2. 2nd case; when XSG=0 and NGF=1, negative gamma voltage can be changed using negative gamma register value and symmetric axis will be changed according to negative gamma voltage. 3rd case; when XSG=1 and NGF=0, Vp<N>=Vn<|255-N|>. 4th case; when XSG=1 and NGF=1, Vp<N>+Vn<N> ≠ Vp<0>+Vn<0> but can have similar value in some degree using both positive and negative gamma registers.

Table 60. Description of gamma adjustment register

Register	Positive polarity	Negative polarity	Set-up contents
Reference adjustment Amplitude adjustment	OSP[5:0]	OSN[5:0]	The voltage of VBOTTOM is selected by the 64 to 1 selector
	RFP[5:0]	RFN[5:0]	The voltage of VTOP is selected by the 64 to 1 selector
X-axis symmetric adjustment	XSG		The voltage of VINP12/VINN12 is selected by the 2 to 1 selector
			The voltage of VINP0/VINN0 is selected by the 2 to 1 selector
Micro adjustment	GLP[1:0]	GLN[1:0]	The voltage of grayscale number from 1 to 254 is adjusted by the variable resistor
	PKP0[5:0]	PKN0[5:0]	The voltage of grayscale number 1 is selected by the 64 to 1 selector
	PKP1[5:0]	PKN1[5:0]	The voltage of grayscale number 5 is selected by the 64 to 1 selector
	PKP2[5:0]	PKN2[5:0]	The voltage of grayscale number 11 is selected by the 64 to 1 selector
	PKP3[5:0]	PKN3[5:0]	The voltage of grayscale number 55 is selected by the 64 to 1 selector
	PKP4[5:0]	PKN4[5:0]	The voltage of grayscale number 95 is selected by the 64 to 1 selector
	PKP5[5:0]	PKN5[5:0]	The voltage of grayscale number VC (middle voltage between v<127> and V<128>) is selected by the 64 to 1 selector
	PKP6[5:0]	PKN6[5:0]	The voltage of grayscale number 160 is selected by the 64 to 1 selector
	PKP7[5:0]	PKN7[5:0]	The voltage of grayscale number 200 is selected by the 64 to 1 selector
	PKP8[5:0]	PKN8[5:0]	The voltage of grayscale number 244 is selected by the 64 to 1 selector
	PKP9[5:0]	PKN9[5:0]	The voltage of grayscale number 250 is selected by the 64 to 1 selector
	PKP10[5:0]	PKN10[5:0]	The voltage of grayscale number 254 is selected by the 64 to 1 selector
	GSRP0[3:0]	GSRN0[3:0]	The register is used to select one among the grayscale numbers 4 to 7
	GSRP1[3:0]	GSRN1[3:0]	The register is used to select one among the grayscale numbers 54 to 57
	GSRP2[3:0]	GSRN2[3:0]	The register is used to select one among the grayscale numbers 199 to 202
	GSRP3[3:0]	GSRN3[3:0]	The register is used to select one among the grayscale numbers 249 to 252

4.2.6. Resistor Ladder Network / Selector

This block outputs the reference voltage of the grayscale voltage. There are three ladder resistors including the 64 to 1 selector selecting voltage generated by the ladder resistance voltage. Also, there are pins that connect to the external volume resistor. In addition, it allows compensating the dispersion of length between one panel and another.

4.2.6.1. Resistor ladder network 1 / selector

There are 2 adjustments that are for the reference / amplitude adjustment (RFP(N)/ OSP(N)) and micro adjustment (PKP(N)). The voltage level is set by the reference / amplitude adjustment registers and micro adjustments as below.

Table 61. Amplitude adjustment

Register value RFP(N) [5:0]	Selected voltage VTOP	Formula of VTOP
000000	VRH0	(320R/320R) * (GVDD-VGS) + VGS
000001	VRH1	(318R/320R) * (GVDD-VGS) + VGS
000010	VRH2	(316R/320R) * (GVDD-VGS) + VGS
000011	VRH3	(314R/320R) * (GVDD-VGS) + VGS
000100	VRH4	(312R/320R) * (GVDD-VGS) + VGS
000101	VRH5	(310R/320R) * (GVDD-VGS) + VGS
000110	VRH6	(308R/320R) * (GVDD-VGS) + VGS
000111	VRH7	(306R/320R) * (GVDD-VGS) + VGS
001000	VRH8	(304R/320R) * (GVDD-VGS) + VGS
001001	VRH9	(302R/320R) * (GVDD-VGS) + VGS
001010	VRH10	(300R/320R) * (GVDD-VGS) + VGS
001011	VRH11	(298R/320R) * (GVDD-VGS) + VGS
001100	VRH12	(296R/320R) * (GVDD-VGS) + VGS
001101	VRH13	(294R/320R) * (GVDD-VGS) + VGS
001110	VRH14	(292R/320R) * (GVDD-VGS) + VGS
001111	VRH15	(290R/320R) * (GVDD-VGS) + VGS
010000	VRH16	(288R/320R) * (GVDD-VGS) + VGS
010001	VRH17	(286R/320R) * (GVDD-VGS) + VGS
010010	VRH18	(284R/320R) * (GVDD-VGS) + VGS
010011	VRH19	(282R/320R) * (GVDD-VGS) + VGS
010100	VRH20	(280R/320R) * (GVDD-VGS) + VGS
010101	VRH21	(278R/320R) * (GVDD-VGS) + VGS
010110	VRH22	(276R/320R) * (GVDD-VGS) + VGS
010111	VRH23	(274R/320R) * (GVDD-VGS) + VGS
011000	VRH24	(272R/320R) * (GVDD-VGS) + VGS
011001	VRH25	(270R/320R) * (GVDD-VGS) + VGS
011010	VRH26	(268R/320R) * (GVDD-VGS) + VGS
011011	VRH27	(266R/320R) * (GVDD-VGS) + VGS
011100	VRH28	(264R/320R) * (GVDD-VGS) + VGS
011101	VRH29	(262R/320R) * (GVDD-VGS) + VGS
011110	VRH30	(260R/320R) * (GVDD-VGS) + VGS
011111	VRH31	(258R/320R) * (GVDD-VGS) + VGS
100000	VRH32	(256R/320R) * (GVDD-VGS) + VGS
100001	VRH33	(254R/320R) * (GVDD-VGS) + VGS
100010	VRH34	(252R/320R) * (GVDD-VGS) + VGS
100011	VRH35	(250R/320R) * (GVDD-VGS) + VGS

Table 62. Amplitude adjustment(continued)

Register value RFP(N) [5:0]	Selected voltage VTOP	Formula of VTOP
100100	VRH36	(248R/320R) * (GVDD-VGS) + VGS
100101	VRH37	(246R/320R) * (GVDD-VGS) + VGS
100110	VRH38	(244R/320R) * (GVDD-VGS) + VGS
100111	VRH39	(242R/320R) * (GVDD-VGS) + VGS
101000	VRH40	(240R/320R) * (GVDD-VGS) + VGS
101001	VRH41	(238R/320R) * (GVDD-VGS) + VGS
101010	VRH42	(236R/320R) * (GVDD-VGS) + VGS
101011	VRH43	(234R/320R) * (GVDD-VGS) + VGS
101100	VRH44	(232R/320R) * (GVDD-VGS) + VGS
101101	VRH45	(230R/320R) * (GVDD-VGS) + VGS
101110	VRH46	(228R/320R) * (GVDD-VGS) + VGS
101111	VRH47	(226R/320R) * (GVDD-VGS) + VGS
110000	VRH48	(224R/320R) * (GVDD-VGS) + VGS
110001	VRH49	(222R/320R) * (GVDD-VGS) + VGS
110010	VRH50	(220R/320R) * (GVDD-VGS) + VGS
110011	VRH51	(218R/320R) * (GVDD-VGS) + VGS
110100	VRH52	(216R/320R) * (GVDD-VGS) + VGS
110101	VRH53	(214R/320R) * (GVDD-VGS) + VGS
110110	VRH54	(212R/320R) * (GVDD-VGS) + VGS
110111	VRH55	(210R/320R) * (GVDD-VGS) + VGS
111000	VRH56	(208R/320R) * (GVDD-VGS) + VGS
111001	VRH57	(206R/320R) * (GVDD-VGS) + VGS
111010	VRH58	(204R/320R) * (GVDD-VGS) + VGS
111011	VRH59	(202R/320R) * (GVDD-VGS) + VGS
111100	VRH60	(200R/320R) * (GVDD-VGS) + VGS
111101	VRH61	(198R/320R) * (GVDD-VGS) + VGS
111110	VRH62	(196R/320R) * (GVDD-VGS) + VGS
111111	VRH63	(194R/320R) * (GVDD-VGS) + VGS

Table 63. Reference adjustment

Register value OSP(N) [5:0]	Selected voltage VBOTTOM	Formula of VBOTTOM
000000	VRL0	(16R/320R) * (GVDD-VGS) + VGS
000001	VRL1	(18R/320R) * (GVDD-VGS) + VGS
000010	VRL2	(20R/320R) * (GVDD-VGS) + VGS
000011	VRL3	(22R/320R) * (GVDD-VGS) + VGS
000100	VRL4	(24R/320R) * (GVDD-VGS) + VGS
000101	VRL5	(26R/320R) * (GVDD-VGS) + VGS
000110	VRL6	(28R/320R) * (GVDD-VGS) + VGS
000111	VRL7	(30R/320R) * (GVDD-VGS) + VGS
001000	VRL8	(32R/320R) * (GVDD-VGS) + VGS
001001	VRL9	(34R/320R) * (GVDD-VGS) + VGS
001010	VRL10	(36R/320R) * (GVDD-VGS) + VGS
001011	VRL11	(38R/320R) * (GVDD-VGS) + VGS
001100	VRL12	(40R/320R) * (GVDD-VGS) + VGS
001101	VRL13	(42R/320R) * (GVDD-VGS) + VGS
001110	VRL14	(44R/320R) * (GVDD-VGS) + VGS
001111	VRL15	(46R/320R) * (GVDD-VGS) + VGS
010000	VRL16	(48R/320R) * (GVDD-VGS) + VGS
010001	VRL17	(50R/320R) * (GVDD-VGS) + VGS
010010	VRL18	(52R/320R) * (GVDD-VGS) + VGS
010011	VRL19	(54R/320R) * (GVDD-VGS) + VGS
010100	VRL20	(56R/320R) * (GVDD-VGS) + VGS
010101	VRL21	(58R/320R) * (GVDD-VGS) + VGS
010110	VRL22	(60R/320R) * (GVDD-VGS) + VGS
010111	VRL23	(62R/320R) * (GVDD-VGS) + VGS
011000	VRL24	(64R/320R) * (GVDD-VGS) + VGS
011001	VRL25	(66R/320R) * (GVDD-VGS) + VGS
011010	VRL26	(68R/320R) * (GVDD-VGS) + VGS
011011	VRL27	(70R/320R) * (GVDD-VGS) + VGS
011100	VRL28	(72R/320R) * (GVDD-VGS) + VGS
011101	VRL29	(74R/320R) * (GVDD-VGS) + VGS
011110	VRL30	(76R/320R) * (GVDD-VGS) + VGS
011111	VRL31	(78R/320R) * (GVDD-VGS) + VGS
100000	VRL32	(80R/320R) * (GVDD-VGS) + VGS
100001	VRL33	(82R/320R) * (GVDD-VGS) + VGS
100010	VRL34	(84R/320R) * (GVDD-VGS) + VGS
100011	VRL35	(86R/320R) * (GVDD-VGS) + VGS

Table 64. Reference adjustment (continued)

Register value OSP(N) [5:0]	Selected voltage VBOTTOM	Formula of VBOTTOM
100100	VRL36	(88R/320R) * (GVDD-VGS) + VGS
100101	VRL37	(90R/320R) * (GVDD-VGS) + VGS
100110	VRL38	(92R/320R) * (GVDD-VGS) + VGS
100111	VRL39	(94R/320R) * (GVDD-VGS) + VGS
101000	VRL40	(96R/320R) * (GVDD-VGS) + VGS
101001	VRL41	(98R/320R) * (GVDD-VGS) + VGS
101010	VRL42	(100R/320R) * (GVDD-VGS) + VGS
101011	VRL43	(102R/320R) * (GVDD-VGS) + VGS
101100	VRL44	(104R/320R) * (GVDD-VGS) + VGS
101101	VRL45	(106R/320R) * (GVDD-VGS) + VGS
101110	VRL46	(108R/320R) * (GVDD-VGS) + VGS
101111	VRL47	(110R/320R) * (GVDD-VGS) + VGS
110000	VRL48	(112R/320R) * (GVDD-VGS) + VGS
110001	VRL49	(114R/320R) * (GVDD-VGS) + VGS
110010	VRL50	(116R/320R) * (GVDD-VGS) + VGS
110011	VRL51	(118R/320R) * (GVDD-VGS) + VGS
110100	VRL52	(120R/320R) * (GVDD-VGS) + VGS
110101	VRL53	(122R/320R) * (GVDD-VGS) + VGS
110110	VRL54	(124R/320R) * (GVDD-VGS) + VGS
110111	VRL55	(126R/320R) * (GVDD-VGS) + VGS
111000	VRL56	(128R/320R) * (GVDD-VGS) + VGS
111001	VRL57	(130R/320R) * (GVDD-VGS) + VGS
111010	VRL58	(132R/320R) * (GVDD-VGS) + VGS
111011	VRL59	(134R/320R) * (GVDD-VGS) + VGS
111100	VRL60	(136R/320R) * (GVDD-VGS) + VGS
111101	VRL61	(138R/320R) * (GVDD-VGS) + VGS
111110	VRL62	(140R/320R) * (GVDD-VGS) + VGS
111111	VRL63	(142R/320R) * (GVDD-VGS) + VGS

4.2.6.2. Resistor ladder network 2 / selector

In the 64-to-1 selector, the voltage level must be selected by the given ladder resistance and the micro-adjustment register and output the nine types of the reference voltage, VIN1 to VIN11.

Following figure explains the relationship between the micro-adjustment register and the selected voltage

Table 65. Relationship between micro-adjustment register and selected voltage

Register value	Selected voltage										
PKP(N) [5:0]	VINP (N)1	VINP (N)2	VINP (N)3	VINP (N)4	VINP (N)5	VINP (N)6	VINP (N)7	VINP (N)8	VINP (N)9	VINP (N)10	VINP (N)11
000000	VRC0	VRC5	VRC8	VRC31	VRC44	VRC50	VRC130	VRC156	VRC225	VRC234	VRC238
000001	VRC1	VRC6	VRC9	VRC32	VRC45	VRC51	VRC129	VRC155	VRC224	VRC233	VRC237
000010	VRC2	VRC7	VRC10	VRC33	VRC46	VRC52	VRC128	VRC154	VRC223	VRC232	VRC236
000011	VRC3	VRC8	VRC11	VRC34	VRC47	VRC53	VRC127	VRC153	VRC222	VRC231	VRC235
000100	VRC4	VRC9	VRC12	VRC35	VRC48	VRC54	VRC126	VRC152	VRC221	VRC230	VRC234
000101	VRC5	VRC10	VRC13	VRC36	VRC49	VRC55	VRC125	VRC151	VRC220	VRC229	VRC233
000110	VRC6	VRC11	VRC14	VRC37	VRC50	VRC56	VRC124	VRC150	VRC219	VRC228	VRC232
000111	VRC7	VRC12	VRC15	VRC38	VRC51	VRC57	VRC123	VRC149	VRC218	VRC227	VRC231
001000	VRC8	VRC13	VRC16	VRC39	VRC52	VRC58	VRC122	VRC148	VRC217	VRC226	VRC230
001001	VRC9	VRC14	VRC17	VRC40	VRC53	VRC59	VRC121	VRC147	VRC216	VRC225	VRC229
001010	VRC10	VRC15	VRC18	VRC41	VRC54	VRC60	VRC120	VRC146	VRC215	VRC224	VRC228
001011	VRC11	VRC16	VRC19	VRC42	VRC55	VRC61	VRC119	VRC145	VRC214	VRC223	VRC227
001100	VRC12	VRC17	VRC20	VRC43	VRC56	VRC62	VRC118	VRC144	VRC213	VRC222	VRC226
001101	VRC13	VRC18	VRC21	VRC44	VRC57	VRC63	VRC117	VRC143	VRC212	VRC221	VRC225
001110	VRC14	VRC19	VRC22	VRC45	VRC58	VRC64	VRC116	VRC142	VRC211	VRC220	VRC224
001111	VRC15	VRC20	VRC23	VRC46	VRC59	VRC65	VRC115	VRC141	VRC210	VRC219	VRC223
010000	VRC16	VRC21	VRC24	VRC47	VRC60	VRC66	VRC114	VRC140	VRC209	VRC218	VRC222
010001	VRC17	VRC22	VRC25	VRC48	VRC61	VRC67	VRC113	VRC139	VRC208	VRC217	VRC221
010010	VRC18	VRC23	VRC26	VRC49	VRC62	VRC68	VRC112	VRC138	VRC207	VRC216	VRC220
010011	VRC19	VRC24	VRC27	VRC50	VRC63	VRC69	VRC111	VRC137	VRC206	VRC215	VRC219
010100	VRC20	VRC25	VRC28	VRC51	VRC64	VRC70	VRC110	VRC136	VRC205	VRC214	VRC218
010101	VRC21	VRC26	VRC29	VRC52	VRC65	VRC71	VRC109	VRC135	VRC204	VRC213	VRC217
010110	VRC22	VRC27	VRC30	VRC53	VRC66	VRC72	VRC108	VRC134	VRC203	VRC212	VRC216
010111	VRC23	VRC28	VRC31	VRC54	VRC67	VRC73	VRC107	VRC133	VRC202	VRC211	VRC215
011000	VRC24	VRC29	VRC32	VRC55	VRC68	VRC74	VRC106	VRC132	VRC201	VRC210	VRC214
011001	VRC25	VRC30	VRC33	VRC56	VRC69	VRC75	VRC105	VRC131	VRC200	VRC209	VRC213
011010	VRC26	VRC31	VRC34	VRC57	VRC70	VRC76	VRC104	VRC130	VRC199	VRC208	VRC212

Table 66. Relationship between micro-adjustment register and selected voltage(continued)

Register value	Selected voltage										
PKP(N) [5:0]	VINP (N)1	VINP (N)2	VINP (N)3	VINP (N)4	VINP (N)5	VINP (N)6	VINP (N)7	VINP (N)8	VINP (N)9	VINP (N)10	VINP (N)11
011011	VRC27	VRC32	VRC35	VRC58	VRC71	VRC77	VRC103	VRC129	VRC198	VRC207	VRC211
011100	VRC28	VRC33	VRC36	VRC59	VRC72	VRC78	VRC102	VRC128	VRC197	VRC206	VRC210
011101	VRC29	VRC34	VRC37	VRC60	VRC73	VRC79	VRC101	VRC127	VRC196	VRC205	VRC209
011110	VRC30	VRC35	VRC38	VRC61	VRC74	VRC80	VRC100	VRC126	VRC195	VRC204	VRC208
011111	VRC31	VRC36	VRC39	VRC62	VRC75	VRC81	VRC99	VRC125	VRC194	VRC203	VRC207
100000	VRC32	VRC37	VRC40	VRC63	VRC76	VRC82	VRC98	VRC124	VRC193	VRC202	VRC206
100001	VRC33	VRC38	VRC41	VRC64	VRC77	VRC83	VRC97	VRC123	VRC192	VRC201	VRC205
100010	VRC34	VRC39	VRC42	VRC65	VRC78	VRC84	VRC96	VRC122	VRC191	VRC200	VRC204
100011	VRC35	VRC40	VRC43	VRC66	VRC79	VRC85	VRC95	VRC121	VRC190	VRC199	VRC203
100100	VRC36	VRC41	VRC44	VRC67	VRC80	VRC86	VRC94	VRC120	VRC189	VRC198	VRC202
100101	VRC37	VRC42	VRC45	VRC68	VRC81	VRC87	VRC93	VRC119	VRC188	VRC197	VRC201
100110	VRC38	VRC43	VRC46	VRC69	VRC82	VRC88	VRC92	VRC118	VRC187	VRC196	VRC200
100111	VRC39	VRC44	VRC47	VRC70	VRC83	VRC89	VRC91	VRC117	VRC186	VRC195	VRC199
101000	VRC40	VRC45	VRC48	VRC71	VRC84	VRC90	VRC90	VRC116	VRC185	VRC194	VRC198
101001	VRC41	VRC46	VRC49	VRC72	VRC85	VRC91	VRC89	VRC115	VRC184	VRC193	VRC197
101010	VRC42	VRC47	VRC50	VRC73	VRC86	VRC92	VRC88	VRC114	VRC183	VRC192	VRC196
101011	VRC43	VRC48	VRC51	VRC74	VRC87	VRC93	VRC87	VRC113	VRC182	VRC191	VRC195
101100	VRC44	VRC49	VRC52	VRC75	VRC88	VRC94	VRC86	VRC112	VRC181	VRC190	VRC194
101101	VRC45	VRC50	VRC53	VRC76	VRC89	VRC95	VRC85	VRC111	VRC180	VRC189	VRC193
101110	VRC46	VRC51	VRC54	VRC77	VRC90	VRC96	VRC84	VRC110	VRC179	VRC188	VRC192
101111	VRC47	VRC52	VRC55	VRC78	VRC91	VRC97	VRC83	VRC109	VRC178	VRC187	VRC191
110000	VRC48	VRC53	VRC56	VRC79	VRC92	VRC98	VRC82	VRC108	VRC177	VRC186	VRC190
110001	VRC49	VRC54	VRC57	VRC80	VRC93	VRC99	VRC81	VRC107	VRC176	VRC185	VRC189
110010	VRC50	VRC55	VRC58	VRC81	VRC94	VRC100	VRC80	VRC106	VRC175	VRC184	VRC188
110011	VRC51	VRC56	VRC59	VRC82	VRC95	VRC101	VRC79	VRC105	VRC174	VRC183	VRC187
110100	VRC52	VRC57	VRC60	VRC83	VRC96	VRC102	VRC78	VRC104	VRC173	VRC182	VRC186
110101	VRC53	VRC58	VRC61	VRC84	VRC97	VRC103	VRC77	VRC103	VRC172	VRC181	VRC185
110110	VRC54	VRC59	VRC62	VRC85	VRC98	VRC104	VRC76	VRC102	VRC171	VRC180	VRC184
110111	VRC55	VRC60	VRC63	VRC86	VRC99	VRC105	VRC75	VRC101	VRC170	VRC179	VRC183
111000	VRC56	VRC61	VRC64	VRC87	VRC100	VRC106	VRC74	VRC100	VRC169	VRC178	VRC182
111001	VRC57	VRC62	VRC65	VRC88	VRC101	VRC107	VRC73	VRC99	VRC168	VRC177	VRC181
111010	VRC58	VRC63	VRC66	VRC89	VRC102	VRC108	VRC72	VRC98	VRC167	VRC176	VRC180

Table 67. Relationship between micro-adjustment register and selected voltage(continued)

Register value	Selected voltage										
PKP(N) [5:0]	VINP (N)1	VINP (N)2	VINP (N)3	VINP (N)4	VINP (N)5	VINP (N)6	VINP (N)7	VINP (N)8	VINP (N)9	VINP (N)10	VINP (N)11
111011	VRC59	VRC64	VRC67	VRC90	VRC103	VRC109	VRC71	VRC97	VRC166	VRC175	VRC179
111100	VRC60	VRC65	VRC68	VRC91	VRC104	VRC110	VRC70	VRC96	VRC165	VRC174	VRC178
111101	VRC61	VRC66	VRC69	VRC92	VRC105	VRC111	VRC69	VRC95	VRC164	VRC173	VRC177
111110	VRC62	VRC67	VRC70	VRC93	VRC106	VRC112	VRC68	VRC94	VRC163	VRC172	VRC176
111111	VRC63	VRC68	VRC71	VRC94	VRC107	VRC113	VRC67	VRC93	VRC162	VRC171	VRC175

The grayscale levels are determined by the following formulas listed in the following equations.

Negative gamma voltages are calculated with the same equation of positive gamma voltages, but the gray scale is symmetric, which means negative V<0> is equal to positive V<255>. Rt and Ra in the below equations are determined by GL[1:0] Registers as follows.

GLP/N[1:0]=00, Rt = 220R, Ra=0

GLP/N [1:0]=01, Rt = 270R, Ra=50R

GLP/N [1:0]=10, Rt = 270R, Ra=0

GLP/N [1:0]=11, Rt = 320R, Ra=50R

4.2.7. Grayscale Levels

Table 68. Formulas for calculating gamma adjusting voltage (positive polarity) 1

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC0	((219.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “000000”	VNP1
VRC1	((219R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “000001”	
VRC2	((218.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “000010”	
VRC3	((218R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “000011”	
VRC4	((217.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “000100”	
VRC5	((217R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “000101”	
VRC6	((216.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “000110”	
VRC7	((216R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “000111”	
VRC8	((215.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “001000”	
VRC9	((215R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “001001”	
VRC10	((214.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “001010”	
VRC11	((214R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “001011”	
VRC12	((213.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “001100”	
VRC13	((213R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “001101”	
VRC14	((212.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “001110”	
VRC15	((212R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “001111”	
VRC16	((211.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “010000”	
VRC17	((211R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “010001”	
VRC18	((210.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “010010”	
VRC19	((210R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “010011”	
VRC20	((209R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “010100”	
VRC21	((208R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “010101”	
VRC22	((207R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “010110”	
VRC23	((206R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “010111”	
VRC24	((205R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “011000”	
VRC25	((204R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “011001”	
VRC26	((203R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “011010”	
VRC27	((202R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “011011”	
VRC28	((201R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “011100”	
VRC29	((200R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “011101”	
VRC30	((199R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “011110”	
VRC31	((198R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “011111”	
VRC32	((197R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “100000”	
VRC33	((196R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “100001”	
VRC34	((195R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “100010”	
VRC35	((194R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “100011”	

Table 69. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC36	((193R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “100100”	VINP1
VRC37	((192R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “100101”	
VRC38	((191R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “100110”	
VRC39	((190R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “100111”	
VRC40	((189R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “101000”	
VRC41	((188R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “101001”	
VRC42	((187R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “101010”	
VRC43	((186R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “101011”	
VRC44	((185R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “101100”	
VRC45	((184R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “101101”	
VRC46	((183R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “101110”	
VRC47	((182R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “101111”	
VRC48	((181R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “110000”	
VRC49	((180R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “110001”	
VRC50	((179R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “110010”	
VRC51	((178R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “110011”	
VRC52	((177R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “110100”	
VRC53	((176R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “110101”	
VRC54	((175R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “110110”	
VRC55	((174R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “110111”	
VRC56	((173R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “111000”	
VRC57	((172R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “111001”	
VRC58	((171R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “111010”	
VRC59	((170R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “111011”	
VRC60	((169R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “111100”	
VRC61	((168R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “111101”	
VRC62	((167R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “111110”	
VRC63	((166R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “111111”	
VRC5	((217R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “000000”	VINP2
VRC6	((216.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “000001”	
VRC7	((216R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “000010”	
VRC8	((215.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “000011”	
VRC9	((215R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “000100”	
VRC10	((214.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “000101”	
VRC11	((214R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “000110”	
VRC12	((213.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “000111”	

Table 70. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC13	((213R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “001000”	VINP2
VRC14	((212.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “001001”	
VRC15	((212R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “001010”	
VRC16	((211.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “001011”	
VRC17	((211R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “001100”	
VRC18	((210.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “001101”	
VRC19	((210R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “001110”	
VRC20	((209R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “001111”	
VRC21	((208R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “010000”	
VRC22	((207R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “010001”	
VRC23	((206R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “010010”	
VRC24	((205R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “010011”	
VRC25	((204R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “010100”	
VRC26	((203R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “010101”	
VRC27	((202R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “010110”	
VRC28	((201R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “010111”	
VRC29	((200R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “011000”	
VRC30	((199R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “011001”	
VRC31	((198R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “011010”	
VRC32	((197R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “011011”	
VRC33	((196R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “011100”	
VRC34	((195R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “011101”	
VRC35	((194R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “011110”	
VRC36	((193R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “011111”	
VRC37	((192R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “100000”	
VRC38	((191R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “100001”	
VRC39	((190R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “100010”	
VRC40	((189R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “100011”	
VRC41	((188R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “100100”	
VRC42	((187R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “100101”	
VRC43	((186R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “100110”	
VRC44	((185R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “100111”	
VRC45	((184R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “101000”	
VRC46	((183R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “101001”	
VRC47	((182R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “101010”	
VRC48	((181R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “101011”	

Table 71. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC49	((180R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “101100”	VINP2
VRC50	((179R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “101101”	
VRC51	((178R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “101110”	
VRC52	((177R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “101111”	
VRC53	((176R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “110000”	
VRC54	((175R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “110001”	
VRC55	((174R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “110010”	
VRC56	((173R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “110011”	
VRC57	((172R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “110100”	
VRC58	((171R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “110101”	
VRC59	((170R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “110110”	
VRC60	((169R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “110111”	
VRC61	((168R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “111000”	
VRC62	((167R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “111001”	
VRC63	((166R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “111010”	
VRC64	((165R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “111011”	
VRC65	((164R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “111100”	
VRC66	((163R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “111101”	
VRC67	((162R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “111110”	
VRC68	((161R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “111111”	
VRC8	((215.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “000000”	VINP3
VRC9	((215R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “000001”	
VRC10	((214.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “000010”	
VRC11	((214R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “000011”	
VRC12	((213.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “000100”	
VRC13	((213R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “000101”	
VRC14	((212.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “000110”	
VRC15	((212R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “000111”	
VRC16	((211.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “001000”	
VRC17	((211R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “001001”	
VRC18	((210.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “001010”	
VRC19	((210R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “001011”	
VRC20	((209R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “001100”	
VRC21	((208R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “001101”	
VRC22	((207R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “001110”	
VRC23	((206R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “001111”	

Table 72. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC24	((205R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “010000”	VINP3
VRC25	((204R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “010001”	
VRC26	((203R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “010010”	
VRC27	((202R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “010011”	
VRC28	((201R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “010100”	
VRC29	((200R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “010101”	
VRC30	((199R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “010110”	
VRC31	((198R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “010111”	
VRC32	((197R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “011000”	
VRC33	((196R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “011001”	
VRC34	((195R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “011010”	
VRC35	((194R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “011011”	
VRC36	((193R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “011100”	
VRC37	((192R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “011101”	
VRC38	((191R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “011110”	
VRC39	((190R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “011111”	
VRC40	((189R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “100000”	
VRC41	((188R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “100001”	
VRC42	((187R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “100010”	
VRC43	((186R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “100011”	
VRC44	((185R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “100100”	
VRC45	((184R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “100101”	
VRC46	((183R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “100110”	
VRC47	((182R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “100111”	
VRC48	((181R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “101000”	
VRC49	((180R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “101001”	
VRC50	((179R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “101010”	
VRC51	((178R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “101011”	
VRC52	((177R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “101100”	
VRC53	((176R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “101101”	
VRC54	((175R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “101110”	
VRC55	((174R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “101111”	
VRC56	((173R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “110000”	
VRC57	((172R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “110001”	
VRC58	((171R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “110010”	
VRC59	((170R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “110011”	

Table 73. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC60	((169R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “110100”	VINP3
VRC61	((168R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “110101”	
VRC62	((167R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “110110”	
VRC63	((166R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “110111”	
VRC64	((165R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “111000”	
VRC65	((164R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “111001”	
VRC66	((163R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “111010”	
VRC67	((162R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “111011”	
VRC68	((161R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “111100”	
VRC69	((160R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “111101”	
VRC70	((159R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “111110”	
VRC71	((158R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “111111”	
VRC31	((198R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “000000”	VINP4
VRC32	((197R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “000001”	
VRC33	((196R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “000010”	
VRC34	((195R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “000011”	
VRC35	((194R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “000100”	
VRC36	((193R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “000101”	
VRC37	((192R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “000110”	
VRC38	((191R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “000111”	
VRC39	((190R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “001000”	
VRC40	((189R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “001001”	
VRC41	((188R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “001010”	
VRC42	((187R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “001011”	
VRC43	((186R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “001100”	
VRC44	((185R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “001101”	
VRC45	((184R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “001110”	
VRC46	((183R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “001111”	
VRC47	((182R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “010000”	
VRC48	((181R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “010001”	
VRC49	((180R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “010010”	
VRC50	((179R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “010011”	
VRC51	((178R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “010100”	
VRC52	((177R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “010101”	
VRC53	((176R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “010110”	
VRC54	((175R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “010111”	

Table 74. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC55	((174R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “011000”	VINP4
VRC56	((173R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “011001”	
VRC57	((172R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “011010”	
VRC58	((171R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “011011”	
VRC59	((170R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “011100”	
VRC60	((169R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “011101”	
VRC61	((168R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “011110”	
VRC62	((167R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “011111”	
VRC63	((166R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “100000”	
VRC64	((165R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “100001”	
VRC65	((164R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “100010”	
VRC66	((163R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “100011”	
VRC67	((162R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “100100”	
VRC68	((161R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “100101”	
VRC69	((160R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “100110”	
VRC70	((159R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “100111”	
VRC71	((158R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “101000”	
VRC72	((157R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “101001”	
VRC73	((156R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “101010”	
VRC74	((155R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “101011”	
VRC75	((154R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “101100”	
VRC76	((153R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “101101”	
VRC77	((152R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “101110”	
VRC78	((151R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “101111”	
VRC79	((150R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “110000”	
VRC80	((149R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “110001”	
VRC81	((148R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “110010”	
VRC82	((147R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “110011”	
VRC83	((146R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “110100”	
VRC84	((145R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “110101”	
VRC85	((144R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “110110”	
VRC86	((143R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “110111”	
VRC87	((142R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “111000”	
VRC88	((141R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “111001”	
VRC89	((140R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “111010”	
VRC90	((139R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “111011”	

Table 75. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC91	((138R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “111100”	VINP4
VRC92	((137R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “111101”	
VRC93	((136R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “111110”	
VRC94	((135R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “111111”	
VRC44	((185R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “000000”	VINP5
VRC45	((184R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “000001”	
VRC46	((183R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “000010”	
VRC47	((182R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “000011”	
VRC48	((181R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “000100”	
VRC49	((180R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “000101”	
VRC50	((179R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “000110”	
VRC51	((178R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “000111”	
VRC52	((177R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “001000”	
VRC53	((176R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “001001”	
VRC54	((175R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “001010”	
VRC55	((174R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “001011”	
VRC56	((173R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “001100”	
VRC57	((172R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “001101”	
VRC58	((171R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “001110”	
VRC59	((170R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “001111”	
VRC60	((169R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “010000”	
VRC61	((168R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “010001”	
VRC62	((167R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “010010”	
VRC63	((166R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “010011”	
VRC64	((165R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “010100”	
VRC65	((164R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “010101”	
VRC66	((163R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “010110”	
VRC67	((162R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “010111”	
VRC68	((161R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “011000”	
VRC69	((160R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “011001”	
VRC70	((159R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “011010”	
VRC71	((158R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “011011”	
VRC72	((157R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “011100”	
VRC73	((156R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “011101”	
VRC74	((155R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “011110”	
VRC75	((154R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “011111”	

Table 76. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC76	((153R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “100000”	VINP5
VRC77	((152R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “100001”	
VRC78	((151R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “100010”	
VRC79	((150R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “100011”	
VRC80	((149R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “100100”	
VRC81	((148R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “100101”	
VRC82	((147R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “100110”	
VRC83	((146R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “100111”	
VRC84	((145R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “101000”	
VRC85	((144R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “101001”	
VRC86	((143R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “101010”	
VRC87	((142R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “101011”	
VRC88	((141R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “101100”	
VRC89	((140R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “101101”	
VRC90	((139R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “101110”	
VRC91	((138R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “101111”	
VRC92	((137R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “110000”	
VRC93	((136R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “110001”	
VRC94	((135R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “110010”	
VRC95	((134R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “110011”	
VRC96	((133R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “110100”	
VRC97	((132R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “110101”	
VRC98	((131R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “110110”	
VRC99	((130R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “110111”	
VRC100	((129R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “111000”	
VRC101	((128R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “111001”	
VRC102	((127R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “111010”	
VRC103	((126R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “111011”	
VRC104	((125R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “111100”	
VRC105	((124R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “111101”	
VRC106	((123R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “111110”	
VRC107	((122R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “111111”	
VRC50	((179R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “000000”	VINP6
VRC51	((178R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “000001”	
VRC52	((177R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “000010”	
VRC53	((176R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “000011”	

Table 77. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC54	((175R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “000100”	VINP6
VRC55	((174R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “000101”	
VRC56	((173R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “000110”	
VRC57	((172R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “000111”	
VRC58	((171R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “001000”	
VRC59	((170R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “001001”	
VRC60	((169R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “001010”	
VRC61	((168R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “001011”	
VRC62	((167R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “001100”	
VRC63	((166R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “001101”	
VRC64	((165R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “001110”	
VRC65	((164R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “001111”	
VRC66	((163R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “010000”	
VRC67	((162R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “010001”	
VRC68	((161R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “010010”	
VRC69	((160R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “010011”	
VRC70	((159R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “010100”	
VRC71	((158R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “010101”	
VRC72	((157R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “010110”	
VRC73	((156R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “010111”	
VRC74	((155R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “011000”	
VRC75	((154R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “011001”	
VRC76	((153R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “011010”	
VRC77	((152R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “011011”	
VRC78	((151R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “011100”	
VRC79	((150R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “011101”	
VRC80	((149R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “011110”	
VRC81	((148R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “011111”	
VRC82	((147R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “100000”	
VRC83	((146R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “100001”	
VRC84	((145R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “100010”	
VRC85	((144R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “100011”	
VRC86	((143R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “100100”	
VRC87	((142R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “100101”	
VRC88	((141R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “100110”	
VRC89	((140R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “100111”	

Table 78. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC90	((139R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “101000”	VINP6
VRC91	((138R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “101001”	
VRC92	((137R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “101010”	
VRC93	((136R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “101011”	
VRC94	((135R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “101100”	
VRC95	((134R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “101101”	
VRC96	((133R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “101110”	
VRC97	((132R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “101111”	
VRC98	((131R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “110000”	
VRC99	((130R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “110001”	
VRC100	((129R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “110010”	
VRC101	((128R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “110011”	
VRC102	((127R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “110100”	
VRC103	((126R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “110101”	
VRC104	((125R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “110110”	
VRC105	((124R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “110111”	
VRC106	((123R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “111000”	
VRC107	((122R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “111001”	
VRC108	((121R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “111010”	
VRC109	((120R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “111011”	
VRC110	((119R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “111100”	
VRC111	((118R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “111101”	
VRC112	((117R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “111110”	
VRC113	((116R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “111111”	
VRC130	((99R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “000000”	VINP7
VRC129	((100R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “000001”	
VRC128	((101R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “000010”	
VRC127	((102R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “000011”	
VRC126	((103R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “000100”	
VRC125	((104R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “000101”	
VRC124	((105R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “000110”	
VRC123	((106R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “000111”	
VRC122	((107R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “001000”	
VRC121	((108R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “001001”	
VRC120	((109R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “001010”	
VRC119	((110R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “001011”	

Table 79. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC118	((111R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “001100”	VINP7
VRC117	((112R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “001101”	
VRC116	((113R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “001110”	
VRC115	((114R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “001111”	
VRC114	((115R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “010000”	
VRC113	((116R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “010001”	
VRC112	((117R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “010010”	
VRC111	((118R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “010011”	
VRC110	((119R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “010100”	
VRC109	((120R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “010101”	
VRC108	((121R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “010110”	
VRC107	((122R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “010111”	
VRC106	((123R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “011000”	
VRC105	((124R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “011001”	
VRC104	((125R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “011010”	
VRC103	((126R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “011011”	
VRC102	((127R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “011100”	
VRC101	((128R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “011101”	
VRC100	((129R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “011110”	
VRC99	((130R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “011111”	
VRC98	((131R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “100000”	
VRC97	((132R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “100001”	
VRC96	((133R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “100010”	
VRC95	((134R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “100011”	
VRC94	((135R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “100100”	
VRC93	((136R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “100101”	
VRC92	((137R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “100110”	
VRC91	((138R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “100111”	
VRC90	((139R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “101000”	
VRC89	((140R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “101001”	
VRC88	((141R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “101010”	
VRC87	((142R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “101011”	
VRC86	((143R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “101100”	
VRC85	((144R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “101101”	
VRC84	((145R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “101110”	
VRC83	((146R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “101111”	

Table 80. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC82	((147R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “110000”	VINP7
VRC81	((148R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “110001”	
VRC80	((149R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “110010”	
VRC79	((150R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “110011”	
VRC78	((151R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “110100”	
VRC77	((152R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “110101”	
VRC76	((153R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “110110”	
VRC75	((154R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “110111”	
VRC74	((155R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “111000”	
VRC73	((156R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “111001”	
VRC72	((157R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “111010”	
VRC71	((158R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “111011”	
VRC70	((159R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “111100”	
VRC69	((160R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “111101”	
VRC68	((161R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “111110”	
VRC67	((162R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “111111”	
VRC156	((73R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “000000”	VINP8
VRC155	((74R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “000001”	
VRC154	((75R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “000010”	
VRC153	((76R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “000011”	
VRC152	((77R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “000100”	
VRC151	((78R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “000101”	
VRC150	((79R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “000110”	
VRC149	((80R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “000111”	
VRC148	((81R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “001000”	
VRC147	((82R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “001001”	
VRC146	((83R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “001010”	
VRC145	((84R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “001011”	
VRC144	((85R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “001100”	
VRC143	((86R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “001101”	
VRC142	((87R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “001110”	
VRC141	((88R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “001111”	
VRC140	((89R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “010000”	
VRC139	((90R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “010001”	
VRC138	((91R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “010010”	
VRC137	((92R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “010011”	

Table 81. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC136	((93R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “010100”	VINP8
VRC135	((94R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “010101”	
VRC134	((95R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “010110”	
VRC133	((96R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “010111”	
VRC132	((97R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “011000”	
VRC131	((98R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “011001”	
VRC130	((99R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “011010”	
VRC129	((100R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “011011”	
VRC128	((101R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “011100”	
VRC127	((102R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “011101”	
VRC126	((103R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “011110”	
VRC125	((104R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “011111”	
VRC124	((105R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “100000”	
VRC123	((106R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “100001”	
VRC122	((107R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “100010”	
VRC121	((108R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “100011”	
VRC120	((109R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “100100”	
VRC119	((110R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “100101”	
VRC118	((111R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “100110”	
VRC117	((112R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “100111”	
VRC116	((113R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “101000”	
VRC115	((114R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “101001”	
VRC114	((115R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “101010”	
VRC113	((116R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “101011”	
VRC112	((117R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “101100”	
VRC111	((118R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “101101”	
VRC110	((119R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “101110”	
VRC109	((120R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “101111”	
VRC108	((121R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “110000”	
VRC107	((122R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “110001”	
VRC106	((123R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “110010”	
VRC105	((124R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “110011”	
VRC104	((125R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “110100”	
VRC103	((126R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “110101”	
VRC102	((127R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “110110”	
VRC101	((128R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “110111”	

Table 82. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC100	((129R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “111000”	VINP8
VRC99	((130R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “111001”	
VRC98	((131R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “111010”	
VRC97	((132R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “111011”	
VRC96	((133R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “111100”	
VRC95	((134R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “111101”	
VRC94	((135R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “111110”	
VRC93	((136R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “111111”	
VRC225	((7R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “000000”	VINP9
VRC224	((7.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “000001”	
VRC223	((8R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “000010”	
VRC222	((8.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “000011”	
VRC221	((9R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “000100”	
VRC220	((9.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “000101”	
VRC219	((10R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “000110”	
VRC218	((11R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “000111”	
VRC217	((12R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “001000”	
VRC216	((13R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “001001”	
VRC215	((14R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “001010”	
VRC214	((15R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “001011”	
VRC213	((16R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “001100”	
VRC212	((17R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “001101”	
VRC211	((18R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “001110”	
VRC210	((19R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “001111”	
VRC209	((20R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “010000”	
VRC208	((21R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “010001”	
VRC207	((22R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “010010”	
VRC206	((23R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “010011”	
VRC205	((24R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “010100”	
VRC204	((25R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “010101”	
VRC203	((26R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “010110”	
VRC202	((27R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “010111”	
VRC201	((28R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “011000”	
VRC200	((29R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “011001”	
VRC199	((30R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “011010”	
VRC198	((31R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “011011”	

Table 83. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC197	((32R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “011100”	VINP9
VRC196	((33R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “011101”	
VRC195	((34R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “011110”	
VRC194	((35R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “011111”	
VRC193	((36R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “100000”	
VRC192	((37R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “100001”	
VRC191	((38R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “100010”	
VRC190	((39R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “100011”	
VRC189	((40R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “100100”	
VRC188	((41R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “100101”	
VRC187	((42R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “100110”	
VRC186	((43R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “100111”	
VRC185	((44R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “101000”	
VRC184	((45R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “101001”	
VRC183	((46R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “101010”	
VRC182	((47R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “101011”	
VRC181	((48R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “101100”	
VRC180	((49R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “101101”	
VRC179	((50R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “101110”	
VRC178	((51R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “101111”	
VRC177	((52R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “110000”	
VRC176	((53R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “110001”	
VRC175	((54R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “110010”	
VRC174	((55R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “110011”	
VRC173	((56R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “110100”	
VRC172	((57R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “110101”	
VRC171	((58R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “110110”	
VRC170	((59R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “110111”	
VRC169	((60R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “111000”	
VRC168	((61R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “111001”	
VRC167	((62R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “111010”	
VRC166	((63R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “111011”	
VRC165	((64R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “111100”	
VRC164	((65R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “111101”	
VRC163	((66R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “111110”	
VRC162	((67R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “111111”	

Table 84. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC234	((2.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “000000”	VNP10
VRC233	((3R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “000001”	
VRC232	((3.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “000010”	
VRC231	((4R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “000011”	
VRC230	((4.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “000100”	
VRC229	((5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “000101”	
VRC228	((5.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “000110”	
VRC227	((6R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “000111”	
VRC226	((6.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “001000”	
VRC225	((7R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “001001”	
VRC224	((7.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “001010”	
VRC223	((8R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “001011”	
VRC222	((8.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “001100”	
VRC221	((9R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “001101”	
VRC220	((9.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “001110”	
VRC219	((10R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “001111”	
VRC218	((11R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “010000”	
VRC217	((12R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “010001”	
VRC216	((13R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “010010”	
VRC215	((14R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “010011”	
VRC214	((15R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “010100”	
VRC213	((16R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “010101”	
VRC212	((17R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “010110”	
VRC211	((18R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “010111”	
VRC210	((19R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “011000”	
VRC209	((20R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “011001”	
VRC208	((21R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “011010”	
VRC207	((22R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “011011”	
VRC206	((23R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “011100”	
VRC205	((24R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “011101”	
VRC204	((25R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “011110”	
VRC203	((26R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “011111”	
VRC202	((27R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “100000”	
VRC201	((28R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “100001”	
VRC200	((29R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “100010”	
VRC199	((30R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “100011”	

Table 85. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC198	((31R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “100100”	VINP10
VRC197	((32R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “100101”	
VRC196	((33R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “100110”	
VRC195	((34R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “100111”	
VRC194	((35R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “101000”	
VRC193	((36R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “101001”	
VRC192	((37R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “101010”	
VRC191	((38R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “101011”	
VRC190	((39R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “101100”	
VRC189	((40R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “101101”	
VRC188	((41R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “101110”	
VRC187	((42R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “101111”	
VRC186	((43R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “110000”	
VRC185	((44R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “110001”	
VRC184	((45R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “110010”	
VRC183	((46R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “110011”	
VRC182	((47R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “110100”	
VRC181	((48R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “110101”	
VRC180	((49R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “110110”	
VRC179	((50R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “110111”	
VRC178	((51R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “111000”	
VRC177	((52R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “111001”	
VRC176	((53R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “111010”	
VRC175	((54R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “111011”	
VRC174	((55R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “111100”	
VRC173	((56R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “111101”	
VRC172	((57R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “111110”	
VRC171	((58R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “111111”	
VRC238	((0.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “000000”	VINP11
VRC237	((1R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “000001”	
VRC236	((1.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “000010”	
VRC235	((2R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “000011”	
VRC234	((2.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “000100”	
VRC233	((3R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “000101”	
VRC232	((3.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “000110”	
VRC231	((4R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “000111”	

Table 86. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC230	((4.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “001000”	VINP11
VRC229	((5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “001001”	
VRC228	((5.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “001010”	
VRC227	((6R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “001011”	
VRC226	((6.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “001100”	
VRC225	((7R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “001101”	
VRC224	((7.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “001110”	
VRC223	((8R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “001111”	
VRC222	((8.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “010000”	
VRC221	((9R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “010001”	
VRC220	((9.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “010010”	
VRC219	((10R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “010011”	
VRC218	((11R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “010100”	
VRC217	((12R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “010101”	
VRC216	((13R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “010110”	
VRC215	((14R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “010111”	
VRC214	((15R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “011000”	
VRC213	((16R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “011001”	
VRC212	((17R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “011010”	
VRC211	((18R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “011011”	
VRC210	((19R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “011100”	
VRC209	((20R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “011101”	
VRC208	((21R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “011110”	
VRC207	((22R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “011111”	
VRC206	((23R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “100000”	
VRC205	((24R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “100001”	
VRC204	((25R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “100010”	
VRC203	((26R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “100011”	
VRC202	((27R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “100100”	
VRC201	((28R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “100101”	
VRC200	((29R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “100110”	
VRC199	((30R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “100111”	
VRC198	((31R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “101000”	
VRC197	((32R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “101001”	
VRC196	((33R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “101010”	
VRC195	((34R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “101011”	

Table 87. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC194	((35R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “101100”	VINP11
VRC193	((36R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “101101”	
VRC192	((37R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “101110”	
VRC191	((38R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “101111”	
VRC190	((39R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “110000”	
VRC189	((40R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “110001”	
VRC188	((41R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “110010”	
VRC187	((42R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “110011”	
VRC186	((43R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “110100”	
VRC185	((44R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “110101”	
VRC184	((45R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “110110”	
VRC183	((46R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “110111”	
VRC182	((47R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “111000”	
VRC181	((48R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “111001”	
VRC180	((49R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “111010”	
VRC179	((50R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “111011”	
VRC178	((51R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “111100”	
VRC177	((52R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “111101”	
VRC176	((53R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “111110”	
VRC175	((54R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “111111”	

Table 88. Formulas for calculating gamma adjusting voltage (positive polarity) 2

Grayscale Voltage	Formula			
	GSRP[3:0]			
	0001	0010	0100	1000
V0	VINP0			
V1	VINP1			
V2	V1-(V1-V4)*(2/6)	V1-(V1-V5)*(2/8.5)	V1-(V1-V6)*(2/9.5)	V1-(V1-V7)*(2/11)
V3	V1-(V1-V4)*(4/6)	V1-(V1-V5)*(4/8.5)	V1-(V1-V6)*(4/9.5)	V1-(V1-V7)*(4/11)
V4	VINP2	V1-(V1-V5)*(6/8.5)	V1-(V1-V6)*(6/9.5)	V1-(V1-V7)*(6/11)
V5	V4-(V4-V11)*(2.5/10.5)	VINP2	V1-(V1-V6)*(8.5/9.5)	V1-(V1-V7)*(8.5/11)
V6	V4-(V4-V11)*(3.5/10.5)	V5-(V5-V11)*(1/8)	VINP2	V1-(V1-V7)*(9.5/11)
V7	V4-(V4-V11)*(5/10.5)	V5-(V5-V11)*(2.5/8)	V6-(V6-V11)*(1.5/7)	VINP2
V8	V4-(V4-V11)*(6.5/10.5)	V5-(V5-V11)*(4/8)	V6-(V6-V11)*(3/7)	V7-(V7-V11)*(1.5/5.5)
V9	V4-(V4-V11)*(7.5/10.5)	V5-(V5-V11)*(5/8)	V6-(V6-V11)*(4/7)	V7-(V7-V11)*(2.5/5.5)
V10	V4-(V4-V11)*(9.5/10.5)	V5-(V5-V11)*(7/8)	V6-(V6-V11)*(6/7)	V7-(V7-V11)*(4.5/5.5)
V11	VINP3			
V12	V11-(V11-V54)*(1/52.5)	V11-(V11-V55)*(1/53.5)	V11-(V11-V56)*(1/54.5)	V11-(V11-V57)*(1/56)
V13	V11-(V11-V54)*(3/52.5)	V11-(V11-V55)*(3/53.5)	V11-(V11-V56)*(3/54.5)	V11-(V11-V57)*(3/56)
V14	V11-(V11-V54)*(5/52.5)	V11-(V11-V55)*(5/53.5)	V11-(V11-V56)*(5/54.5)	V11-(V11-V57)*(5/56)
V15	V11-(V11-V54)*(6/52.5)	V11-(V11-V55)*(6/53.5)	V11-(V11-V56)*(6/54.5)	V11-(V11-V57)*(6/56)
V16	V11-(V11-V54)*(8/52.5)	V11-(V11-V55)*(8/53.5)	V11-(V11-V56)*(8/54.5)	V11-(V11-V57)*(8/56)
V17	V11-(V11-V54)*(9.5/52.5)	V11-(V11-V55)*(9.5/53.5)	V11-(V11-V56)*(9.5/54.5)	V11-(V11-V57)*(9.5/56)
V18	V11-(V11-V54)*(11.5/52.5)	V11-(V11-V55)*(11.5/53.5)	V11-(V11-V56)*(11.5/54.5)	V11-(V11-V57)*(11.5/56)
V19	V11-(V11-V54)*(12.5/52.5)	V11-(V11-V55)*(12.5/53.5)	V11-(V11-V56)*(12.5/54.5)	V11-(V11-V57)*(12.5/56)
V20	V11-(V11-V54)*(14/52.5)	V11-(V11-V55)*(14/53.5)	V11-(V11-V56)*(14/54.5)	V11-(V11-V57)*(14/56)
V21	V11-(V11-V54)*(15/52.5)	V11-(V11-V55)*(15/53.5)	V11-(V11-V56)*(15/54.5)	V11-(V11-V57)*(15/56)
V22	V11-(V11-V54)*(16/52.5)	V11-(V11-V55)*(16/53.5)	V11-(V11-V56)*(16/54.5)	V11-(V11-V57)*(16/56)
V23	V11-(V11-V54)*(17.5/52.5)	V11-(V11-V55)*(17.5/53.5)	V11-(V11-V56)*(17.5/54.5)	V11-(V11-V57)*(17.5/56)
V24	V11-(V11-V54)*(19.5/52.5)	V11-(V11-V55)*(19.5/53.5)	V11-(V11-V56)*(19.5/54.5)	V11-(V11-V57)*(19.5/56)
V25	V11-(V11-V54)*(21/52.5)	V11-(V11-V55)*(21/53.5)	V11-(V11-V56)*(21/54.5)	V11-(V11-V57)*(21/56)
V26	V11-(V11-V54)*(22/52.5)	V11-(V11-V55)*(22/53.5)	V11-(V11-V56)*(22/54.5)	V11-(V11-V57)*(22/56)
V27	V11-(V11-V54)*(23.5/52.5)	V11-(V11-V55)*(23.5/53.5)	V11-(V11-V56)*(23.5/54.5)	V11-(V11-V57)*(23.5/56)
V28	V11-(V11-V54)*(25/52.5)	V11-(V11-V55)*(25/53.5)	V11-(V11-V56)*(25/54.5)	V11-(V11-V57)*(25/56)
V29	V11-(V11-V54)*(26/52.5)	V11-(V11-V55)*(26/53.5)	V11-(V11-V56)*(26/54.5)	V11-(V11-V57)*(26/56)
V30	V11-(V11-V54)*(27/52.5)	V11-(V11-V55)*(27/53.5)	V11-(V11-V56)*(27/54.5)	V11-(V11-V57)*(27/56)
V31	V11-(V11-V54)*(29/52.5)	V11-(V11-V55)*(29/53.5)	V11-(V11-V56)*(29/54.5)	V11-(V11-V57)*(29/56)
V32	V11-(V11-V54)*(30/52.5)	V11-(V11-V55)*(30/53.5)	V11-(V11-V56)*(30/54.5)	V11-(V11-V57)*(30/56)
V33	V11-(V11-V54)*(31/52.5)	V11-(V11-V55)*(31/53.5)	V11-(V11-V56)*(31/54.5)	V11-(V11-V57)*(31/56)

Table 89. Formulas for calculating gamma adjusting voltage (positive polarity) 2 (continued)

Grayscale Voltage	Formula			
	GSRP[3:0]			
	0001	0010	0100	1000
V34	V11-(V11-V54)*(32/52.5)	V11-(V11-V55)*(32/53.5)	V11-(V11-V56)*(32/54.5)	V11-(V11-V57)*(32/56)
V35	V11-(V11-V54)*(33/52.5)	V11-(V11-V55)*(33/53.5)	V11-(V11-V56)*(33/54.5)	V11-(V11-V57)*(33/56)
V36	V11-(V11-V54)*(34/52.5)	V11-(V11-V55)*(34/53.5)	V11-(V11-V56)*(34/54.5)	V11-(V11-V57)*(34/56)
V37	V11-(V11-V54)*(35/52.5)	V11-(V11-V55)*(35/53.5)	V11-(V11-V56)*(35/54.5)	V11-(V11-V57)*(35/56)
V38	V11-(V11-V54)*(36.5/52.5)	V11-(V11-V55)*(36.5/53.5)	V11-(V11-V56)*(36.5/54.5)	V11-(V11-V57)*(36.5/56)
V39	V11-(V11-V54)*(37.5/52.5)	V11-(V11-V55)*(37.5/53.5)	V11-(V11-V56)*(37.5/54.5)	V11-(V11-V57)*(37.5/56)
V40	V11-(V11-V54)*(38.5/52.5)	V11-(V11-V55)*(38.5/53.5)	V11-(V11-V56)*(38.5/54.5)	V11-(V11-V57)*(38.5/56)
V41	V11-(V11-V54)*(39.5/52.5)	V11-(V11-V55)*(39.5/53.5)	V11-(V11-V56)*(39.5/54.5)	V11-(V11-V57)*(39.5/56)
V42	V11-(V11-V54)*(40.5/52.5)	V11-(V11-V55)*(40.5/53.5)	V11-(V11-V56)*(40.5/54.5)	V11-(V11-V57)*(40.5/56)
V43	V11-(V11-V54)*(41.5/52.5)	V11-(V11-V55)*(41.5/53.5)	V11-(V11-V56)*(41.5/54.5)	V11-(V11-V57)*(41.5/56)
V44	V11-(V11-V54)*(42.5/52.5)	V11-(V11-V55)*(42.5/53.5)	V11-(V11-V56)*(42.5/54.5)	V11-(V11-V57)*(42.5/56)
V45	V11-(V11-V54)*(43.5/52.5)	V11-(V11-V55)*(43.5/53.5)	V11-(V11-V56)*(43.5/54.5)	V11-(V11-V57)*(43.5/56)
V46	V11-(V11-V54)*(44.5/52.5)	V11-(V11-V55)*(44.5/53.5)	V11-(V11-V56)*(44.5/54.5)	V11-(V11-V57)*(44.5/56)
V47	V11-(V11-V54)*(45.5/52.5)	V11-(V11-V55)*(45.5/53.5)	V11-(V11-V56)*(45.5/54.5)	V11-(V11-V57)*(45.5/56)
V48	V11-(V11-V54)*(46.5/52.5)	V11-(V11-V55)*(46.5/53.5)	V11-(V11-V56)*(46.5/54.5)	V11-(V11-V57)*(46.5/56)
V49	V11-(V11-V54)*(47.5/52.5)	V11-(V11-V55)*(47.5/53.5)	V11-(V11-V56)*(47.5/54.5)	V11-(V11-V57)*(47.5/56)
V50	V11-(V11-V54)*(48.5/52.5)	V11-(V11-V55)*(48.5/53.5)	V11-(V11-V56)*(48.5/54.5)	V11-(V11-V57)*(48.5/56)
V51	V11-(V11-V54)*(49.5/52.5)	V11-(V11-V55)*(49.5/53.5)	V11-(V11-V56)*(49.5/54.5)	V11-(V11-V57)*(49.5/56)
V52	V11-(V11-V54)*(50.5/52.5)	V11-(V11-V55)*(50.5/53.5)	V11-(V11-V56)*(50.5/54.5)	V11-(V11-V57)*(50.5/56)
V53	V11-(V11-V54)*(51.5/52.5)	V11-(V11-V55)*(51.5/53.5)	V11-(V11-V56)*(51.5/54.5)	V11-(V11-V57)*(51.5/56)
V54	VINP4	V11-(V11-V55)*(52.5/53.5)	V11-(V11-V56)*(52.5/54.5)	V11-(V11-V57)*(52.5/56)
V55	V54-(V54-V95)*(1/42)	VINP4	V11-(V11-V56)*(53.5/54.5)	V11-(V11-V57)*(53.5/56)
V56	V54-(V54-V95)*(2/42)	V55-(V55-V95)*(1/41)	VINP4	V11-(V11-V57)*(54.5/56)
V57	V54-(V54-V95)*(3.5/42)	V55-(V55-V95)*(2.5/41)	V56-(V56-V95)*(1.5/40)	VINP4
V58	V54-(V54-V95)*(4.5/42)	V55-(V55-V95)*(3.5/41)	V56-(V56-V95)*(2.5/40)	V57-(V57-V95)*(1/38.5)
V59	V54-(V54-V95)*(5.5/42)	V55-(V55-V95)*(4.5/41)	V56-(V56-V95)*(3.5/40)	V57-(V57-V95)*(2/38.5)
V60	V54-(V54-V95)*(7/42)	V55-(V55-V95)*(6/41)	V56-(V56-V95)*(5/40)	V57-(V57-V95)*(3.5/38.5)
V61	V54-(V54-V95)*(8/42)	V55-(V55-V95)*(7/41)	V56-(V56-V95)*(6/40)	V57-(V57-V95)*(4.5/38.5)
V62	V54-(V54-V95)*(9/42)	V55-(V55-V95)*(8/41)	V56-(V56-V95)*(7/40)	V57-(V57-V95)*(5.5/38.5)
V63	V54-(V54-V95)*(10/42)	V55-(V55-V95)*(9/41)	V56-(V56-V95)*(8/40)	V57-(V57-V95)*(6.5/38.5)
V64	V54-(V54-V95)*(11/42)	V55-(V55-V95)*(10/41)	V56-(V56-V95)*(9/40)	V57-(V57-V95)*(7.5/38.5)
V65	V54-(V54-V95)*(12/42)	V55-(V55-V95)*(11/41)	V56-(V56-V95)*(10/40)	V57-(V57-V95)*(8.5/38.5)
V66	V54-(V54-V95)*(13/42)	V55-(V55-V95)*(12/41)	V56-(V56-V95)*(11/40)	V57-(V57-V95)*(9.5/38.5)
V67	V54-(V54-V95)*(14/42)	V55-(V55-V95)*(13/41)	V56-(V56-V95)*(12/40)	V57-(V57-V95)*(10.5/38.5)

Table 90. Formulas for calculating gamma adjusting voltage (positive polarity) 2 (continued)

Grayscale Voltage	Formula			
	GSRP[3:0]			
	0001	0010	0100	1000
V68	V54-(V54-V95)*(15/42)	V55-(V55-V95)*(14/41)	V56-(V56-V95)*(13/40)	V57-(V57-V95)*(11.5/38.5)
V69	V54-(V54-V95)*(16/42)	V55-(V55-V95)*(15/41)	V56-(V56-V95)*(14/40)	V57-(V57-V95)*(12.5/38.5)
V70	V54-(V54-V95)*(17/42)	V55-(V55-V95)*(16/41)	V56-(V56-V95)*(15/40)	V57-(V57-V95)*(13.5/38.5)
V71	V54-(V54-V95)*(18/42)	V55-(V55-V95)*(17/41)	V56-(V56-V95)*(16/40)	V57-(V57-V95)*(14.5/38.5)
V72	V54-(V54-V95)*(19/42)	V55-(V55-V95)*(18/41)	V56-(V56-V95)*(17/40)	V57-(V57-V95)*(15.5/38.5)
V73	V54-(V54-V95)*(20/42)	V55-(V55-V95)*(19/41)	V56-(V56-V95)*(18/40)	V57-(V57-V95)*(16.5/38.5)
V74	V54-(V54-V95)*(21/42)	V55-(V55-V95)*(20/41)	V56-(V56-V95)*(19/40)	V57-(V57-V95)*(17.5/38.5)
V75	V54-(V54-V95)*(22/42)	V55-(V55-V95)*(21/41)	V56-(V56-V95)*(20/40)	V57-(V57-V95)*(18.5/38.5)
V76	V54-(V54-V95)*(23/42)	V55-(V55-V95)*(22/41)	V56-(V56-V95)*(21/40)	V57-(V57-V95)*(19.5/38.5)
V77	V54-(V54-V95)*(24/42)	V55-(V55-V95)*(23/41)	V56-(V56-V95)*(22/40)	V57-(V57-V95)*(20.5/38.5)
V78	V54-(V54-V95)*(25/42)	V55-(V55-V95)*(24/41)	V56-(V56-V95)*(23/40)	V57-(V57-V95)*(21.5/38.5)
V79	V54-(V54-V95)*(26/42)	V55-(V55-V95)*(25/41)	V56-(V56-V95)*(24/40)	V57-(V57-V95)*(22.5/38.5)
V80	V54-(V54-V95)*(27/42)	V55-(V55-V95)*(26/41)	V56-(V56-V95)*(25/40)	V57-(V57-V95)*(23.5/38.5)
V81	V54-(V54-V95)*(28/42)	V55-(V55-V95)*(27/41)	V56-(V56-V95)*(26/40)	V57-(V57-V95)*(24.5/38.5)
V82	V54-(V54-V95)*(29/42)	V55-(V55-V95)*(28/41)	V56-(V56-V95)*(27/40)	V57-(V57-V95)*(25.5/38.5)
V83	V54-(V54-V95)*(30/42)	V55-(V55-V95)*(29/41)	V56-(V56-V95)*(28/40)	V57-(V57-V95)*(26.5/38.5)
V84	V54-(V54-V95)*(31/42)	V55-(V55-V95)*(30/41)	V56-(V56-V95)*(29/40)	V57-(V57-V95)*(27.5/38.5)
V85	V54-(V54-V95)*(32/42)	V55-(V55-V95)*(31/41)	V56-(V56-V95)*(30/40)	V57-(V57-V95)*(28.5/38.5)
V86	V54-(V54-V95)*(33/42)	V55-(V55-V95)*(32/41)	V56-(V56-V95)*(31/40)	V57-(V57-V95)*(29.5/38.5)
V87	V54-(V54-V95)*(34/42)	V55-(V55-V95)*(33/41)	V56-(V56-V95)*(32/40)	V57-(V57-V95)*(30.5/38.5)
V88	V54-(V54-V95)*(35/42)	V55-(V55-V95)*(34/41)	V56-(V56-V95)*(33/40)	V57-(V57-V95)*(31.5/38.5)
V89	V54-(V54-V95)*(36/42)	V55-(V55-V95)*(35/41)	V56-(V56-V95)*(34/40)	V57-(V57-V95)*(32.5/38.5)
V90	V54-(V54-V95)*(37/42)	V55-(V55-V95)*(36/41)	V56-(V56-V95)*(35/40)	V57-(V57-V95)*(33.5/38.5)
V91	V54-(V54-V95)*(38/42)	V55-(V55-V95)*(37/41)	V56-(V56-V95)*(36/40)	V57-(V57-V95)*(34.5/38.5)
V92	V54-(V54-V95)*(39/42)	V55-(V55-V95)*(38/41)	V56-(V56-V95)*(37/40)	V57-(V57-V95)*(35.5/38.5)
V93	V54-(V54-V95)*(40/42)	V55-(V55-V95)*(39/41)	V56-(V56-V95)*(38/40)	V57-(V57-V95)*(36.5/38.5)
V94	V54-(V54-V95)*(41/42)	V55-(V55-V95)*(40/41)	V56-(V56-V95)*(39/40)	V57-(V57-V95)*(37.5/38.5)
V95	VINP5			
V96	V95-(V95-VC)*(1/33)			
V97	V95-(V95-VC)*(2/33)			
V98	V95-(V95-VC)*(3/33)			
V99	V95-(V95-VC)*(4/33)			
V100	V95-(V95-VC)*(5/33)			
V101	V95-(V95-VC)*(6/33)			

Table 91. Formulas for calculating gamma adjusting voltage (positive polarity) 2 (continued)

Grayscale Voltage	Formula			
	GSRP[3:0]			
	0001	0010	0100	1000
V102	V95-(V95-VC)*(7/33)			
V103	V95-(V95-VC)*(8/33)			
V104	V95-(V95-VC)*(9/33)			
V105	V95-(V95-VC)*(10/33)			
V106	V95-(V95-VC)*(11/33)			
V107	V95-(V95-VC)*(12/33)			
V108	V95-(V95-VC)*(13/33)			
V109	V95-(V95-VC)*(14/33)			
V110	V95-(V95-VC)*(15/33)			
V111	V95-(V95-VC)*(16/33)			
V112	V95-(V95-VC)*(17/33)			
V113	V95-(V95-VC)*(18/33)			
V114	V95-(V95-VC)*(19/33)			
V115	V95-(V95-VC)*(20/33)			
V116	V95-(V95-VC)*(21/33)			
V117	V95-(V95-VC)*(22/33)			
V118	V95-(V95-VC)*(23/33)			
V119	V95-(V95-VC)*(24.5/33)			
V120	V95-(V95-VC)*(25.5/33)			
V121	V95-(V95-VC)*(26.5/33)			
V122	V95-(V95-VC)*(27.5/33)			
V123	V95-(V95-VC)*(28.5/33)			
V124	V95-(V95-VC)*(29.5/33)			
V125	V95-(V95-VC)*(30.5/33)			
V126	V95-(V95-VC)*(31/33)			
V127	V95-(V95-VC)*(32/33)			
VC	VINP6			
V128	VC-(VC-V160)*(0.5/32)			
V129	VC-(VC-V160)*(1.5/32)			
V130	VC-(VC-V160)*(2.5/32)			
V131	VC-(VC-V160)*(3.5/32)			
V132	VC-(VC-V160)*(4.5/32)			
V133	VC-(VC-V160)*(5.5/32)			
V134	VC-(VC-V160)*(6.5/32)			

Table 92. Formulas for calculating gamma adjusting voltage (positive polarity) 2 (continued)

Grayscale Voltage	Formula			
	GSRP[3:0]			
	0001	0010	0100	1000
V135	VC-(VC-V160)*(7.5/32)			
V136	VC-(VC-V160)*(8.5/32)			
V137	VC-(VC-V160)*(9/32)			
V138	VC-(VC-V160)*(10/32)			
V139	VC-(VC-V160)*(11/32)			
V140	VC-(VC-V160)*(12/32)			
V141	VC-(VC-V160)*(13/32)			
V142	VC-(VC-V160)*(14/32)			
V143	VC-(VC-V160)*(15/32)			
V144	VC-(VC-V160)*(16/32)			
V145	VC-(VC-V160)*(17/32)			
V146	VC-(VC-V160)*(18/32)			
V147	VC-(VC-V160)*(19/32)			
V148	VC-(VC-V160)*(20/32)			
V149	VC-(VC-V160)*(21/32)			
V150	VC-(VC-V160)*(22/32)			
V151	VC-(VC-V160)*(23/32)			
V152	VC-(VC-V160)*(24.5/32)			
V153	VC-(VC-V160)*(25.5/32)			
V154	VC-(VC-V160)*(26.5/32)			
V155	VC-(VC-V160)*(27.5/32)			
V156	VC-(VC-V160)*(28.5/32)			
V157	VC-(VC-V160)*(29.5/32)			
V158	VC-(VC-V160)*(30/32)			
V159	VC-(VC-V160)*(31/32)			
V160	VINP7			
V161	V160-(V160-V199)*(1/40.5)	V160-(V160-V200)*(1/41.5)	V160-(V160-V201)*(1/42.5)	V160-(V160-V202)*(1/43)
V162	V160-(V160-V199)*(2/40.5)	V160-(V160-V200)*(2/41.5)	V160-(V160-V201)*(2/42.5)	V160-(V160-V202)*(2/43)
V163	V160-(V160-V199)*(3/40.5)	V160-(V160-V200)*(3/41.5)	V160-(V160-V201)*(3/42.5)	V160-(V160-V202)*(3/43)
V164	V160-(V160-V199)*(3.5/40.5)	V160-(V160-V200)*(3.5/41.5)	V160-(V160-V201)*(3.5/42.5)	V160-(V160-V202)*(3.5/43)
V165	V160-(V160-V199)*(4.5/40.5)	V160-(V160-V200)*(4.5/41.5)	V160-(V160-V201)*(4.5/42.5)	V160-(V160-V202)*(4.5/43)
V166	V160-(V160-V199)*(5.5/40.5)	V160-(V160-V200)*(5.5/41.5)	V160-(V160-V201)*(5.5/42.5)	V160-(V160-V202)*(5.5/43)
V167	V160-(V160-V199)*(6.5/40.5)	V160-(V160-V200)*(6.5/41.5)	V160-(V160-V201)*(6.5/42.5)	V160-(V160-V202)*(6.5/43)
V168	V160-(V160-V199)*(7.5/40.5)	V160-(V160-V200)*(7.5/41.5)	V160-(V160-V201)*(7.5/42.5)	V160-(V160-V202)*(7.5/43)

Table 93. Formulas for calculating gamma adjusting voltage (positive polarity) 2 (continued)

Grayscale Voltage	Formula			
	GSRP[3:0]			
	0001	0010	0100	1000
V169	V160-(V160-V199)*(8.5/40.5)	V160-(V160-V200)*(8.5/41.5)	V160-(V160-V201)*(8.5/42.5)	V160-(V160-V202)*(8.5/43)
V170	V160-(V160-V199)*(9.5/40.5)	V160-(V160-V200)*(9.5/41.5)	V160-(V160-V201)*(9.5/42.5)	V160-(V160-V202)*(9.5/43)
V171	V160-(V160-V199)*(10.5/40.5)	V160-(V160-V200)*(10.5/41.5)	V160-(V160-V201)*(10.5/42.5)	V160-(V160-V202)*(10.5/43)
V172	V160-(V160-V199)*(11.5/40.5)	V160-(V160-V200)*(11.5/41.5)	V160-(V160-V201)*(11.5/42.5)	V160-(V160-V202)*(11.5/43)
V173	V160-(V160-V199)*(12.5/40.5)	V160-(V160-V200)*(12.5/41.5)	V160-(V160-V201)*(12.5/42.5)	V160-(V160-V202)*(12.5/43)
V174	V160-(V160-V199)*(13.5/40.5)	V160-(V160-V200)*(13.5/41.5)	V160-(V160-V201)*(13.5/42.5)	V160-(V160-V202)*(13.5/43)
V175	V160-(V160-V199)*(14.5/40.5)	V160-(V160-V200)*(14.5/41.5)	V160-(V160-V201)*(14.5/42.5)	V160-(V160-V202)*(14.5/43)
V176	V160-(V160-V199)*(15.5/40.5)	V160-(V160-V200)*(15.5/41.5)	V160-(V160-V201)*(15.5/42.5)	V160-(V160-V202)*(15.5/43)
V177	V160-(V160-V199)*(16.5/40.5)	V160-(V160-V200)*(16.5/41.5)	V160-(V160-V201)*(16.5/42.5)	V160-(V160-V202)*(16.5/43)
V178	V160-(V160-V199)*(17.5/40.5)	V160-(V160-V200)*(17.5/41.5)	V160-(V160-V201)*(17.5/42.5)	V160-(V160-V202)*(17.5/43)
V179	V160-(V160-V199)*(18.5/40.5)	V160-(V160-V200)*(18.5/41.5)	V160-(V160-V201)*(18.5/42.5)	V160-(V160-V202)*(18.5/43)
V180	V160-(V160-V199)*(19.5/40.5)	V160-(V160-V200)*(19.5/41.5)	V160-(V160-V201)*(19.5/42.5)	V160-(V160-V202)*(19.5/43)
V181	V160-(V160-V199)*(20.5/40.5)	V160-(V160-V200)*(20.5/41.5)	V160-(V160-V201)*(20.5/42.5)	V160-(V160-V202)*(20.5/43)
V182	V160-(V160-V199)*(21.5/40.5)	V160-(V160-V200)*(21.5/41.5)	V160-(V160-V201)*(21.5/42.5)	V160-(V160-V202)*(21.5/43)
V183	V160-(V160-V199)*(22.5/40.5)	V160-(V160-V200)*(22.5/41.5)	V160-(V160-V201)*(22.5/42.5)	V160-(V160-V202)*(22.5/43)
V184	V160-(V160-V199)*(23.5/40.5)	V160-(V160-V200)*(23.5/41.5)	V160-(V160-V201)*(23.5/42.5)	V160-(V160-V202)*(23.5/43)
V185	V160-(V160-V199)*(24.5/40.5)	V160-(V160-V200)*(24.5/41.5)	V160-(V160-V201)*(24.5/42.5)	V160-(V160-V202)*(24.5/43)
V186	V160-(V160-V199)*(25.5/40.5)	V160-(V160-V200)*(25.5/41.5)	V160-(V160-V201)*(25.5/42.5)	V160-(V160-V202)*(25.5/43)
V187	V160-(V160-V199)*(26.5/40.5)	V160-(V160-V200)*(26.5/41.5)	V160-(V160-V201)*(26.5/42.5)	V160-(V160-V202)*(26.5/43)
V188	V160-(V160-V199)*(27.5/40.5)	V160-(V160-V200)*(27.5/41.5)	V160-(V160-V201)*(27.5/42.5)	V160-(V160-V202)*(27.5/43)
V189	V160-(V160-V199)*(29.5/40.5)	V160-(V160-V200)*(29.5/41.5)	V160-(V160-V201)*(29.5/42.5)	V160-(V160-V202)*(29.5/43)
V190	V160-(V160-V199)*(30.5/40.5)	V160-(V160-V200)*(30.5/41.5)	V160-(V160-V201)*(30.5/42.5)	V160-(V160-V202)*(30.5/43)
V191	V160-(V160-V199)*(31.5/40.5)	V160-(V160-V200)*(31.5/41.5)	V160-(V160-V201)*(31.5/42.5)	V160-(V160-V202)*(31.5/43)
V192	V160-(V160-V199)*(32.5/40.5)	V160-(V160-V200)*(32.5/41.5)	V160-(V160-V201)*(32.5/42.5)	V160-(V160-V202)*(32.5/43)
V193	V160-(V160-V199)*(33.5/40.5)	V160-(V160-V200)*(33.5/41.5)	V160-(V160-V201)*(33.5/42.5)	V160-(V160-V202)*(33.5/43)
V194	V160-(V160-V199)*(35/40.5)	V160-(V160-V200)*(35/41.5)	V160-(V160-V201)*(35/42.5)	V160-(V160-V202)*(35/43)
V195	V160-(V160-V199)*(36/40.5)	V160-(V160-V200)*(36/41.5)	V160-(V160-V201)*(36/42.5)	V160-(V160-V202)*(36/43)
V196	V160-(V160-V199)*(37/40.5)	V160-(V160-V200)*(37/41.5)	V160-(V160-V201)*(37/42.5)	V160-(V160-V202)*(37/43)
V197	V160-(V160-V199)*(38/40.5)	V160-(V160-V200)*(38/41.5)	V160-(V160-V201)*(38/42.5)	V160-(V160-V202)*(38/43)
V198	V160-(V160-V199)*(39.5/40.5)	V160-(V160-V200)*(39.5/41.5)	V160-(V160-V201)*(39.5/42.5)	V160-(V160-V202)*(39.5/43)
V199	VINP8	V160-(V160-V200)*(40.5/41.5)	V160-(V160-V201)*(40.5/42.5)	V160-(V160-V202)*(40.5/43)
V200	V199-(V199-V244)*(1/50.5)	VINP8	V160-(V160-V201)*(41.5/42.5)	V160-(V160-V202)*(41.5/43)
V201	V199-(V199-V244)*(2/50.5)	V200-(V200-V244)*(1/49.5)	VINP8	V160-(V160-V202)*(42.5/43)
V202	V199-(V199-V244)*(2.5/50.5)	V200-(V200-V244)*(1.5/49.5)	V201-(V201-V244)*(0.5/48.5)	VINP8

Table 94. Formulas for calculating gamma adjusting voltage (positive polarity) 2 (continued)

Grayscale Voltage	Formula			
	GSRP[3:0]			
	0001	0010	0100	1000
V203	V199-(V199-V244)*(3/50.5)	V200-(V200-V244)*(2/49.5)	V201-(V201-V244)*(1/48.5)	V202-(V202-V244)*(0.5/48)
V204	V199-(V199-V244)*(3.5/50.5)	V200-(V200-V244)*(2.5/49.5)	V201-(V201-V244)*(1.5/48.5)	V202-(V202-V244)*(1/48)
V205	V199-(V199-V244)*(5/50.5)	V200-(V200-V244)*(4/49.5)	V201-(V201-V244)*(3/48.5)	V202-(V202-V244)*(2.5/48)
V206	V199-(V199-V244)*(5.5/50.5)	V200-(V200-V244)*(4.5/49.5)	V201-(V201-V244)*(3.5/48.5)	V202-(V202-V244)*(3/48)
V207	V199-(V199-V244)*(6/50.5)	V200-(V200-V244)*(5/49.5)	V201-(V201-V244)*(4/48.5)	V202-(V202-V244)*(3.5/48)
V208	V199-(V199-V244)*(6.5/50.5)	V200-(V200-V244)*(5.5/49.5)	V201-(V201-V244)*(4.5/48.5)	V202-(V202-V244)*(4/48)
V209	V199-(V199-V244)*(7.5/50.5)	V200-(V200-V244)*(6.5/49.5)	V201-(V201-V244)*(5.5/48.5)	V202-(V202-V244)*(5/48)
V210	V199-(V199-V244)*(8/50.5)	V200-(V200-V244)*(7/49.5)	V201-(V201-V244)*(6/48.5)	V202-(V202-V244)*(5.5/48)
V211	V199-(V199-V244)*(9/50.5)	V200-(V200-V244)*(8/49.5)	V201-(V201-V244)*(7/48.5)	V202-(V202-V244)*(6.5/48)
V212	V199-(V199-V244)*(10/50.5)	V200-(V200-V244)*(9/49.5)	V201-(V201-V244)*(8/48.5)	V202-(V202-V244)*(7.5/48)
V213	V199-(V199-V244)*(11/50.5)	V200-(V200-V244)*(10/49.5)	V201-(V201-V244)*(9/48.5)	V202-(V202-V244)*(8.5/48)
V214	V199-(V199-V244)*(11.5/50.5)	V200-(V200-V244)*(10.5/49.5)	V201-(V201-V244)*(9.5/48.5)	V202-(V202-V244)*(9/48)
V215	V199-(V199-V244)*(12/50.5)	V200-(V200-V244)*(11/49.5)	V201-(V201-V244)*(10/48.5)	V202-(V202-V244)*(9.5/48)
V216	V199-(V199-V244)*(13/50.5)	V200-(V200-V244)*(12/49.5)	V201-(V201-V244)*(11/48.5)	V202-(V202-V244)*(10.5/48)
V217	V199-(V199-V244)*(14/50.5)	V200-(V200-V244)*(13/49.5)	V201-(V201-V244)*(12/48.5)	V202-(V202-V244)*(11.5/48)
V218	V199-(V199-V244)*(15/50.5)	V200-(V200-V244)*(14/49.5)	V201-(V201-V244)*(13/48.5)	V202-(V202-V244)*(12.5/48)
V219	V199-(V199-V244)*(16/50.5)	V200-(V200-V244)*(15/49.5)	V201-(V201-V244)*(14/48.5)	V202-(V202-V244)*(13.5/48)
V220	V199-(V199-V244)*(17/50.5)	V200-(V200-V244)*(16/49.5)	V201-(V201-V244)*(15/48.5)	V202-(V202-V244)*(14.5/48)
V221	V199-(V199-V244)*(18/50.5)	V200-(V200-V244)*(17/49.5)	V201-(V201-V244)*(16/48.5)	V202-(V202-V244)*(15.5/48)
V222	V199-(V199-V244)*(19/50.5)	V200-(V200-V244)*(18/49.5)	V201-(V201-V244)*(17/48.5)	V202-(V202-V244)*(16.5/48)
V223	V199-(V199-V244)*(20/50.5)	V200-(V200-V244)*(19/49.5)	V201-(V201-V244)*(18/48.5)	V202-(V202-V244)*(17.5/48)
V224	V199-(V199-V244)*(21/50.5)	V200-(V200-V244)*(20/49.5)	V201-(V201-V244)*(19/48.5)	V202-(V202-V244)*(18.5/48)
V225	V199-(V199-V244)*(22/50.5)	V200-(V200-V244)*(21/49.5)	V201-(V201-V244)*(20/48.5)	V202-(V202-V244)*(19.5/48)
V226	V199-(V199-V244)*(23/50.5)	V200-(V200-V244)*(22/49.5)	V201-(V201-V244)*(21/48.5)	V202-(V202-V244)*(20.5/48)
V227	V199-(V199-V244)*(24/50.5)	V200-(V200-V244)*(23/49.5)	V201-(V201-V244)*(22/48.5)	V202-(V202-V244)*(21.5/48)
V228	V199-(V199-V244)*(25.5/50.5)	V200-(V200-V244)*(24.5/49.5)	V201-(V201-V244)*(23.5/48.5)	V202-(V202-V244)*(23/48)
V229	V199-(V199-V244)*(26.5/50.5)	V200-(V200-V244)*(25.5/49.5)	V201-(V201-V244)*(24.5/48.5)	V202-(V202-V244)*(24/48)
V230	V199-(V199-V244)*(27.5/50.5)	V200-(V200-V244)*(26.5/49.5)	V201-(V201-V244)*(25.5/48.5)	V202-(V202-V244)*(25/48)
V231	V199-(V199-V244)*(29/50.5)	V200-(V200-V244)*(28/49.5)	V201-(V201-V244)*(27/48.5)	V202-(V202-V244)*(26.5/48)
V232	V199-(V199-V244)*(30.5/50.5)	V200-(V200-V244)*(29.5/49.5)	V201-(V201-V244)*(28.5/48.5)	V202-(V202-V244)*(28/48)
V233	V199-(V199-V244)*(32/50.5)	V200-(V200-V244)*(31/49.5)	V201-(V201-V244)*(30/48.5)	V202-(V202-V244)*(29.5/48)
V234	V199-(V199-V244)*(33.5/50.5)	V200-(V200-V244)*(32.5/49.5)	V201-(V201-V244)*(31.5/48.5)	V202-(V202-V244)*(31/48)
V235	V199-(V199-V244)*(34.5/50.5)	V200-(V200-V244)*(33.5/49.5)	V201-(V201-V244)*(32.5/48.5)	V202-(V202-V244)*(32/48)
V236	V199-(V199-V244)*(36/50.5)	V200-(V200-V244)*(35/49.5)	V201-(V201-V244)*(34/48.5)	V202-(V202-V244)*(33.5/48)

Table 95. Formulas for calculating gamma adjusting voltage (positive polarity) 2 (continued)

Grayscale Voltage	Formula			
	GSRP[3:0]			
	0001	0010	0100	1000
V237	V199-(V199-V244)*(37.5/50.5)	V200-(V200-V244)*(36.5/49.5)	V201-(V201-V244)*(35.5/48.5)	V202-(V202-V244)*(35/48)
V238	V199-(V199-V244)*(39.5/50.5)	V200-(V200-V244)*(38.5/49.5)	V201-(V201-V244)*(37.5/48.5)	V202-(V202-V244)*(37/48)
V239	V199-(V199-V244)*(40.5/50.5)	V200-(V200-V244)*(39.5/49.5)	V201-(V201-V244)*(38.5/48.5)	V202-(V202-V244)*(38/48)
V240	V199-(V199-V244)*(42.5/50.5)	V200-(V200-V244)*(41.5/49.5)	V201-(V201-V244)*(40.5/48.5)	V202-(V202-V244)*(40/48)
V241	V199-(V199-V244)*(44.5/50.5)	V200-(V200-V244)*(43.5/49.5)	V201-(V201-V244)*(42.5/48.5)	V202-(V202-V244)*(42/48)
V242	V199-(V199-V244)*(46.5/50.5)	V200-(V200-V244)*(45.5/49.5)	V201-(V201-V244)*(44.5/48.5)	V202-(V202-V244)*(44/48)
V243	V199-(V199-V244)*(48.5/50.5)	V200-(V200-V244)*(47.5/49.5)	V201-(V201-V244)*(46.5/48.5)	V202-(V202-V244)*(46/48)
V244	VINP9			
V245	V244-(V244-V249)*(1.5/9.5)	V244-(V244-V250)*(1.5/13)	V244-(V244-V251)*(1.5/15)	V244-(V244-V252)*(1.5/17)
V246	V244-(V244-V249)*(3.5/9.5)	V244-(V244-V250)*(3.5/13)	V244-(V244-V251)*(3.5/15)	V244-(V244-V252)*(3.5/17)
V247	V244-(V244-V249)*(5.5/9.5)	V244-(V244-V250)*(5.5/13)	V244-(V244-V251)*(5.5/15)	V244-(V244-V252)*(5.5/17)
V248	V244-(V244-V249)*(7.5/9.5)	V244-(V244-V250)*(7.5/13)	V244-(V244-V251)*(7.5/15)	V244-(V244-V252)*(7.5/17)
V249	VINP10	V244-(V244-V250)*(9.5/13)	V244-(V244-V251)*(9.5/15)	V244-(V244-V252)*(9.5/17)
V250	V249-(V249-V254)*(3.5/12)	VINP10	V244-(V244-V251)*(13/15)	V244-(V244-V252)*(13/17)
V251	V249-(V249-V254)*(5.5/12)	V250-(V250-V254)*(2/8.5)	VINP10	V244-(V244-V252)*(15/17)
V252	V249-(V249-V254)*(7.5/12)	V250-(V250-V254)*(4/8.5)	V251-(V251-V254)*(2/6.5)	VINP10
V253	V249-(V249-V254)*(10/12)	V250-(V250-V254)*(6.5/8.5)	V251-(V251-V254)*(4.5/4.5)	V252-(V252-V254)*(2.5/4.5)
V254	VINP11			
V255	VINP12			

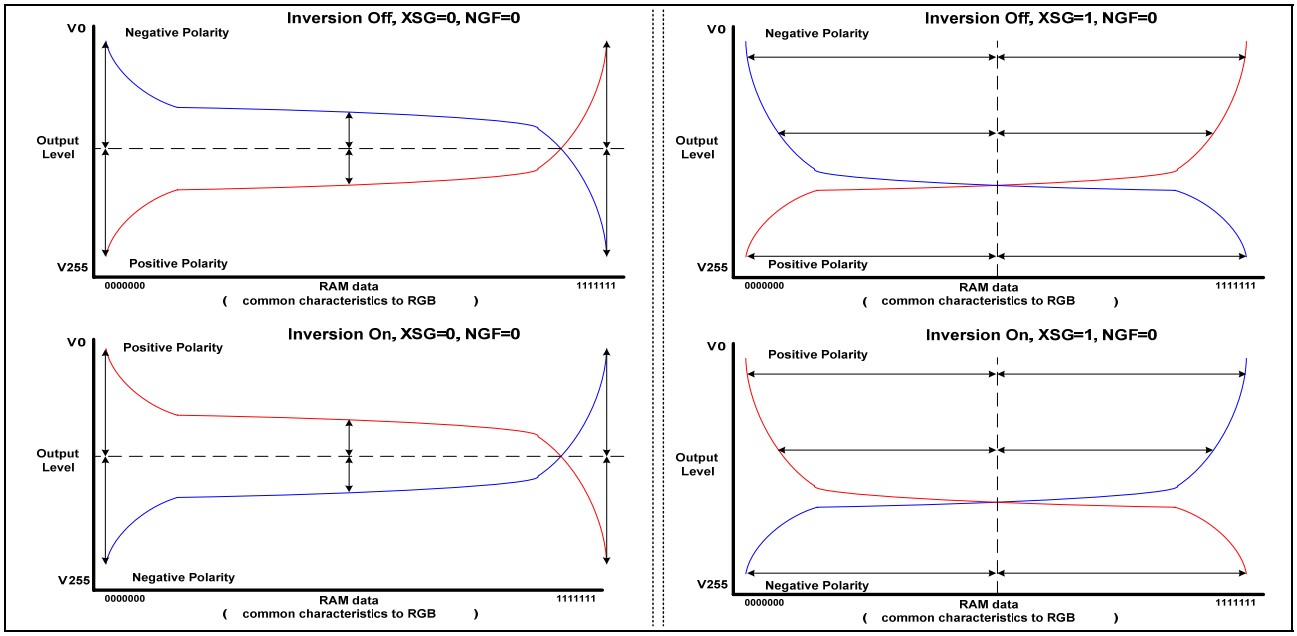


Figure 111. Relationship between RAM data and output voltage

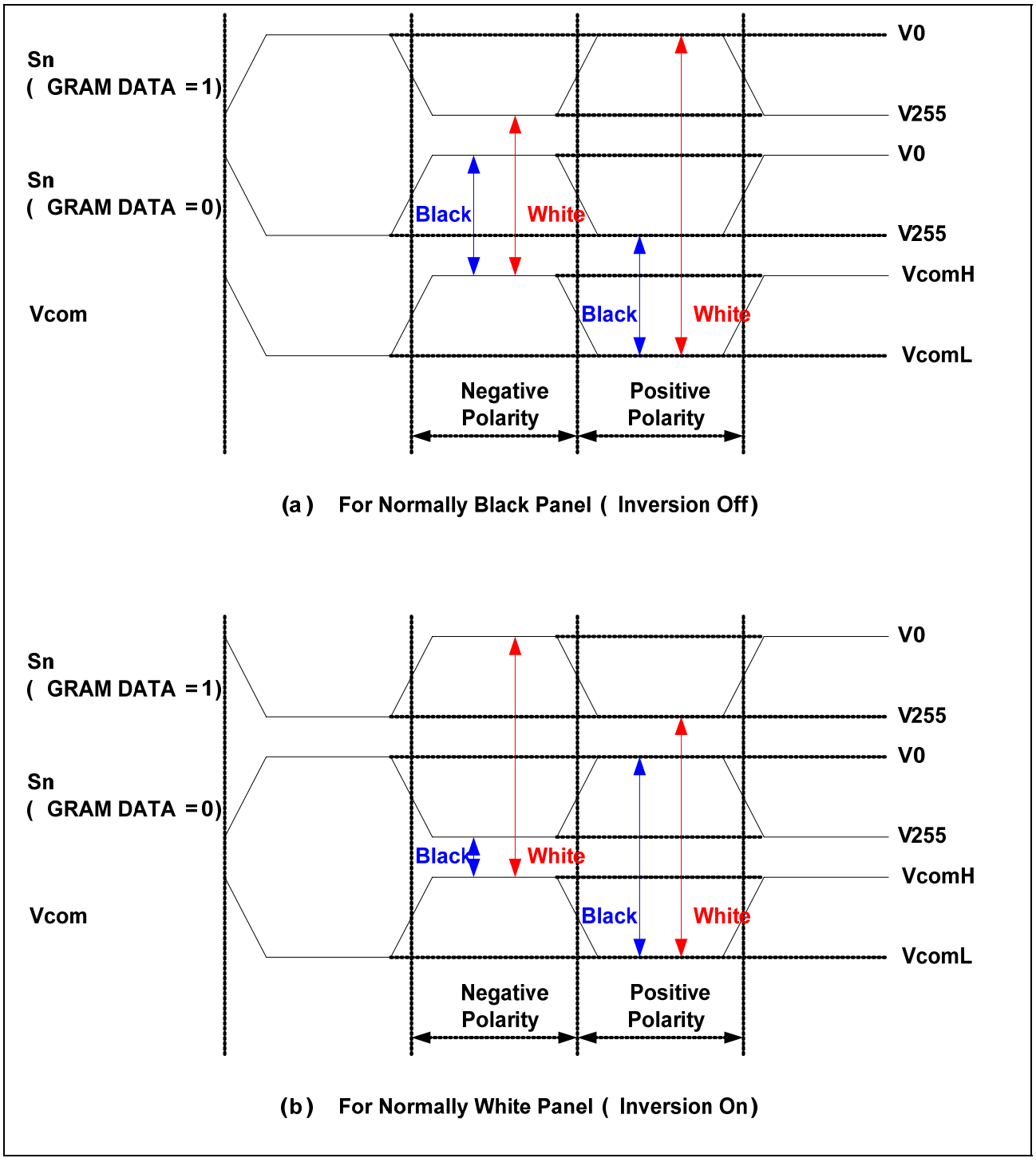


Figure 112. Relationship between source output and VCOM

4.3. PANEL CONTROL

4.3.1. Gate Driver

The gate driver block includes gate control outputs (G1 to G432) which should be connected directly to the TFT-LCD.

4.4. OSCILLATOR- SYSTEM CLOCK GENERATOR

S6D04D1 has an on-chip oscillator which does not require any external components. This oscillator output signal is used for the system clock generation for internal display operation.

4.4.1. Oscillator Circuit

The S6D04D1 can provide R-C oscillation. S6D04D1 internal oscillator does not need to attach the external resistor. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the oscillator frequency control register setting. Since R-C oscillation stops during the standby mode, power consumption can be reduced.

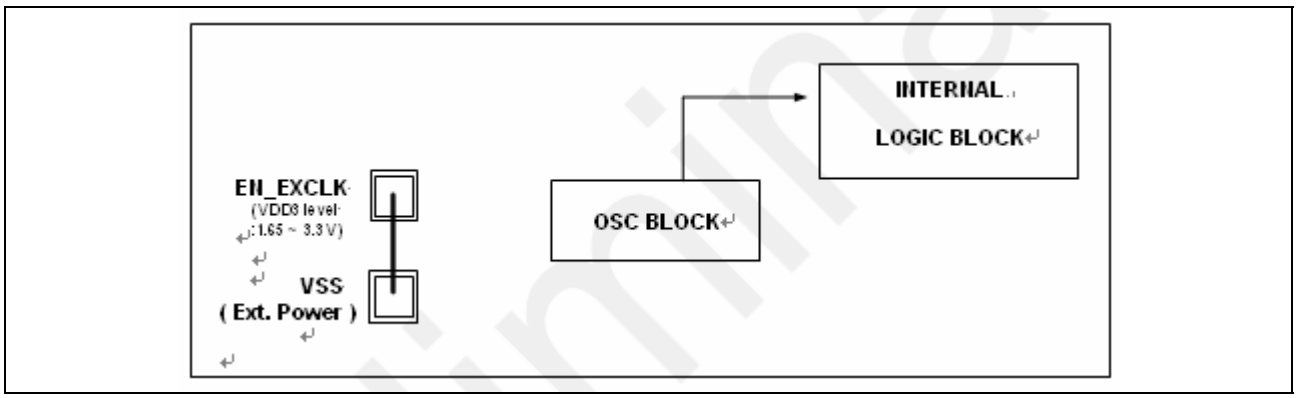


Figure 113. Application diagram for oscillator circuitry

4.4.2. Frame Frequency Adjusting Function

The S6D04D1 has an on-chip frame-frequency adjustment function. The frame frequency can be adjusted by the instruction setting (RTN & CRTN) during the LCD driver operation as the oscillation frequency is always same. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching for an animated display is required, the frame frequency can be set high.

The relationship between the LCD driving duty and the frame frequency is calculated by the following expression. The frame frequency can be adjusted in the RTN (1H period adjusting bit) and CRTN (1 RTN period adjusting bit) .

$$\text{Frame Frequency} = \frac{f_{osc}}{CRTN \times RTN \times (Line + B)} \ [Hz]$$

f osc : R-C oscillation frequency (Fixed to 13.9MHz)
Line : Number of raster rows
RTN : Clock cycles per raster rows
CRTN : Clock cycles per 1 RTN Clock
B : Blank period (Back porch + Front porch)

* Note : (RTN x CTRN) > 260

Figure 114. Formula for the frame frequency

Calculation Example :

* Display Condition
  - Line: 432
  - Frame frequency = 60 Hz
  - B: Blank period (BP + FP): 16

If RTN[4:0] set to 10110(1H period: 22clock), CRTN[4:0] set to 10110(1RTN period: 22 clock),
13.9 MHz / {(22x 22) x (432+16)} = 64.1 [Hz]

The calculation result says that the required RTN, CRTN setting in the display condition listed above is 22. So the RTN and CRTN value should be selected to make 60Hz frame frequency is 22.

4.5. DISPLAY DATA RAM

4.5.1. Address Counter

The address counter sets the addresses of the display data RAM for writing and reading. Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 8-8-8-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=239 (EFh) and Y=0 to Y=431 (1AFh). Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined onto which it will be written. The window is programmable via the command registers SC, SP designating the start address and EC, EP designating the end address. For example, the whole display contents will be written, and the window will be defined by the following values: SC=0 (0h), SP=0 (0h) and EC=239 (EFh), EP=431 (1AFh).

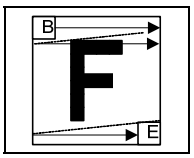
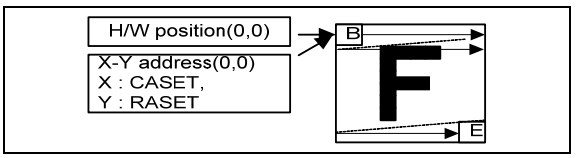
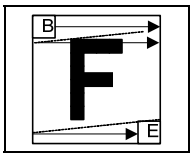
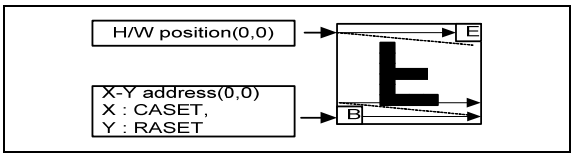
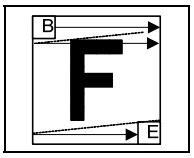
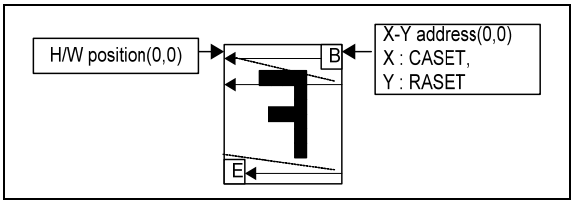
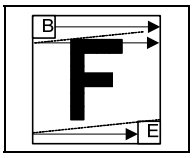
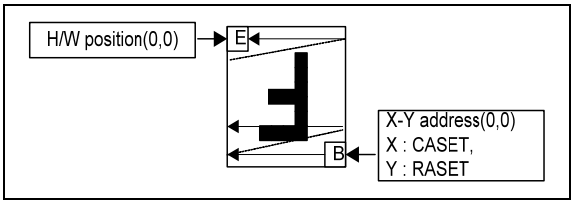
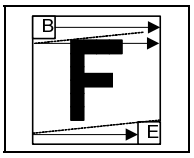
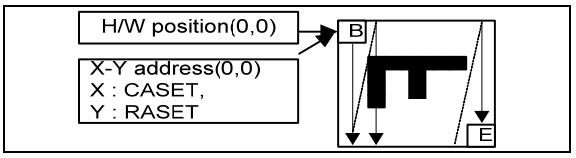
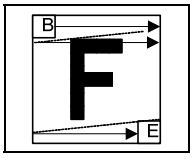
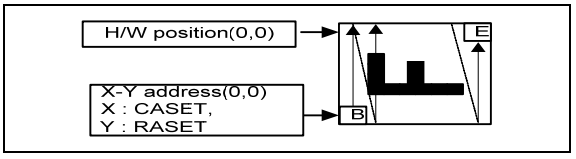
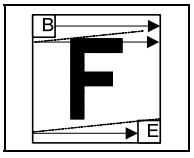
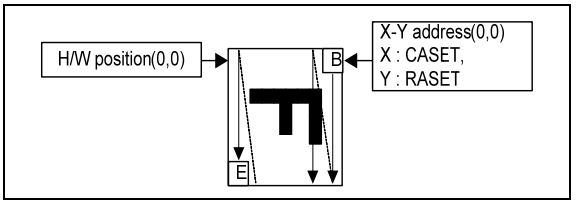
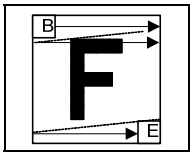
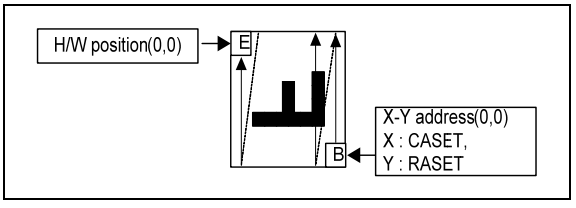
In vertical addressing mode (D5=1), the Y-address increments after each byte. After the last Y-address (Y=EP), Y wraps around to SP and X increments to address the next column. In horizontal addressing mode (D5=0), the X-address increments after each byte. After the last X-address (X=EC), X wraps around to SC and Y increments to address the next page. After every last address (X=EC and Y=EP) the address pointers wrap around to address (X=SC and Y=SP). For flexibility in handling a wide variety of display architectures, the commands "CASET, PASET" and "MADCTL" (see section 5 command lists) define flags D6 and D7, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Following Figure shows the available combinations of writing to the display RAM. When D6, D7 and D5 will be changed the data must be rewritten to the display RAM.

For each image condition, the controls for the column and page counters apply as below:

Table 96. Control for column and page counter

Condition	Column counter	Page counter
When RAMWR/RAMRD command is accepted	Return to "start column(SC)"	Return to "start page(SP)"
Complete pixel read/write action	Increment by 1	No change
The column counter value is large than "End column (EC)"	Return to "start column(SC)"	Increment by 1
The page counter value is large than "End page (EP)"	Return to "start column(SC)"	Return to "start page(SP)"

Table 97. Frame data write direction according to the MADCTL parameters (D5, D6 and D7)

Display Data direction	MADCTL parameter			Image in the host(MCU)	Image in the driver (GRAM)
	D5	D6	D7		
Normal	0	0	0		
Y-mirror	0	0	1		
X-mirror	0	1	0		
X-mirror Y-mirror	0	1	1		
X-Y exchange	1	0	0		
X-Y exchange Y-mirror	1	0	1		
X-Y exchange X-mirror	1	1	0		
X-Y exchange X-mirror Y-mirror	1	1	1		

Note.D5, D6 and D7 are parameters of MADCTL command. D5(MV), D6(MX), D7(MY)

4.5.2. Memory to Display Address Mapping

4.5.2.1. When Using 240RGB x 432 Resolution (MX = MY = RGB = '0')

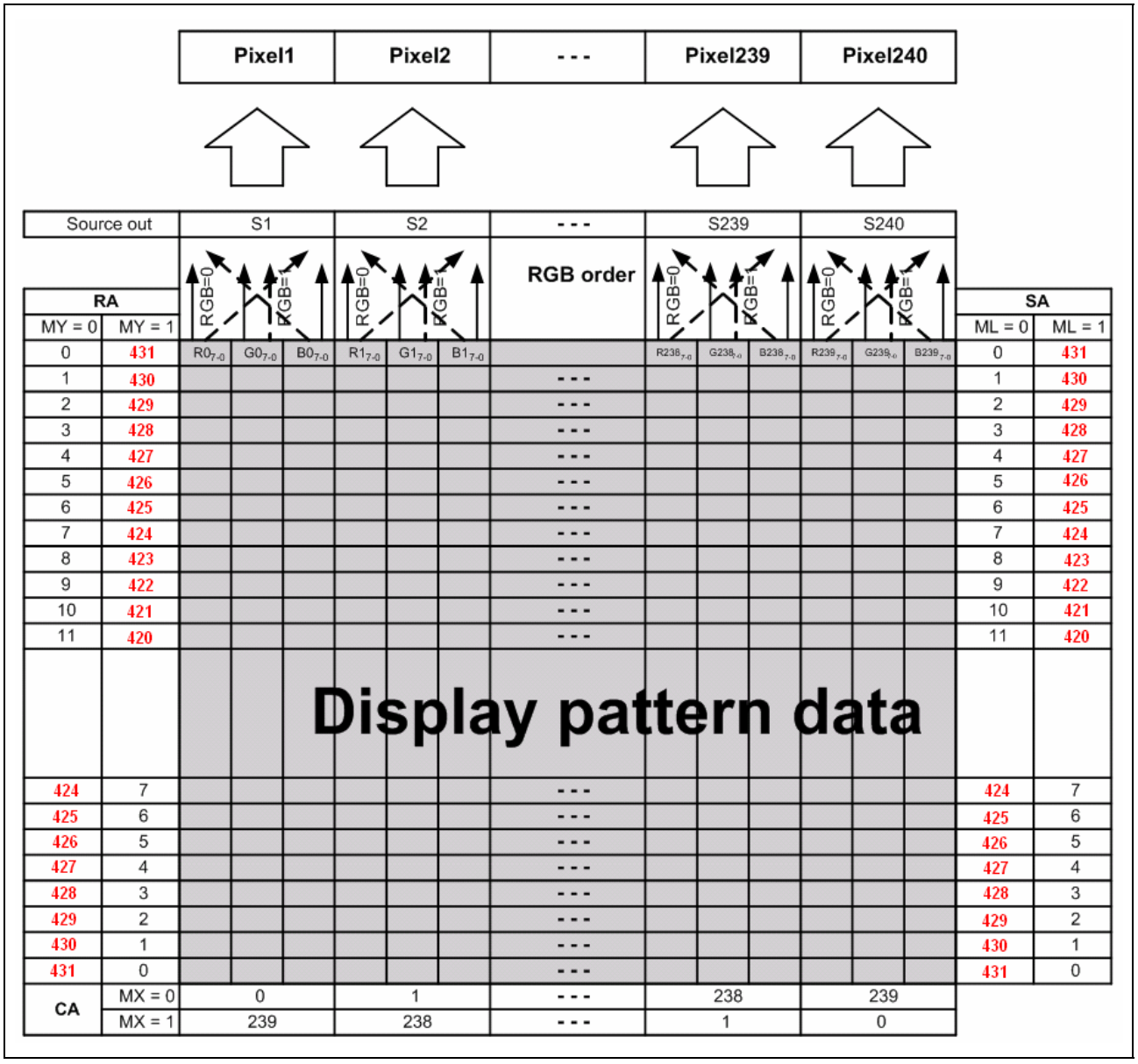


Figure 115. Memory to display address mapping

Note1. RA = Row Address,(Page Address)

Note2. CA = Column Address,

Note3. SA = Scan Address,

Note4. MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

Note5. MY = Mirror Y-axis (Page address direction parameter), D7 parameter of MADCTL command

Note6. ML = Scan direction parameter, D4 parameter of MADCTL command

Note7. RGB= Red, Green and Blue pixel position change, D3 parameter of MADCTL command

4.5.3. Normal Display On or Partial Mode On

4.5.3.1. When Using 240RGB x 432 Resolution

In this mode, the content of the frame memory within an area where column pointer is 00h to EFh and page pointer is 000h to 1AFh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0).

1. Example for Normal Display On (D6 = D7 = D4 = '0', MX = MY = '0')

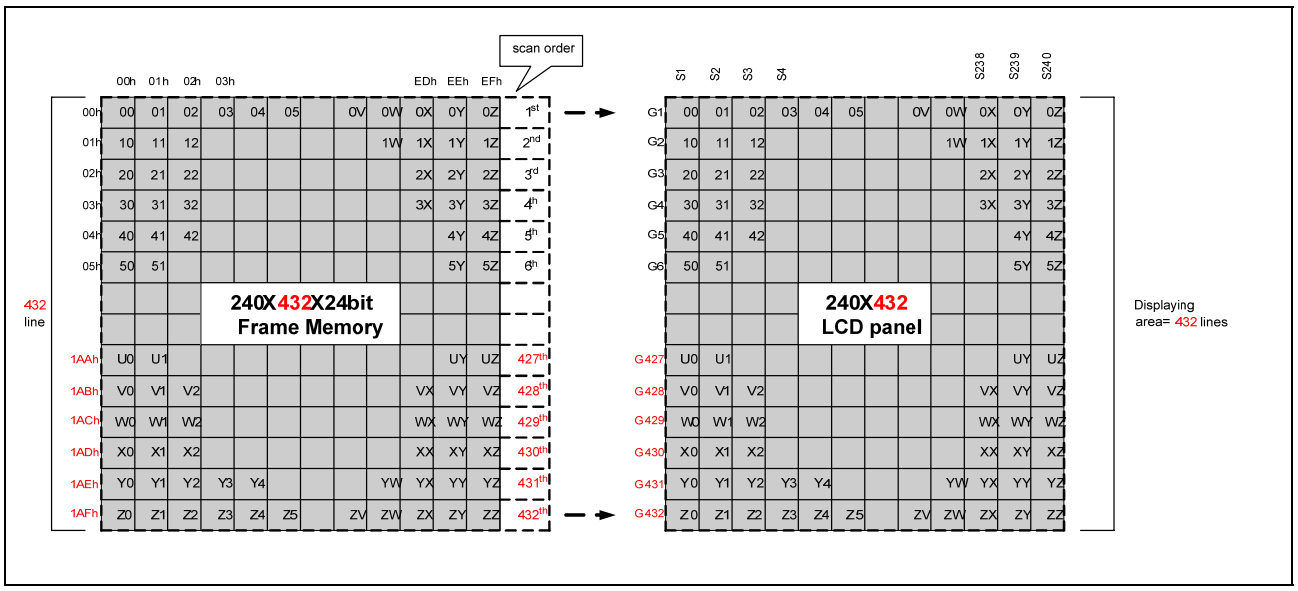


Figure 116. Example for normal display on (D6 = D7 = D4 = '0', MX = MY = '0')

2. Partial Display On: SR [15:0] = 04h, ER [15:0] = 1ACh, MADCTL

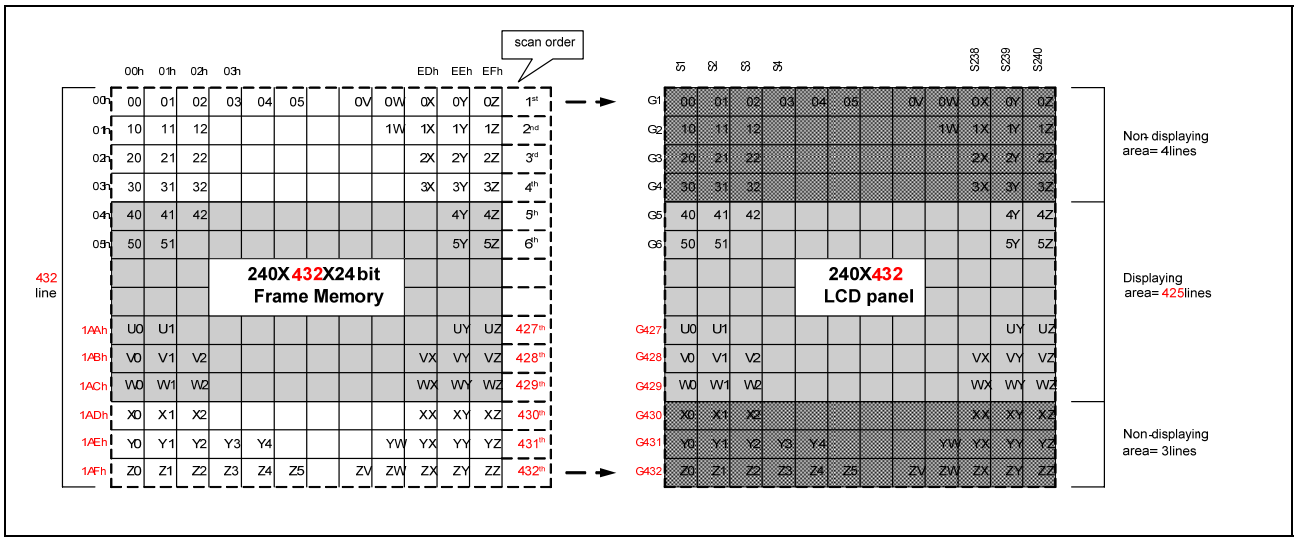


Figure 117. Partial display on: SR [15:0] = 04h, ER [15:0] = 1ACh, MADCTL

4.5.4. Command Definition is Independent of the IC Mount Position

Depending on how the MADCTL command is set, the top-bottom / left-right definitions are changed in the driver IC to adapt to the mounted form.

4.5.4.1. Model of LCD Module for the S6D04D1

The LCD module for the S6D04D1 is shown below. The top-bottom / left-right positions, RGB filter and white/ black back ground defined in this development specification are in accordance with the diagram shown below.

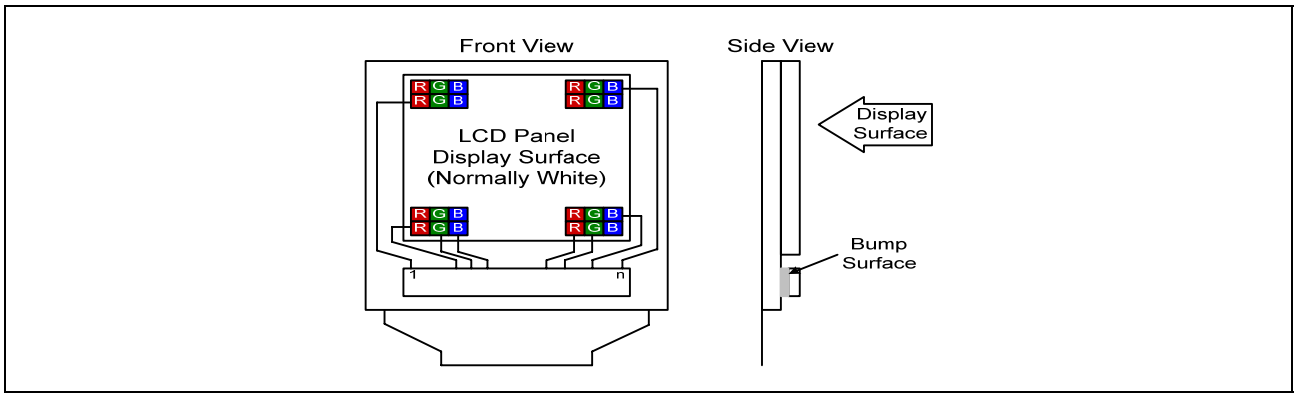


Figure 118. Model of LCD module for the S6D04D1

4.5.4.2. Position Definition by IC Mount

The set value of MADCTL actually used internally in the IC changes depending on how MADDEF is set. The arithmetic operation in the table below is performed on each bit. (The 'n' in the table means the nth bit.)

Table 98. Arithmetic operation between MADCTL & MADDEF

MADCTL(0Bh)	MADDEF(F6h)	IC Internal setting value
0	0	0
0	1	1
1	0	1
1	1	0

Note. MADDEF is F6h's 1st Parameter.

In the case of MADDEF set to "00h," the result of memory access is controlled as show below.

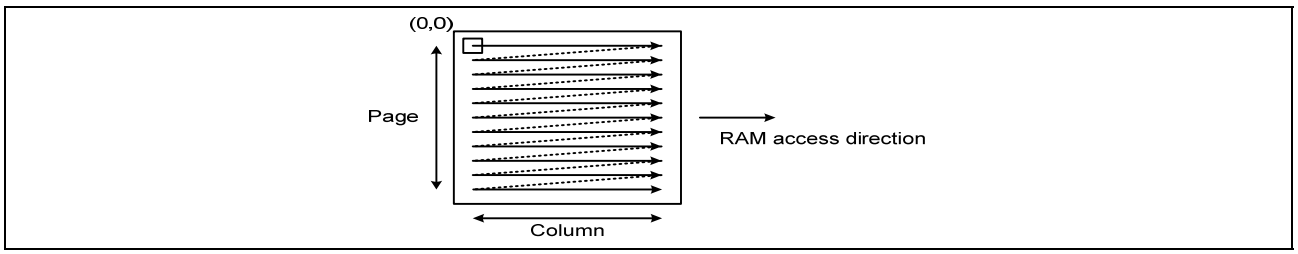


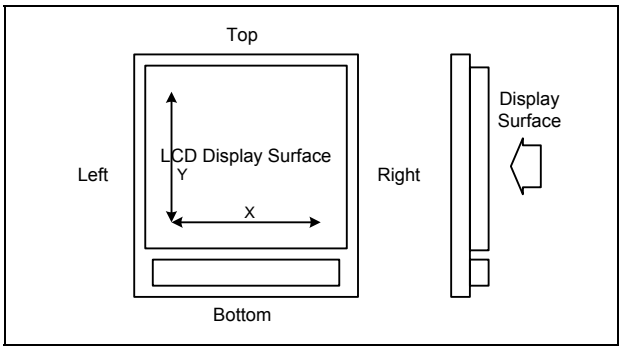
Figure 119. An example of MADDEF(00h)

Refer to the top-bottom / left-right relationship. (The non-bump plane is the surface.)

If the driver IC is left-mounted or right-mounted due to the device structure, the display data RAM to LCD display data readout and gate scan direction should be set left-right rather than top-bottom.

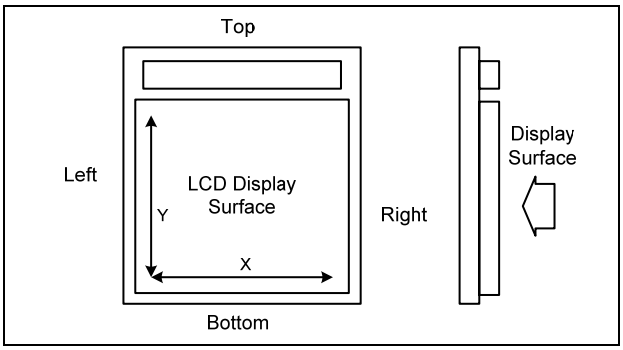
Table 99. Cases of panel position mounted IC

Case of bottom-mounted IC



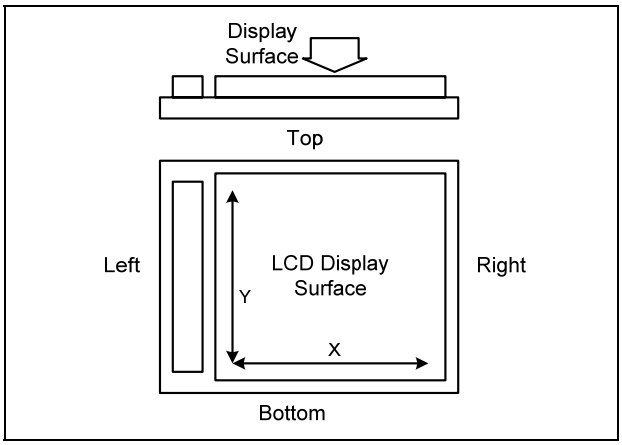
(Example) MADDEF(00h)	
RAM address (0,0) Position	Left-top
RAM Access Direction	Column Direction
Column	X direction
Page	Y direction
RAM→LCD readout direction	Top to Bottom
Gate line scan Direction	Top to Bottom

Case of top-mounted IC



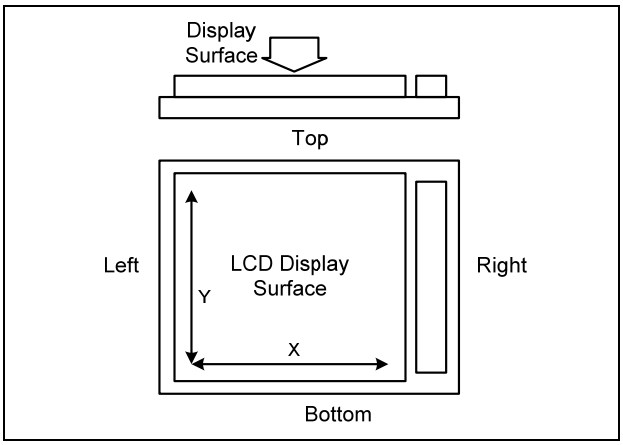
(Example) MADDEF(D0h)	
RAM address (0,0) Position	Left-top
RAM Access Direction	Column Direction
Column	X direction
Page	Y direction
RAM→LCD readout direction	Top to Bottom
Gate line scan Direction	Top to Bottom

Case of left-mounted IC



(Example) MADDEF(A0h)	
RAM address (0,0) Position	Left-top
RAM Access Direction	Column Direction
Column	X direction
Page	Y direction
RAM→LCD readout direction	Right to Left
Gate line scan Direction	Right to Left

Case of right-mounted IC



(Example) MADDEF(60h)	
RAM address (0,0) Position	Left-top
RAM Access Direction	Column Direction
Column	X direction
Page	Y direction
RAM→LCD readout direction	Left to Right
Gate line scan Direction	Left to Right

4.5.4.3. 0-Address Position and RAM Access Scan Direction

Refer to MADCTL (MADDEF=00h)

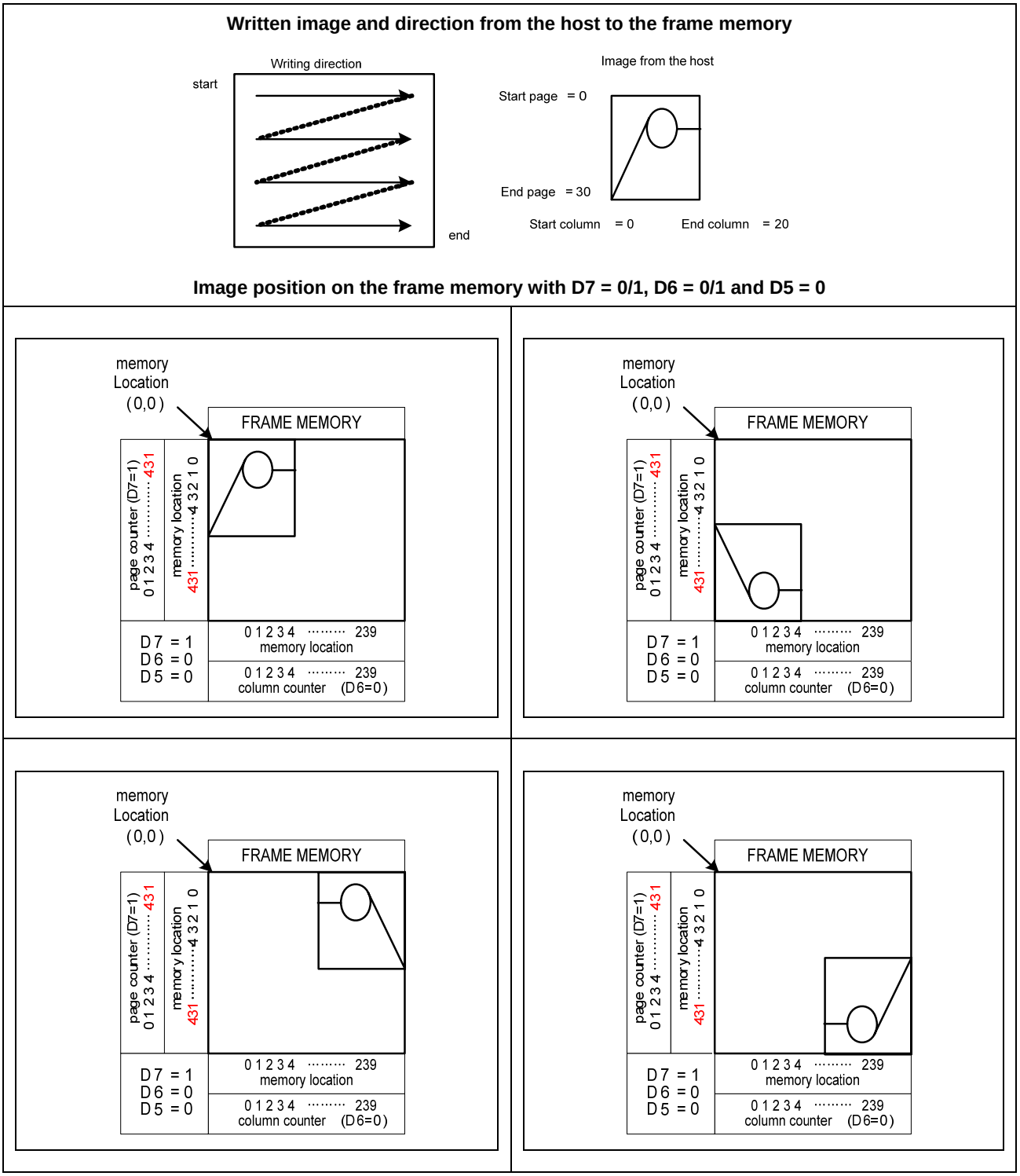


Figure 120. 0-Address position and RAM access scan direction(D5=0)

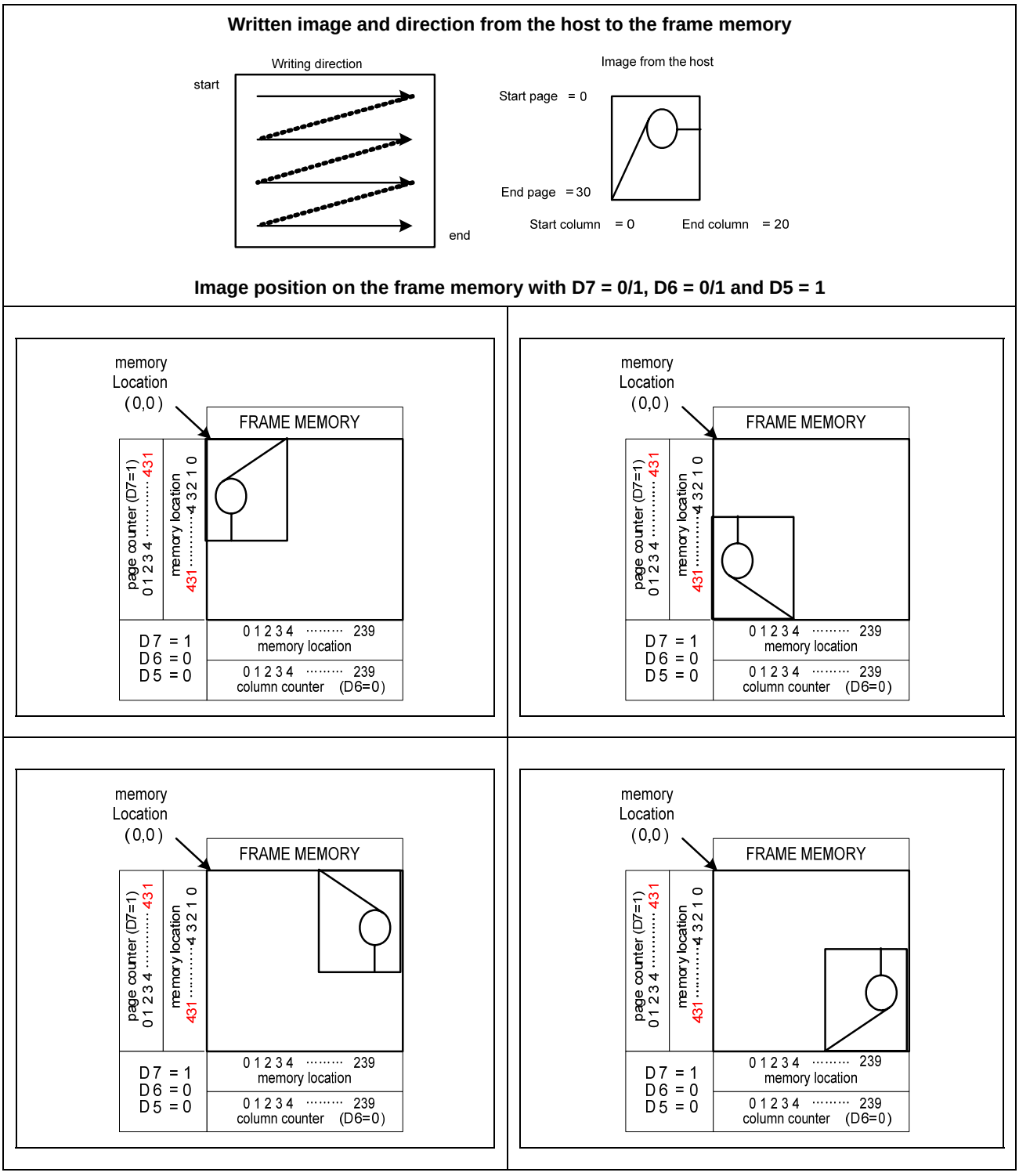


Figure 121. 0-Address position and RAM access scan direction(D5=1)

4.5.4.4. LCD Read Scan Direction and Common Scan Direction

Refer to MADCTL (MADDEF = 00h)

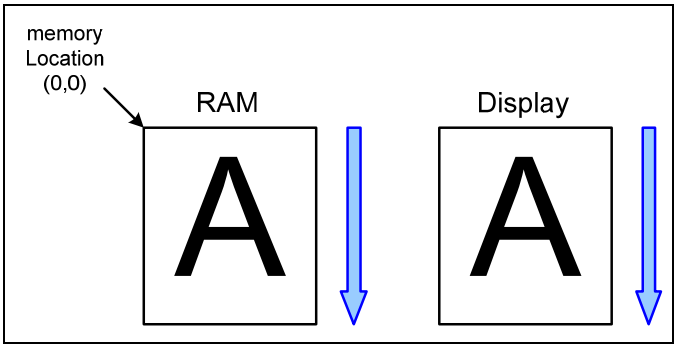
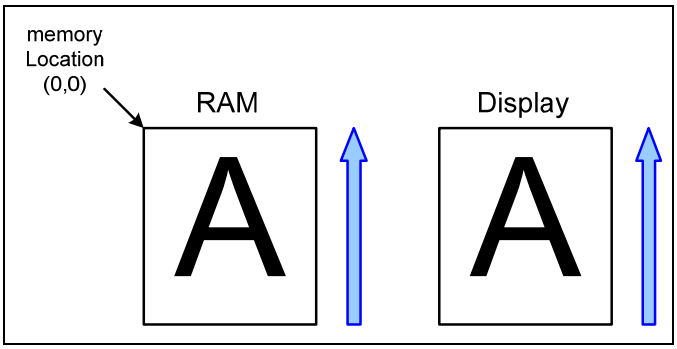
D4 : Memory Scan Direction	0	Top to Bottom	
	1	Bottom to Top	

Figure 122. LCD read scan direction and common scan direction

4.5.4.5. Partial Area and Scan Direction

Refer to MADCTL, PTLAR

A. Partial Mode

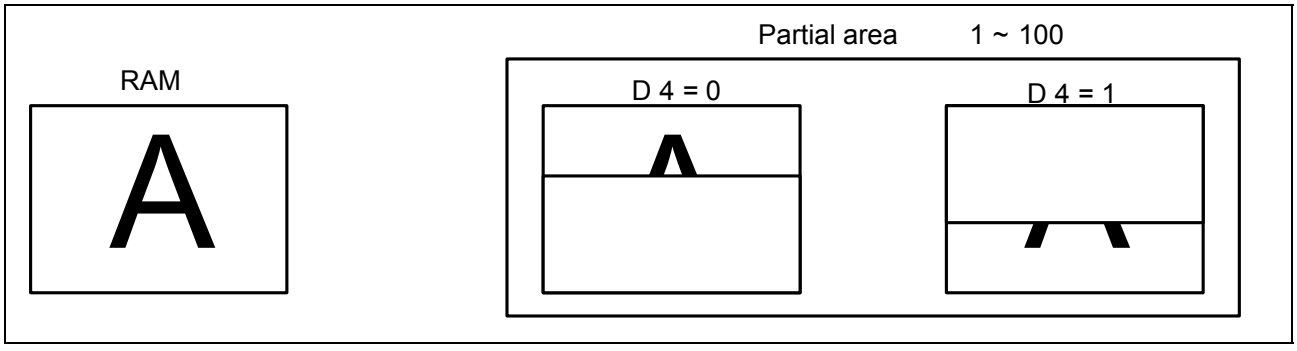


Figure 123. Partial area and scan direction

4.6. RESET

4.6.1. Registers

Table 100. The default value of the register set

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Column: Start Address (SC)	0000h	0000h	0000h
Column: End Address (EC)	00EFh	00EFh	00EFh (239d) (when MADCTL's D5=0) 01AFh (431d) (when MADCTL's D5=1)
Page: Start Address (SP)	0000h	0000h	0000h
Page: End Address (EP)	01AFh (431d)	01AFh (431d)	01AFh (431d) (when MADCTL's D5=0) 00EFh (239d) (when MADCTL's D5=1)
Partial: Start Address (SR)	0000h	0000h	0000h
Partial: End Address (ER)	01AFh	01AFh	01AFh
Color Pixel Fomat	24bit/pixel	24bit/pixel	No change
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode	00h (Mode1)	00h (Mode1)	00h (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB/MH)	0/0/0/0/0/0	0/0/0/0/0/0	No Change
RDDPM (0Ah)	08h	08h	08h
RDDMADCTL (0Bh)	00h	00h	No Change
RDDCOLMOD(0Ch)	24bit/pixel	24bit/pixel	No change
RDDSM (0Eh)	00h	00h	00h
RDDSDR (0Fh)	00h	00h	00h
ID1 (DAh)	(MTP values)	(MTP values)	(MTP values)
ID2 (DBh)	(MTP values)	(MTP values)	(MTP values)
ID3 (DCh)	(MTP values)	(MTP values)	(MTP values)
WRDISBV(51h)	00h	00h	00h
RDDISBV(52h)	00h	00h	00h
WRCTRLD(53h)	00h	00h	00h

Item	After Power On	After Hardware Reset	After Software Reset
RDCTRLD(54h)	00h	00h	00h
WRCABC(55h)	00h	00h	00h
RDCABC(56h)	00h	00h	00h
WRCABCMB(5Eh)	00h	00h	00h
RDCABCMB(5Fh)	00h	00h	00h
MIECTL(CAh)	80_80_10h	80_80_10h	80_80_10h
BCMODE(CBh)	01h	01h	01h

Note1. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied.

Note2. Powered-On Reset finishes within 500μs after both VDD3 & VCI are applied.

Note3. For detail informatiom of TE Mode 1 , refer to the section 4.12

Table 101. The default value of the register set 1(level II)

Item	Default value
MIECTL2(CCh)	20_01_3F_00_EFh
MIECTL3(CDh)	03_14h
MTPCTL (D0h)	0C_05h
WRVCMOC (D1h)	00h
WRVMLOC (D2h)	00h
WRGVDOC (D3h)	00h
WRID (D4h)	00_00_00h
RDOFFSETC (D5h)	MTP[39:24]
WRPWD (F0h)	30h
DISCTL (F2h)	1316_0308_0808_0810_0016_16h
PWRCTL (F3h)	8000_0000_0000_002Ch
VCMCTL (F4h)	0000_0000_44h
SRCCTL (F5h)	1000_03f0_301fh
IFCTL (F6h)	0080_0010h
RPGAMCTL(F7h)	06h / 03h / 04h / 0Ah / 10h / 1Ah / 22h / 2Ch/ 13h / 12h / 1Dh / 11h / 02h / 22h / 22h
RNPGAMCTL(F8h)	06h / 03h / 04h / 0Ah / 10h / 1Ah / 22h / 2Ch/ 13h / 12h / 1Dh / 11h / 02h / 22h / 22h

Table 102. The default value of the register set 2

Item	Default value
GPGAMCTL(F9h)	06h / 03h / 04h / 0Ah / 10h / 1Ah / 22h / 2Ch/ 13h / 12h / 1Dh / 11h / 02h / 22h / 22h
GNPGAMCTL(FAh)	06h / 03h / 04h / 0Ah / 10h / 1Ah / 22h / 2Ch/ 13h / 12h / 1Dh / 11h / 02h / 22h / 22h
	06h / 03h / 04h / 0Ah / 10h / 1Ah / 22h / 2Ch/ 13h / 12h / 1Dh / 11h / 02h / 22h / 22h
BPGAMCTL(FBh)	06h / 03h / 04h / 0Ah / 10h / 1Ah / 22h / 2Ch/ 13h / 12h / 1Dh / 11h / 02h / 22h / 22h

Table 103. The default value of the register set 2

Item	Default value
BNPGAMCTL(FCh)	06h / 03h / 04h / 0Ah / 10h / 1Ah / 22h / 2Ch/ 13h / 12h / 1Dh / 11h / 02h / 22h / 22h
GATECTL(FDh)	11h

4.6.2. Module input/output/Bi-direction (I/O) Pads

4.6.2.1. Output or Bi-directional (I/O) Pads

Table 104. Reset states of output pads

Output or Bi-directional pads	When RESX is Low	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low	Low
BC	Low	Low	Low	Low
BC_CTL	High	High	High	High
DB23 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
SDO (Output driver)	Low	Low	Low	Low

Note. There will be no output from DB23-DB0 during Power On/Off sequence, Hardware Reset and Software Reset

4.6.2.2. Input Pads

Table 105. Reset states of input pads

Input pads	During Power On Process	After Power On	When RESX is Low	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See Section 4.1.1	Input valid	-	Input valid	Input valid	See Section 4.1.1
CSX	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input invalid
DCX	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input invalid
DB23 to DB0 (Input driver)	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input invalid
SDA (Input driver)	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input invalid
HSYNC	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input valid (RGB IF & DM=1) Input invalid (The other cases)
VSYNC	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input valid (RGB IF & DM=1or VSM = 1)

						Input invalid (The other cases)
DOTCLK	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input valid (RGB IF & DM=1) Input invalid (The other cases)
ENABLE	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input invalid

4.7. SLEEP OUT –COMMAND AND SELF-DIAGNOSTIC FUNCTIONS OF THE DISP LAY MODULE

4.7.1. Register Loading Detection

Sleep-out command is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

Data of the EEPROM and register values of driver IC are compared as shown in the figure below. If those both values (EEPROM and register values) are the same, there is an inverted (=increased by 1) bit, which is defined in command "Read Display Self-Diagnostic Result (0Fh)" (=RDDSDR) (The used bit of this command is D7). If both those values are not same, this bit (D7) is not inverted (= not increased by 1).

The flowchart of the function described above is as follows.

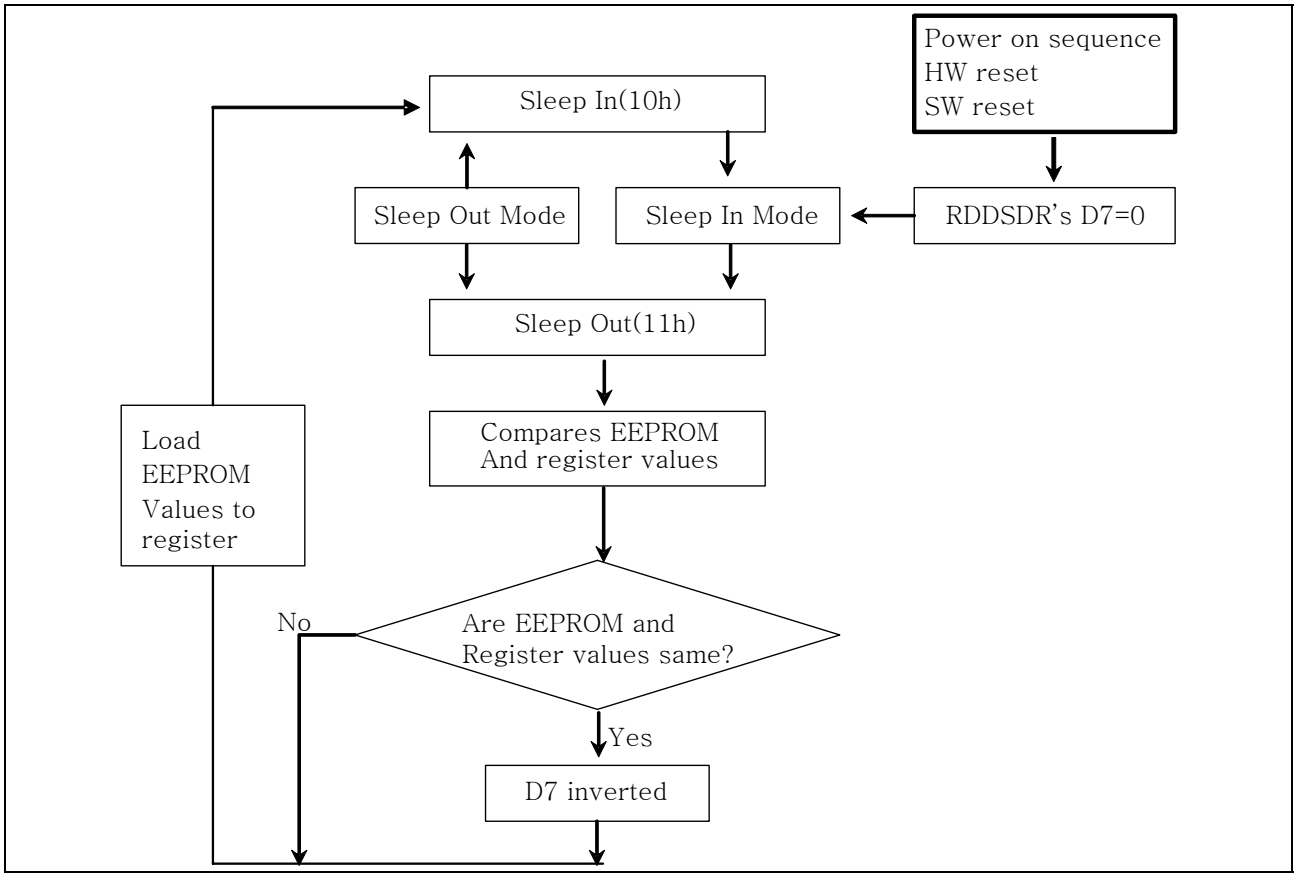


Figure 124. Flowchart of register loading detection

Note. There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DDh), by the display module.

4.7.2. Functionality Detection

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command "Read Display Self- Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= not increased by 1).

The flow chart for this internal function is following:

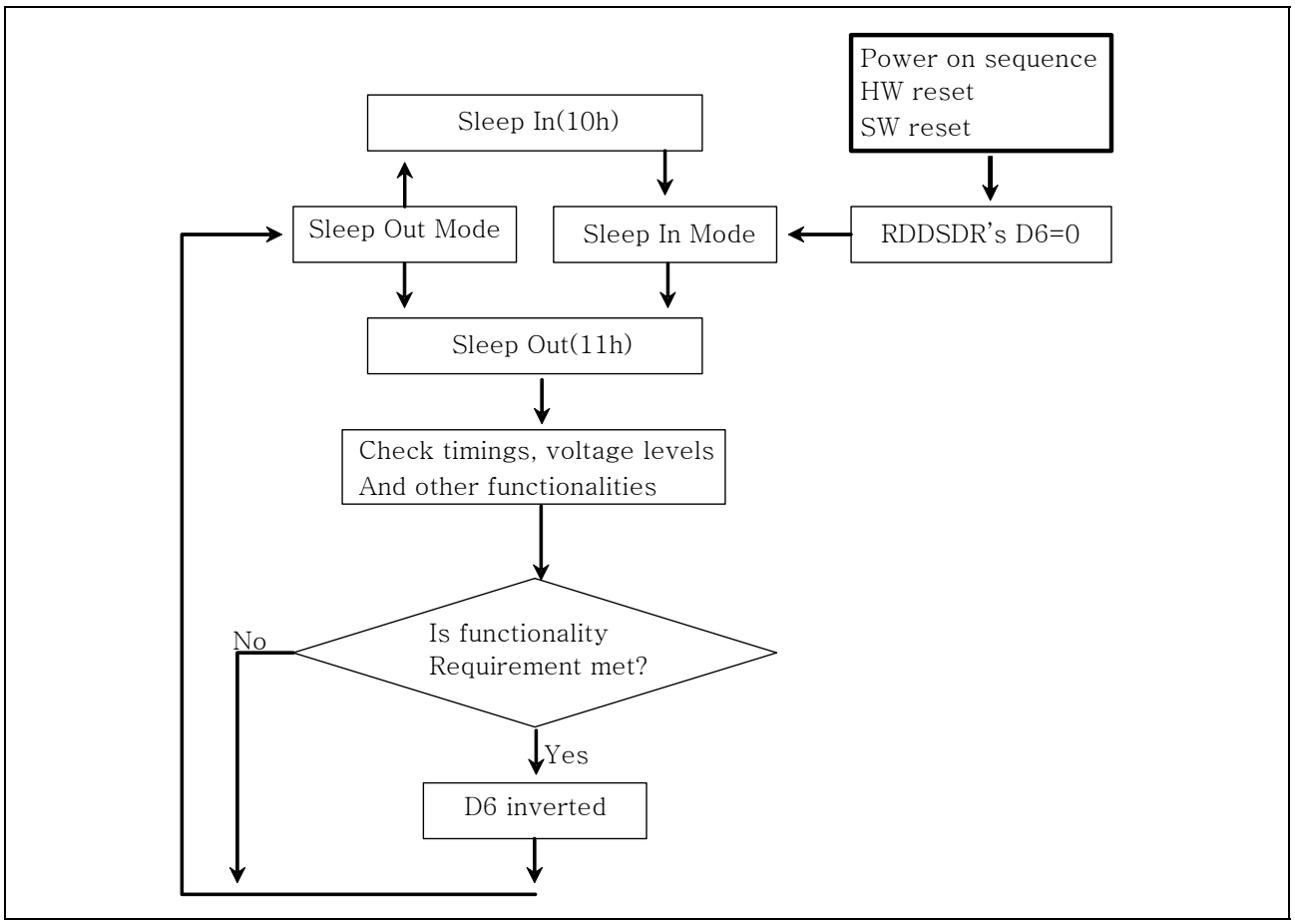


Figure 125. Flowchart of functionality detection

Note 1. There is needed 120msec after Sleep Out –command, when there is changing from Sleep In –mode to Sleep Out –mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out –mode.

Note 2. If VGH level is lower than 12V according to VCI1 & BT settings, D6 register cannot be inverted.

4.8. NVM MEMORY CONTROL

4.8.1. MTP Control

4.8.1.1. MTP Control Flow

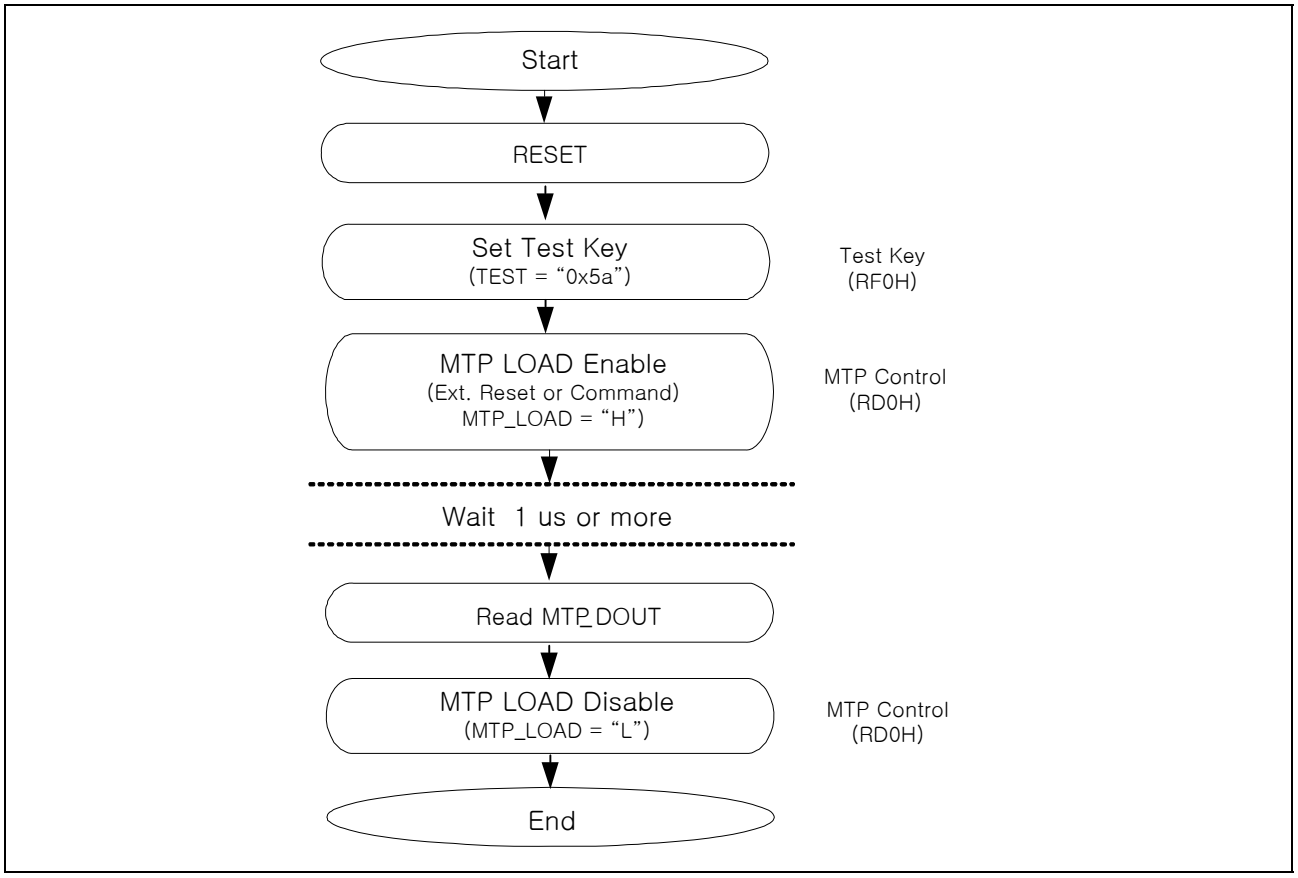


Figure 126. Flow of MTP load / Read

4.8.1.2. Internal Control

A. Using VCI for MTP

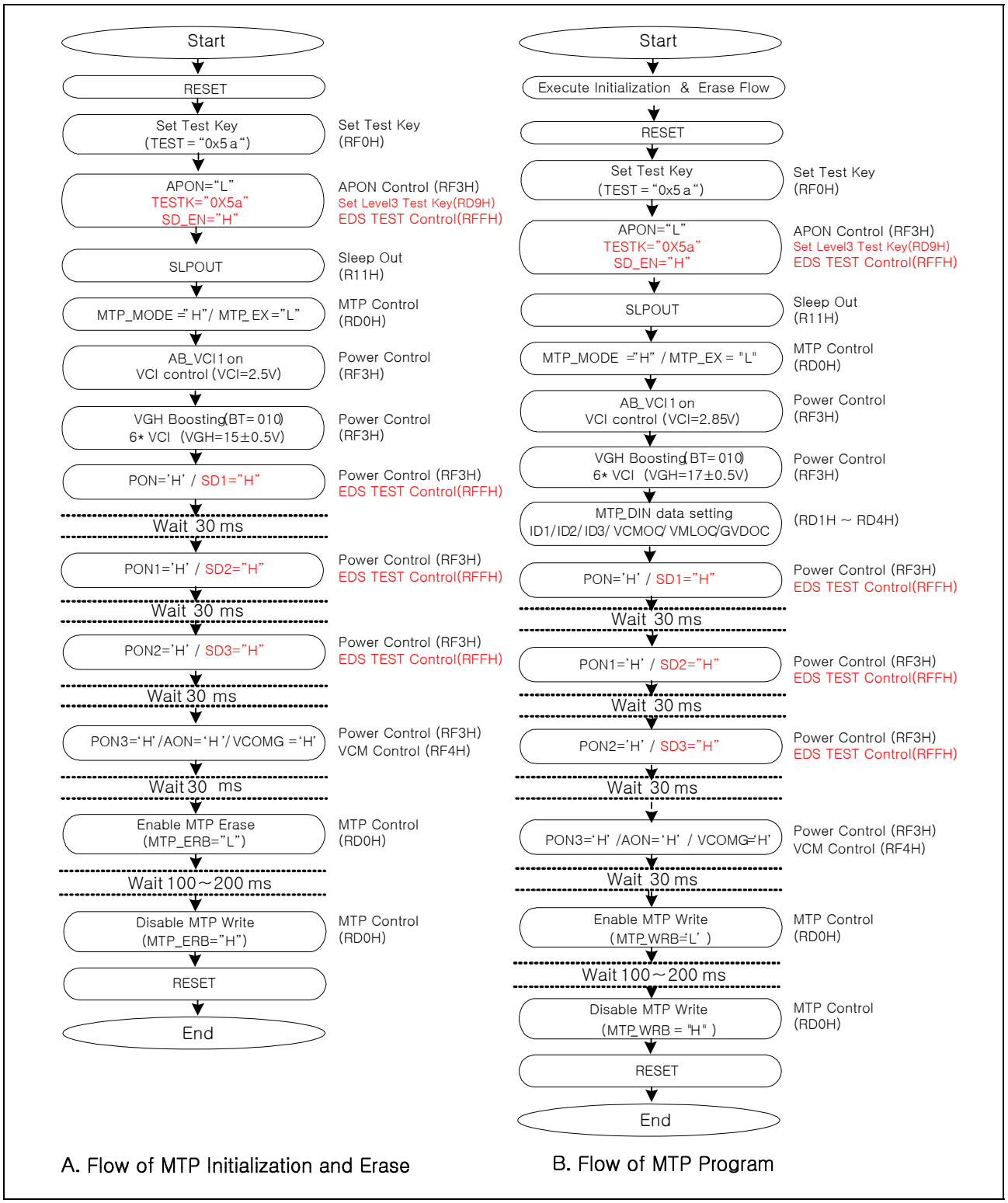


Figure 127. MTP initialization, erase and program (internal mode using VCI)

B. Using VCI1 for MTP

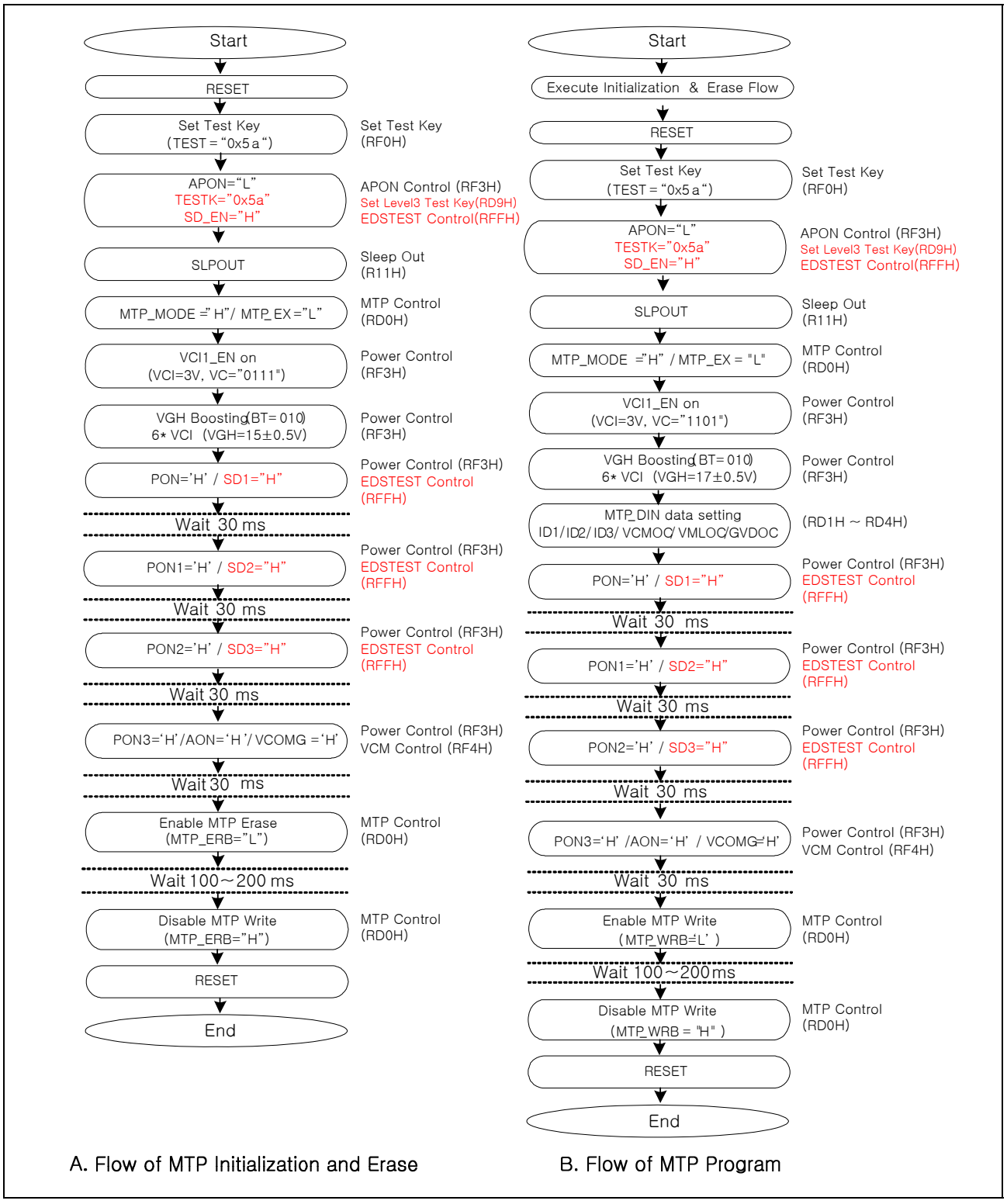


Figure 128. MTP initialization, erase and program (internal mode using VCI1)

4.8.1.3. External Control

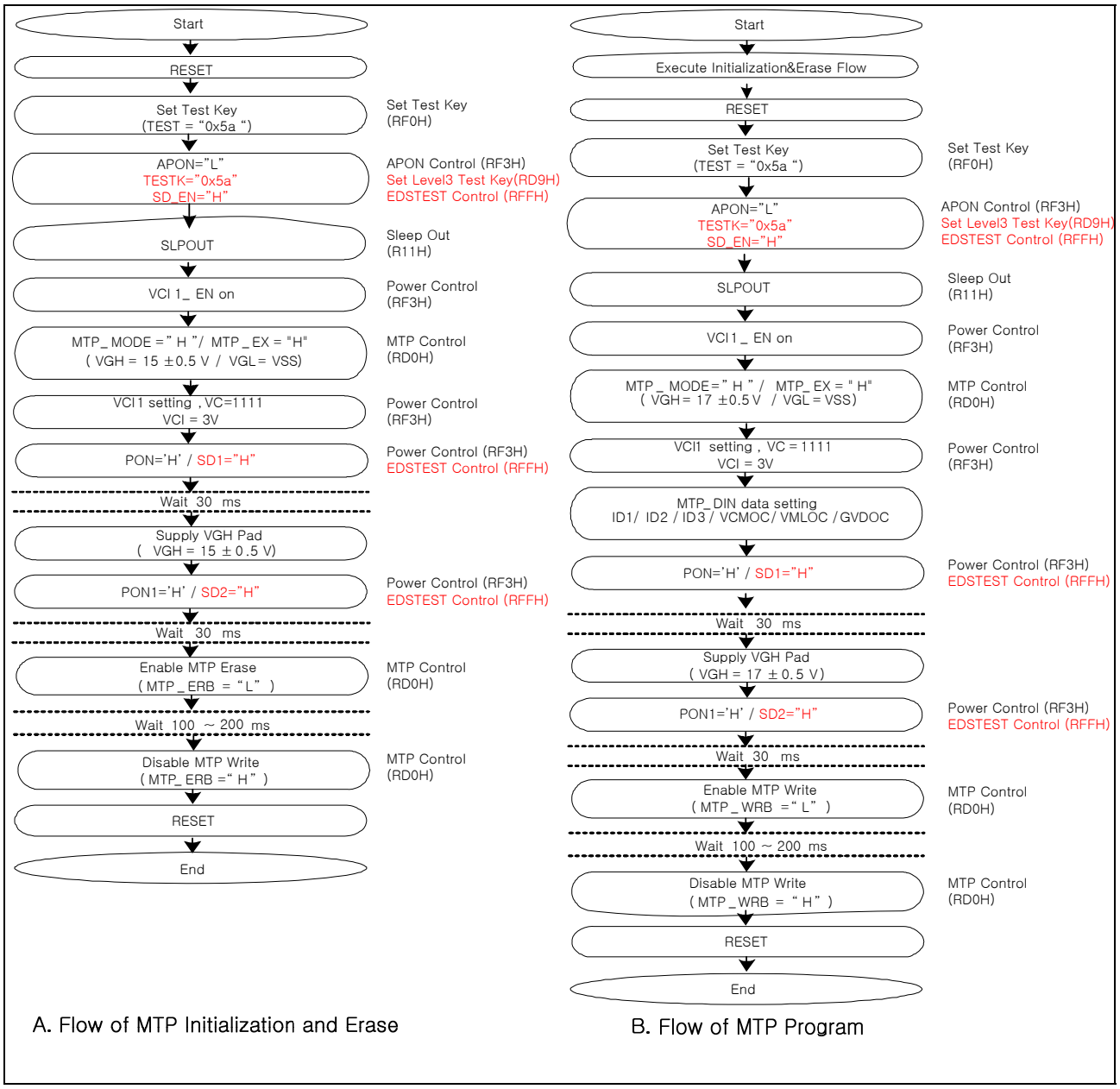


Figure 129. MTP initialization, erase and program (external mode)

4.8.1.4. Timing of MTP Control

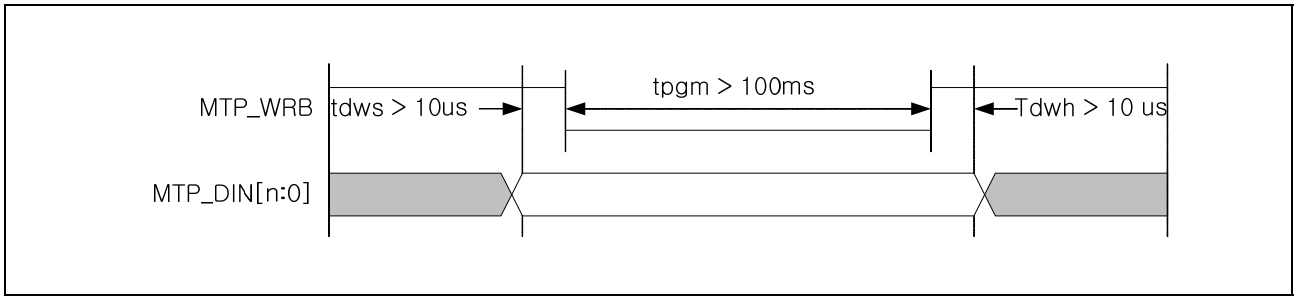


Figure 130. Timing of MTP program

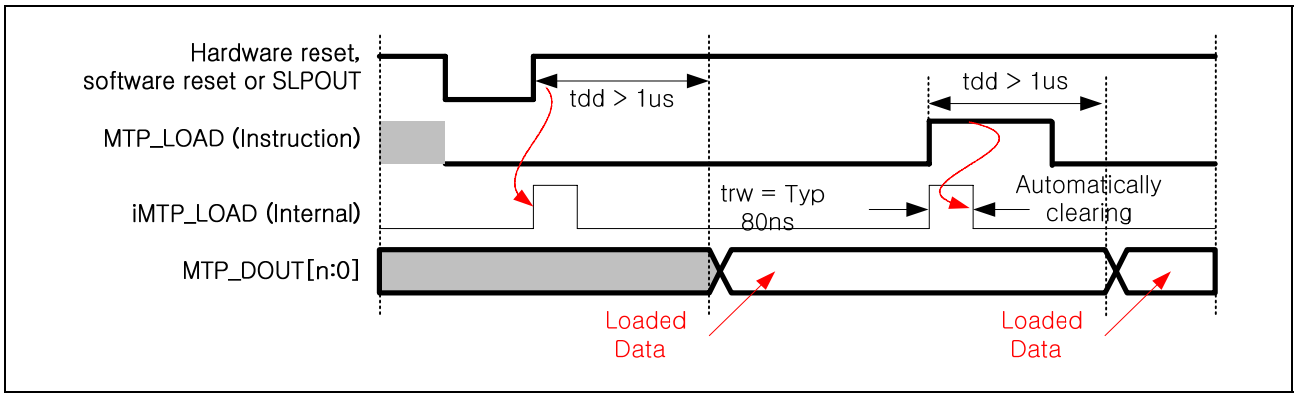


Figure 131. Timing of MTP load

Note :

1. The shipping value (=initialized value) of MTP ROM : All “0”.

2. The maximum number of re-writable times of MTP ROM : 20 times.

4.9. 8-COLOR DISPLAY MODE

An 8-color display mode is also provided by the S6D04D1. In an 8-color mode of operation, gray scale voltage generation (V0-V255) is halted to conserve power and the values of gamma micro-adjustment registers (PKP and PKN) become invalid. Also, the only MSB of each R, G, and B in the Frame Memory are displayed. (Refer to 39h Command)

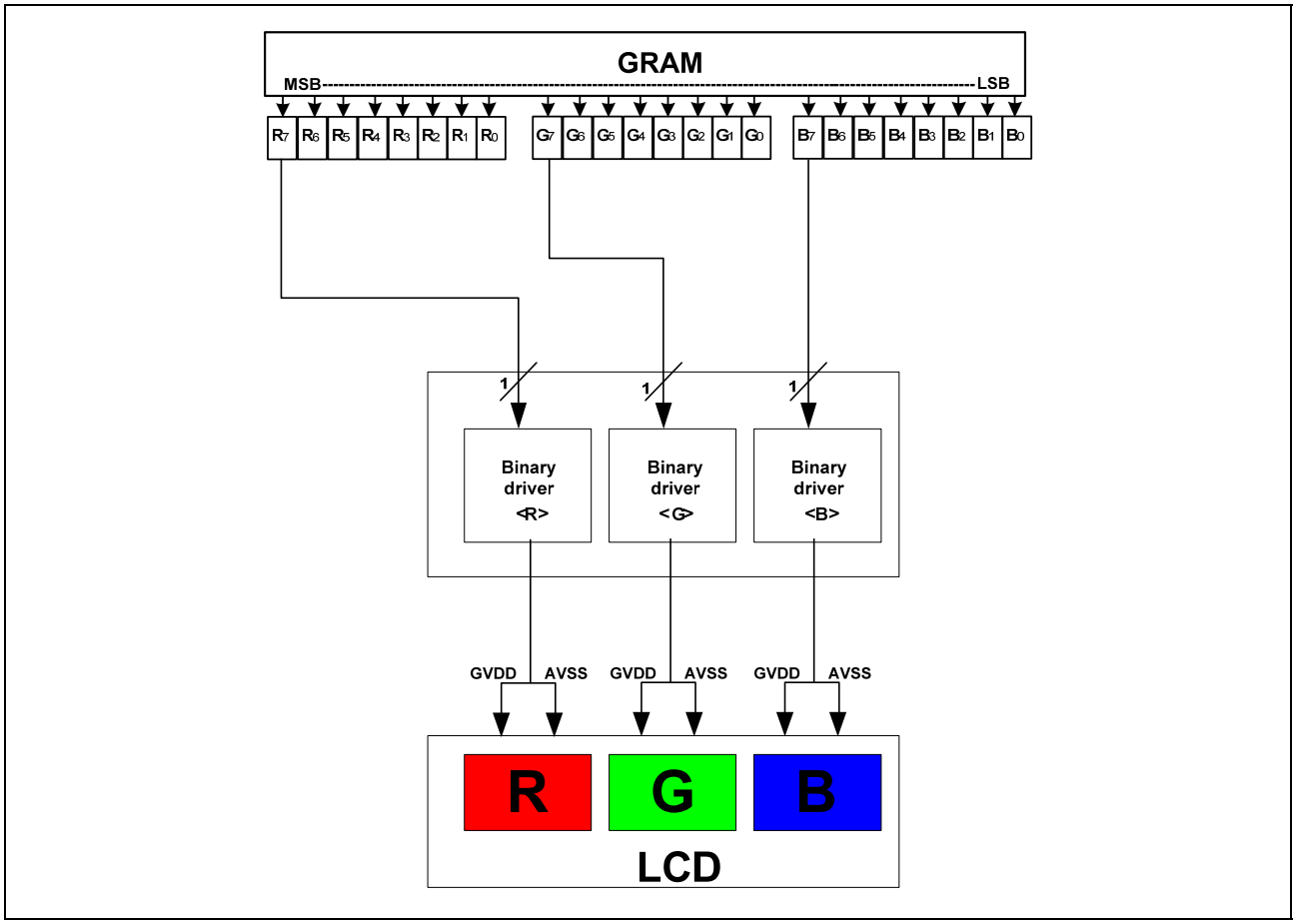


Figure 132. 8-color display control.

4.10. INSTRUCTION SETUP FLOW

4.10.1. Initializing the Built-In Power Supply Circuits

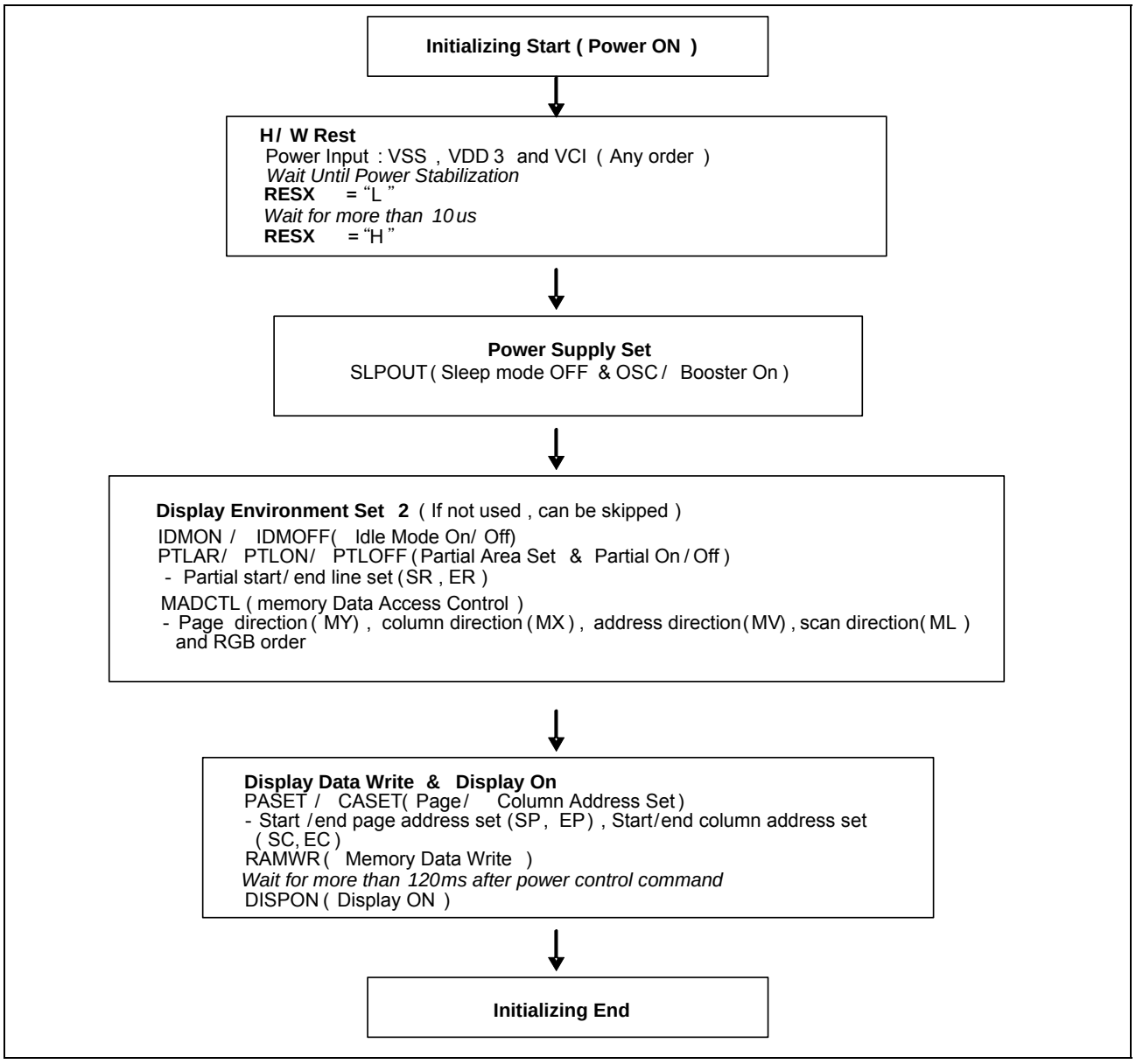


Figure 133. Initializing the built-in power supply circuits

The initializing sequence does not have any effect on the display. The display is in its normal background color during the initialization.

4.10.2. Power OFF Sequence

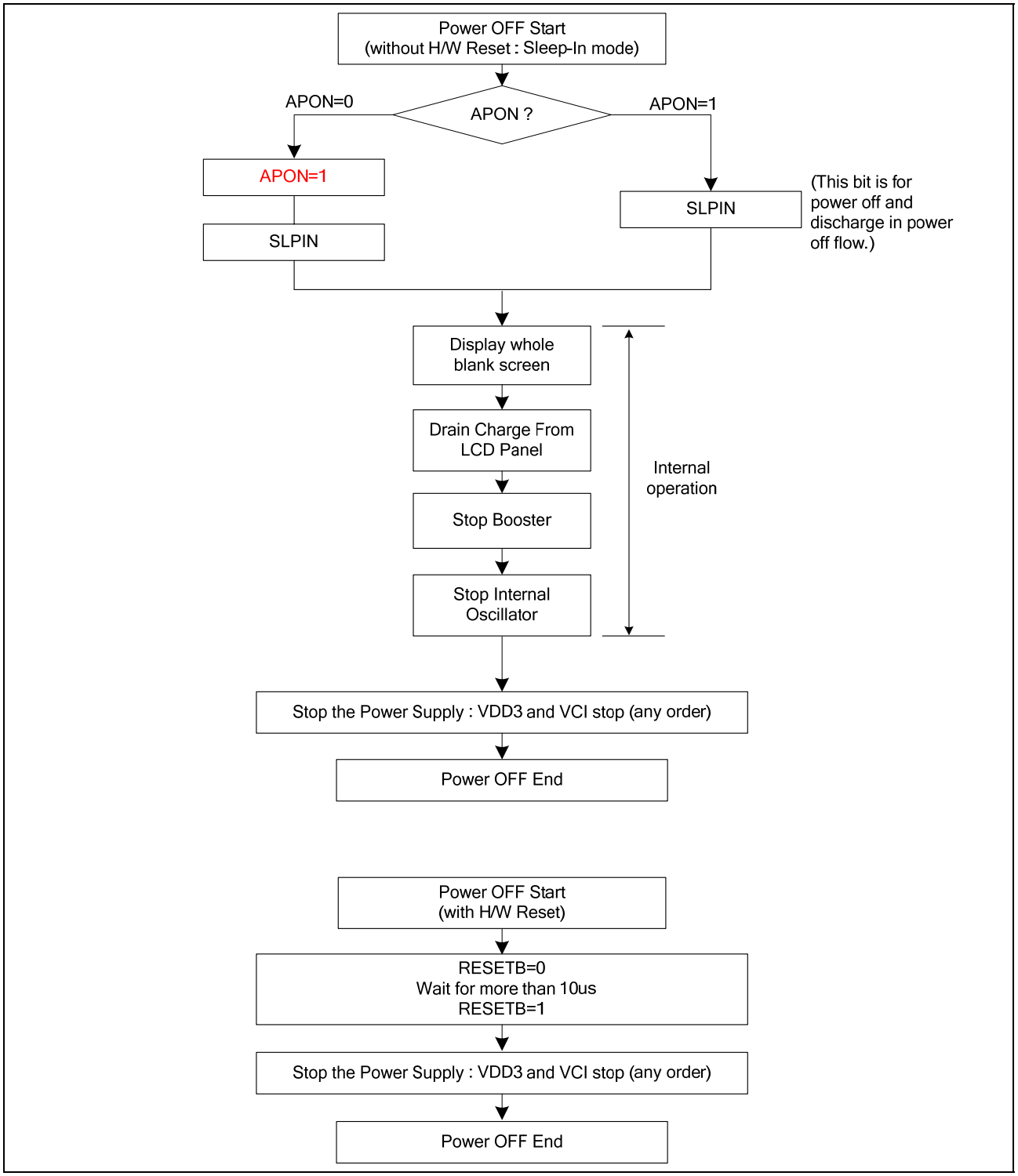


Figure 134. Power off sequence

4.11. TEARING EFFECT OUTPUT LINE

The Tearing Effect output line supplies a Panel synchronization signal to the MCU. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command and interface type (IM[2:0] pads). The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

Note. In MPU I/F type2 mode, TE pad is not used for tearing effect signal. Refer to section 4.12.3

4.11.1. Tearing Effect Line Modes

Mode 1. the Tearing Effect Output signal consists of V-Blanking Information only

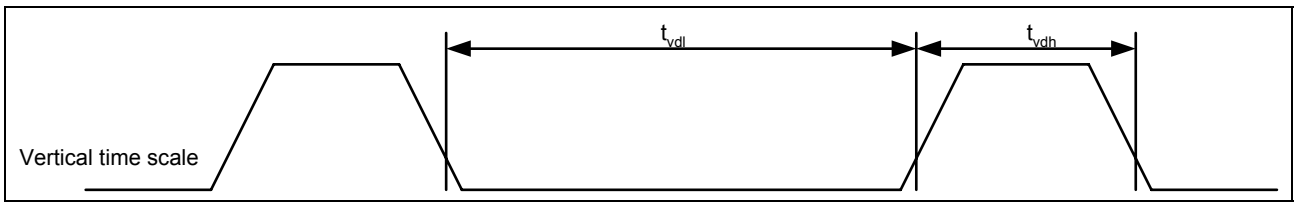


Figure 135. Tearing effect output signal consists of v-blanking information only

t_{vdh} = The LCD display is not updated from the Frame Memory

t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2. the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 432H-sync pulses per field.

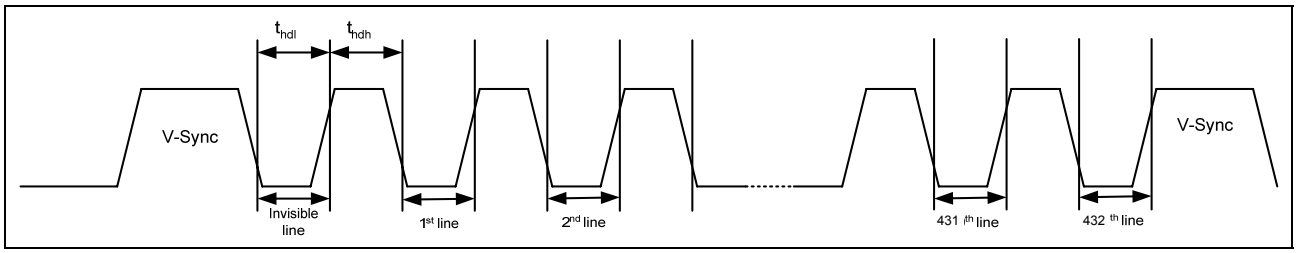


Figure 136. Tearing effect output signal consists of v-blanking and g-blanking information

t_{vdh} = The LCD display is not updated from the Frame Memory

t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line- see above)

t_{hdh} = The LCD display is not updated from the Frame Memory

t_{hdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see above)

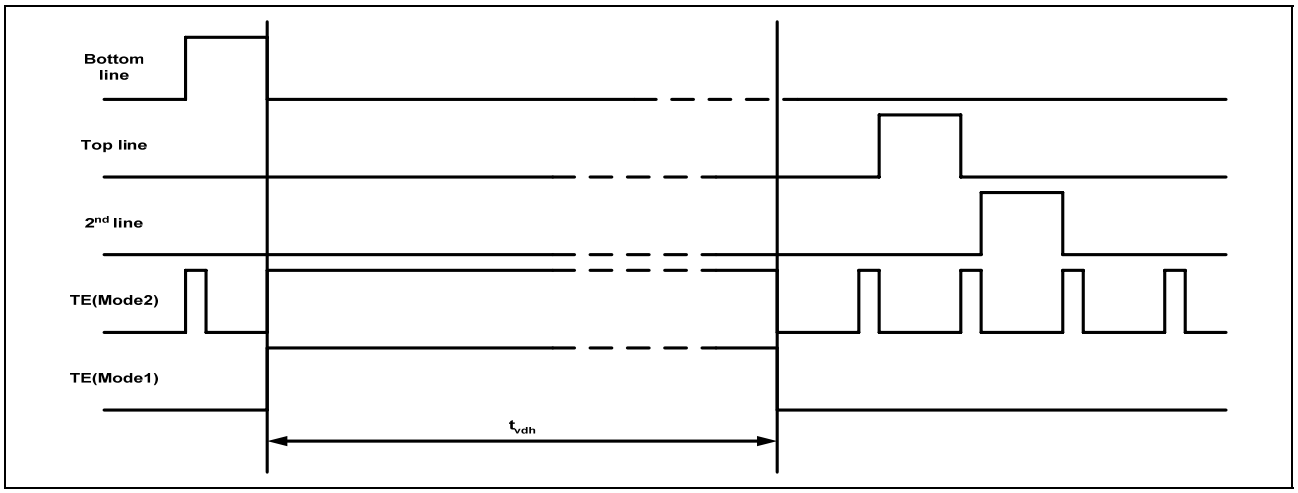


Figure 137. Tearing effect output signal

Note. During Sleep In Mode, The Tearing Output Pin is active Low

4.11.2. Tearing Effect Line Timings

The Tearing effect signal is described below.

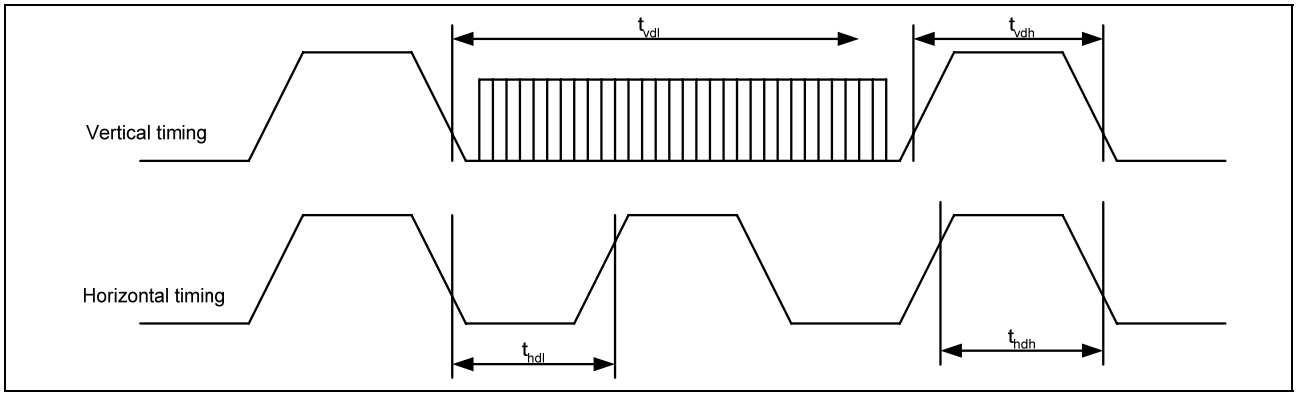


Figure 138. Tearing effect output signal timing

Table 106. AC characteristics of tearing effect signal (IDLE mode off)

Symbol	Parameter	min	max	unit	Description
t_{vdl}	Vertical timing low duration	-	-	ms	
t_{vdh}	Vertical timing high duration	1000	-	us	
t_{hdl}	Horizontal timing low duration	-	-	us	
t_{hdh}	Horizontal timing high duration	-	500	us	

Note1. The timings in above Table apply when MADCTL D4=0 and D4=1

Note2. tvdh is controlled by VBP and VFP. To meet the timing in above table, BP + FP must be bigger than 21 (Frame Freq. 60Hz)

Note3. When TE mode 2 in MCU Interface, the high period of TE signal in horizontal timing can be controlled in HBP+2.

The rise and fall time of TE signal is stipulated to be equal to or less than 15ns.

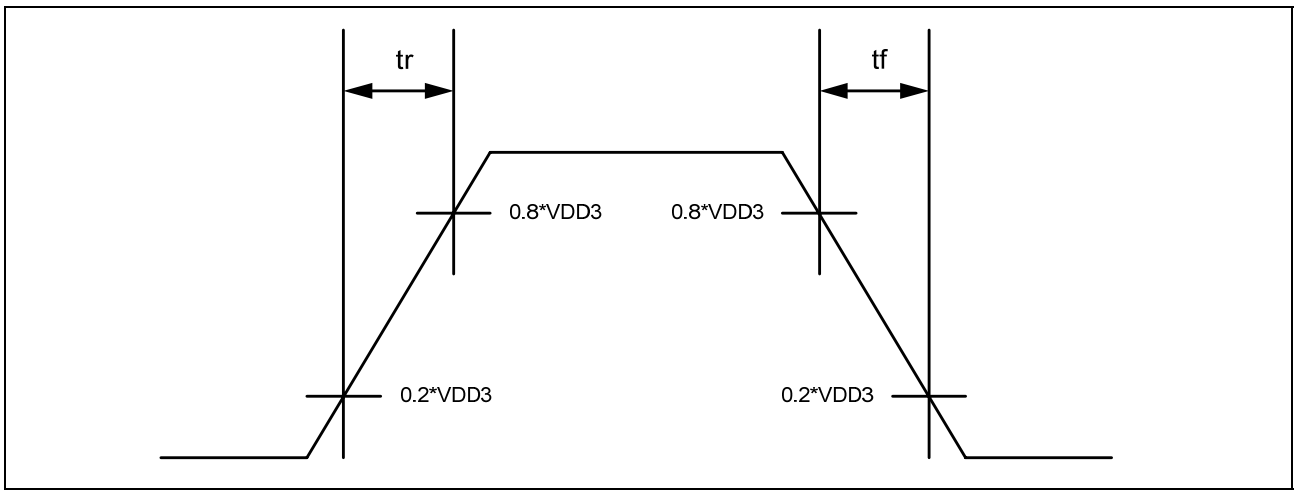


Figure 139. Rise and fall time of TE signal

The Tearing Effect Output Line is fed back to the MCU and should be used as shown below to avoid Tearing Effect.

4.11.2.1. Example 1: MCU write is faster than panel read.

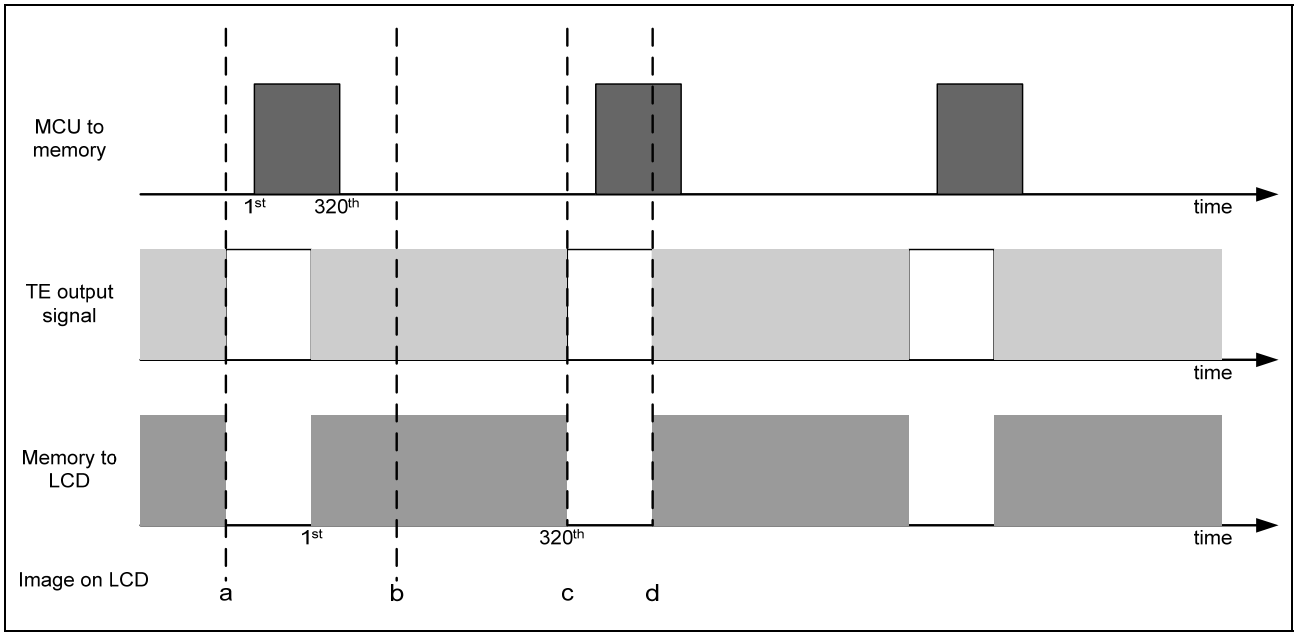


Figure 140. Method 1 to avoid tearing effect

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image.

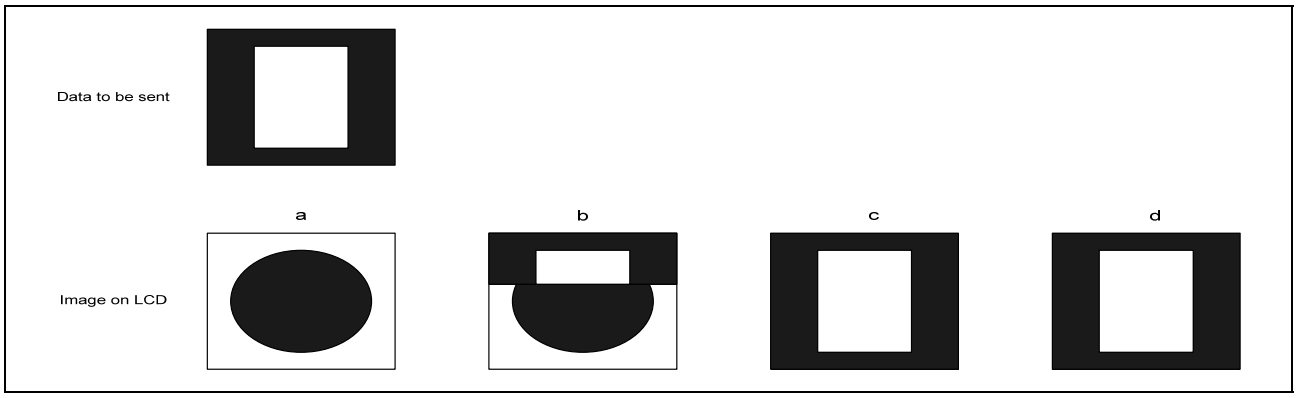


Figure 141. Panel image refreshment of method 1

4.11.2.2. Example 2 : MCU write is slower than panel read.

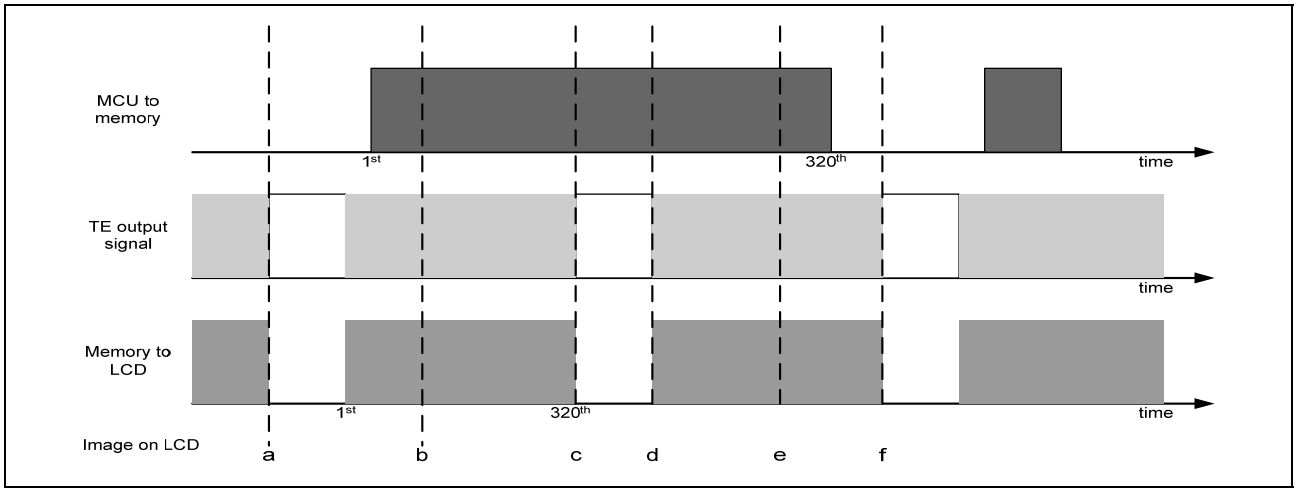


Figure 142. Method 2 to avoid tearing effect

The MCU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and to finish downloading during the subsequent Frame before the Read Pointer “catches” the MCU to Frame memory write position.

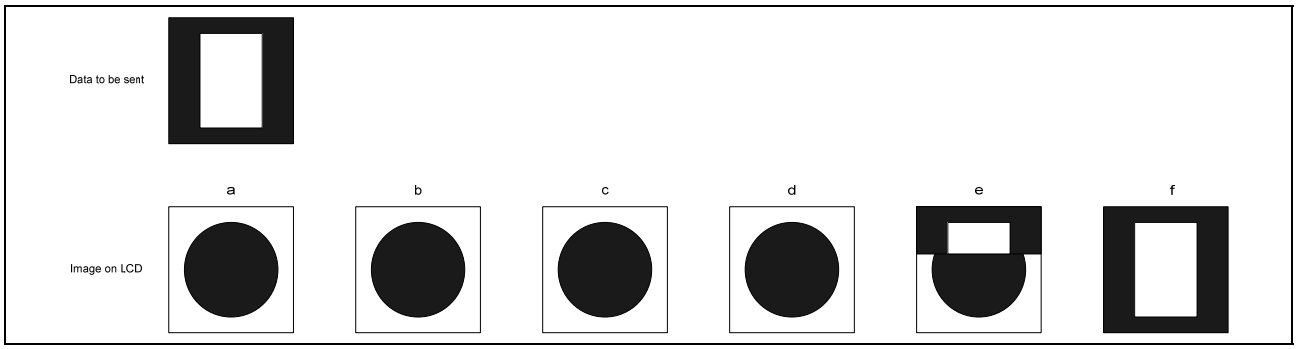


Figure 143. Panel image refreshment of method 2

4.12. MIE FUNCTION

S6D04D1 has a special image enhancement function. MIE (Mobile Image Enhancement) reduces power consumption of backlight unit by adaptive enhancement of luminance and contrast. According the brightness enhancement rate of input image, the power reduction of BLU is controlled automatically.

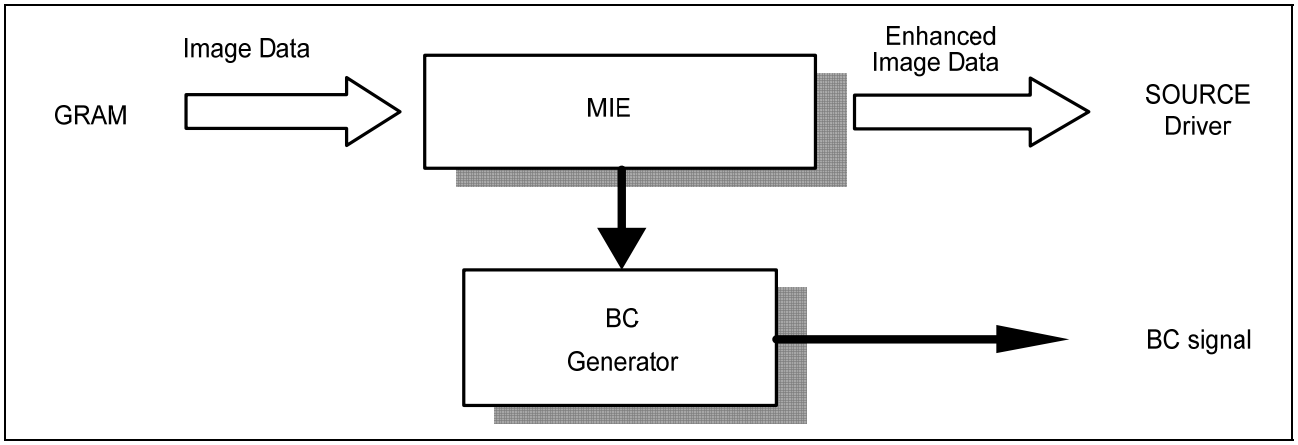


Figure 144. Flowchart of MIE function

When MIE is enabled, MIE dynamically changes the brightness of backlight unit by on-chip BC(Backlight Control) Generator. Host can control the rate of BLU power reduction by setting RRC value (Refer to CAh Command.)

When MIE is enabled, the enhanced data is outputted to Source block. Host processor should select movie or still-Image mode (Refer to 55h Command).

4.13. SHARPNESS ENHANCEMENT

Sharpening emphasizes the details in an image. Because this function operates calculating data of pixel, images with sharp outlines can be realized regardless of still or moving images. (Refer to C6h Command.)

The following figure shows the each stages of operational sequence.

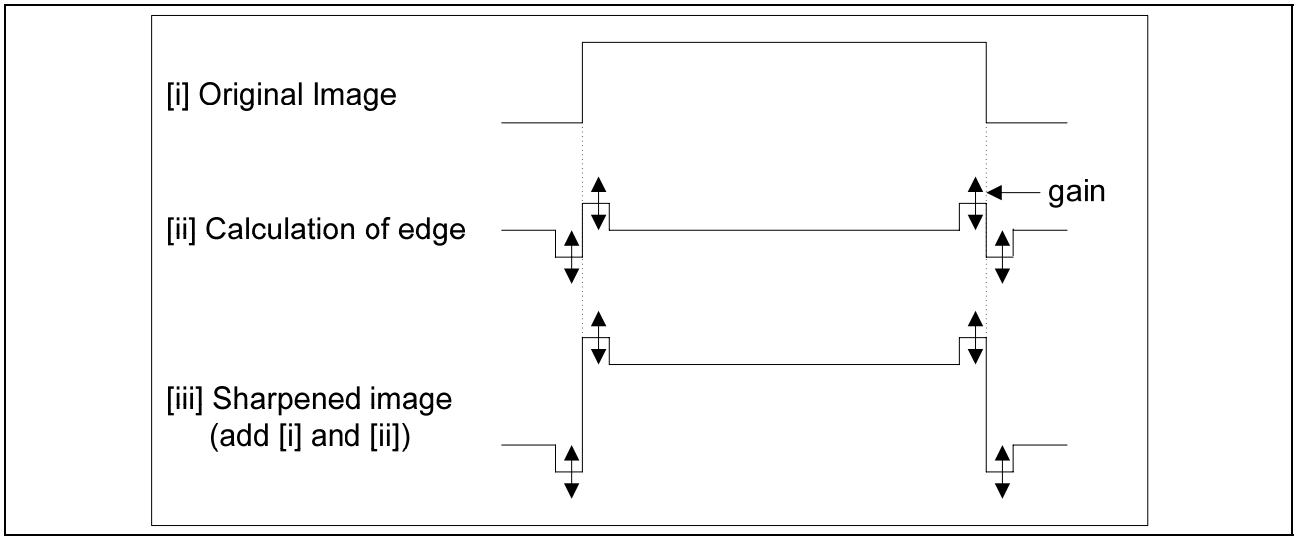


Figure 145. shows the each stages of operational sequence

The characteristics of algorithm used in this function may not be fit some type of data to realize wanted result. Please confirm images after sharpening operation

CHAPTER 5

COMMAND

5 COMMAND

5.1. COMMAND LIST

5.1.1. Level 1 : Function Command

Table 107. Instruction code

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Reference
NOP	W	0	0	0	0	0	0	0	0	0	00h	5.2.1
SWRESET	W	0	0	0	0	0	0	0	0	1	01h	5.2.2
RDDIDIF	R	0	0	0	0	0	0	1	0	0	04h	5.2.3
		1	-	-	-	-	-	-	-	-		
		1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		
		1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		
		1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		
RDDST	R	0	0	0	0	0	1	0	0	1	09h	5.2.4
		1	-	-	-	-	-	-	-	-		
		1	D31	D30	D29	D28	D27	D26	D25	0		
		1	0	D22	D21	D20	D19	D18	D17	D16		
		1	0	0	0	0	0	D10	D9	0		
		1	0	0	D5	0	0	0	0	0		
RDDPM	R	0	0	0	0	0	1	0	1	0	0Ah	5.2.5
		1	-	-	-	-	-	-	-	-		
		1	D7	D6	D5	D4	D3	D2	0	0		
RDD MADCTL	R	0	0	0	0	0	1	0	1	1	0Bh	5.2.6
		1	-	-	-	-	-	-	-	-		
		1	D7	D6	D4	D4	D3	D2	0	0		
RDD COLMOD	R	0	0	0	0	0	1	1	0	0	0Ch	5.2.7
		1	-	-	-	-	-	-	-	-		
		1	0	D6	D5	D4	0	D2	D1	D0		
RDDSM	R	0	0	0	0	0	1	1	1	0	0Eh	5.2.8
		1	-	-	-	-	-	-	-	-		
		1	D7	D6	0	0	0	0	0	0		
RDDSDR	R	0	0	0	0	0	1	1	1	1	0Fh	5.2.9
		1	-	-	-	-	-	-	-	-		
		1	D7	D6	0	0	0	0	0	0		

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Reference
SLPIN	W	0	0	0	0	1	0	0	0	0	10h	5.2.10
SLPOUT	W	0	0	0	0	1	0	0	0	1	11h	5.2.11
PTLON	W	0	0	0	0	1	0	0	1	0	12h	5.2.12
NORON	W	0	0	0	0	1	0	0	1	1	13h	5.2.13
DISPOFF	W	0	0	0	1	0	1	0	0	0	28h	5.2.14
DISPON	W	0	0	0	1	0	1	0	0	1	29h	5.2.15
CASET	W	0	0	0	1	0	1	0	1	0	2Ah	5.2.16
		1	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8		
		1	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0		
		1	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8		
		1	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0		
PASET	W	0	0	0	1	0	1	0	1	1	2Bh	5.2.17
		1	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8		
		1	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0		
		1	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8		
		1	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0		
RAMWR	W	0	0	0	1	0	1	1	0	0	2Ch	5.2.18
		1	D7	D6	D5	D4	D3	D2	D1	D0		
RAMRD	R	0	0	0	1	0	1	1	1	0	2Eh	5.2.19
		1	-	-	-	-	-	-	-	-		
		1	D7	D6	D5	D4	D3	D2	D1	D0		
PTLAR	W	0	0	0	1	1	0	0	0	0	30h	5.2.20
		1	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8		
		1	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0		
		1	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8		
		1	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0		
TEOFF	W	0	0	0	1	1	0	1	0	0	34h	5.2.21
TEON	W	0	0	0	1	1	0	1	0	1	35h	5.2.22
		1	0	0	0	0	0	0	0	M		

Table 108. Instruction code (continued)

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Reference
MADCTL	W	0	0	0	1	1	0	1	1	0	36h	5.2.23
		1	D7	D6	D5	D4	D3	D2	0	0		
IDMOFF	W	0	0	0	1	1	1	0	0	0	38h	5.2.24
IDMON	W	0	0	0	1	1	1	0	0	1	39h	5.2.25
COLMOD	W	0	0	0	1	1	1	0	1	0	3Ah	5.2.26
		1	-	D6	D5	D4	-	D2	D1	D0		
RDID1	R	0	1	1	0	1	1	0	1	0	DAh	5.2.27
		1	-	-	-	-	-	-	-	-		
		1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		
RDID2	R	0	1	1	0	1	1	0	1	1	DBh	5.2.28
		1	-	-	-	-	-	-	-	-		
		1	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20		
RDID3	R	0	1	1	0	1	1	1	0	0	DCh	5.2.29
		1	-	-	-	-	-	-	-	-		
		1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		
WRDISBV	W	0	0	1	0	1	0	0	0	1	51h	5.2.30
		1	MAN_B RIGHT7	MAN_B RIGHT6	MAN_B RIGHT5	MAN_B RIGHT4	MAN_B RIGHT3	MAN_B RIGHT2	MAN_B RIGHT1	MAN_B RIGHT0		
RDDISBV	R	0	0	1	0	1	0	0	1	0	52h	5.2.31
		1	-	-	-	-	-	-	-	-		
		1	DISP_B RIGHT7	DISP_B RIGHT6	DISP_B RIGHT5	DISP_B RIGHT4	DISP_B RIGHT3	DISP_B RIGHT2	DISP_B RIGHT1	DISP_B RIGHT0		
WRCTRLD	W	0	0	1	0	1	0	0	1	1	53h	5.2.32
		1	-	-	BCTRL	-	DD	BL	-	-		
RDCTRLD	R	0	0	1	0	1	0	1	0	0	54h	5.2.33
		1	-	-	-	-	-	-	-	-		
		1	-	-	BCTRL	-	DD	BL	-	-		
WRCABC	W	0	0	1	0	1	0	1	0	1	55h	5.2.34
		1	-	-	-	-	-	-	MIE_M ODE1	MIE_M ODE0		
RDCABC	R	0	0	1	0	1	0	1	1	0	56h	5.2.35
		1	-	-	-	-	-	-	-	-		
		1	-	-	-	-	-	-	MIE_M ODE1	MIE_M ODE0		
WRCABCMB	W	0	0	1	0	1	1	1	1	0	5Eh	5.2.36
		1	MIN_B RIGHT7	MIN_B RIGHT6	MIN_B RIGHT5	MIN_B RIGHT4	MIN_B RIGHT3	MIN_B RIGHT2	MIN_B RIGHT1	MIN_B RIGHT0		

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Reference
RDCABCMB	R	0	0	1	0	1	1	1	1	1	5Fh	5.2.37
		1	-	-	-	-	-	-	-	-		
		1	MIN_B RIGHT7	MIN_B RIGHT6	MIN_B RIGHT5	MIN_B RIGHT4	MIN_B RIGHT3	MIN_B RIGHT2	MIN_B RIGHT1	MIN_B RIGHT0		
MIECTL1	W	0	1	1	0	0	1	0	1	0	CAh	5.2.38
		1	RRC7	RRC6	RRC5	RRC4	RRC3	RRC2	RRC1	RRC0		
		1	IERC7	IERC6	IERC5	IERC4	IERC3	IERC2	IERC1	IERC0		
		1	-	-	ONOFF _DIMM _EN	SERC4	SERC3	SERC2	SERC1	SERC0		
BCMODE	W	0	1	1	0	0	1	0	1	1	CBh	5.2.39
		1	-	-	-	-	-	-	BC_MO DE1	BC_MO DE0		

Note. Undefined commands are treated as NOP(00h) command.

B0 to D9 and DE to FF are for the factory use of the display supplier. User can decide if these commands are available or they are treated as NOP(00h) commands before shipping to user. Default value is NOP(00h).

Commands 10h, 12h, 13h, 28h, 29h, 30h, 36h (Bit 4 only), 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Signal Mode (0Eh) and Read Self Diagnostic Result (0Fh) commands are updated immediately both in Sleep In mode and Sleep Out mode.

5.1.2. Level 2 : Function Command

Table 109. Instruction code – (B0)

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
DSTB	W	0	1	0	1	1	0	0	0	0	B0h	5.3.1
		1	-	-	-	-	-	-	-	DSTB		

Table 110. Instruction code – (C6)

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
SE	W	0	1	1	0	0	0	1	1	0	C6h	5.3.1
		1	SE_MODE	0	0	0	0	0	GAIN [1]	GAIN [0]		

Table 111. Instruction code – (CC ~ CD)

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
MIECTL2	R/W	0	1	1	0	0	1	1	0	0	CCh	5.3.2
		1	-	-	CAT1	CAT0	CST1	CST0	WINVADDR08	WINVADDR07		
			WINVADDR06	WINVADDR05	WINVADDR04	WINVADDR03	WINVADDR02	WINVADDR01	WINVADDR00	WINVADDR18		
			WINVADDR17	WINVADDR16	WINVADDR15	WINVADDR14	WINVADDR13	WINVADDR12	WINVADDR11	WINVADDR10		
			0	0	0	0	0	0	0	0		
			1	1	1	0	1	1	1	1		
MIECTL3	R/W	0	1	1	0	0	1	1	0	1	CDh	5.3.3
		1	-	BC_FRQ_SEL6	BC_FRQ_SEL5	BC_FRQ_SEL4	BC_FRQ_SEL3	BC_FRQ_SEL2	BC_FRQ_SEL1	BC_FRQ_SEL0		
			BL_MODE_INSLP	-	DT2	DT1	DT0	BL_DRV_EN	BL_DIMM_STEP1	BL_DIMM_STEP0		

Table 112. Instruction code – (D0 ~ D5)

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
MTPCTL	R/W	0	1	1	0	1	0	0	0	0	D0h	5.3.4
		1	-	-	-	-	ID_SEL	MTP_SEL	MTP_MODE	MTP_EX		
			-	-	-	-	-	MTP_ERB	MTP_LOAD	MTP_WRB		
WRVCMOC	R/W	0	1	1	0	1	0	0	0	1	D1h	5.3.5
		1	-	-	VCMOC5	VCMOC4	VCMOC3	VCMOC2	VCMOC1	VCMOC0		
WRVMLOC	R/W	0	1	1	0	1	0	0	1	0	D2h	5.3.6
		1	-	-	-	VMLOC4	VMLOC3	VMLOC2	VMLOC1	VMLOC0		
WRGVDOC	R/W	0	1	1	0	1	0	0	1	1	D3h	5.3.7
		1	-	-	-	GVDOC4	GVDOC3	GVDOC2	GVDOC1	GVDOC0		
WRID	R/W	0	1	1	0	1	0	1	0	0	D4h	5.3.8
		1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		
			ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		
			ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		
RDOFFSETC	R	0	1	1	0	1	0	1	0	1	D5h	5.3.9
		1	-	-	-	-	-	-	-	-		
			0	0	VCMOC_MTP5	VCMOC_MTP4	VCMOC_MTP3	VCMOC_MTP2	VCMOC_MTP1	VCMOC_MTP0		
			0	0	0	VMLOC_MTP4	VMLOC_MTP3	VMLOC_MTP2	VMLOC_MTP1	VMPOC_MTP0		
			0	0	0	GVDOC_MTP4	GVDOC_MTP3	GVDOC_MTP2	GVDOC_MTP1	GVDOC_MTP0		

Table 113. Instruction code – (E0 ~ F6)

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
MDDICTL	W	0	1	1	1	0	0	0	0	0	E0h	5.3.10
		1	-	-	-	-	-	-	MDDI_SLP	VWAKE_EN		
MDDILIK	W	0	1	1	1	0	0	0	0	1	E1h	5.3.11
		1	WKL8	WKL7	WKL6	WKL5	WKL4	WKL3	WKL2	WKL1		
		1	WKL0	0	WKF3	WKF2	WKF1	WKF0	0	0		
WRPWD	R/W	0	1	1	1	1	0	0	0	0	F0h	5.3.12
		1	TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0		
DISCTL	R/W	0	1	1	1	1	0	0	1	0	F2h	5.3.13
		1	-	-	-	NRTN4	NRTN3	NRTN2	NRTN1	NRTN0		
			-	-	-	IPRTN4	IPRTN3	IPRTN2	IPRTN1	IPRTN0		
			-	-	-	-	IPINV	IINV	PINV	NINV		
			NVBP7	NVBP6	NVBP5	NVBP4	NVBP3	NVBP2	NVBP1	NVBP0		
			NVFP7	NVFP6	NVFP5	NVFP4	NVFP3	NVFP2	NVFP1	NVFP0		
			IPVBP7	IPVBP6	IPVBP5	IPVBP4	IPVBP3	IPVBP2	IPVBP1	IPVBP0		
			IPVFP7	IPVFP6	IPVFP5	IPVFP4	IPVFP3	IPVFP2	IPVFP1	IPVFP0		
			-	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0		
			-	-	-	-	-	SM	GS	REV		
			-	-	-	NCRTN4	NCRTN3	NCRTN2	NCRTN1	NCRTN0		
			-	-	-	IPCRTN4	IPCRTN3	IPCRTN2	IPCRTN1	IPCRTN0		
PWRCTL	R/W	0	1	1	1	1	0	0	1	1	F3h	5.3.14
		1	APON	GON	AON	PON3	PON2	PON1	PON	VCI1_EN		
			-	-	NDC31	NDC30	NDC21	NDC20	NDC11	NDC10		
			-	-	IPDC31	IPDC30	IPDC21	IPDC20	IPDC11	IPDC10		
			-	-	-	-	VC3	VC2	VC1	VC0		
			-	IPBT2	IPBT1	IPBT0	-	NBT2	NBT1	NBT0		
			-	GVD6	GVD5	GVD4	GVD3	GVD2	GVD1	GVD0		
			-	IPGVD6	IPGVD5	IPGVD4	IPGVD3	IPGVD2	IPGVD1	IPGVD0		
			-	-	VGH_FLAG_EN	AB_VCI1	NAB2A_G	IPAB2A_G	NAB2A	IPAB2A		
VCMCTL	R/W	0	1	1	1	1	0	1	0	0	F4h	5.3.15

		1	-	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0		
			-	IPVCM6	IPVCM5	IPVCM4	IPVCM3	IPVCM2	IPVCM1	IPVCM0		
			VCOMG	VML6	VML5	VML4	VML3	VML2	VML1	VML0		
			-	IPVML6	IPVML5	IPVML4	IPVML3	IPVML2	IPVML1	IPVML0		
			-	VCIRA2	VCIRA1	VCIRA0	0	VCIR2	VCIR1	VCIR0		
SRCCTL	R/W	0	1	1	1	1	0	1	0	1	F5h	5.3.16
		1	--	-	-	GS_EN	-	-	NGF	XSG		
			-	IPSDT2	IPSDT1	IPSDT0	-	NSDT2	NSDT1	NSDT0		
			-	-	-	-	SAP3	SAP2	SAP1	SAP0		
			NBLK_VCIR1	NBLK_VCIR0	IPBLK_VCIR1	IPBLK_VCIR0	NDISP_CON1	NDISP_CON0	IPDISP_CON1	IPDISP_CON0		
			-	VCOM_BLK_OFF	-	-	NBLK_CON1	NBLK_CON0	IPBLK_CON1	IPBLK_CON0		
			-	-	-	GOCM2	GOCM1	GOCM0	OCM1	OCM0		
IFCTL	R/W	0	1	1	1	1	0	1	1	0	F6h	5.3.17
		1	MY_EOR	MX_EOR	MV_EOR	ML_EOR	BGR_EOR	-	-	-		
			IPM2	IPM1	IPM0	MDT1	MDT0	0	VSM	DM		
			VPL	HPL	DPL	EPL	ENDIAN	-	-	RIM		
			-	-	-	-	RGB_DIV3	RGB_DIV2	RGB_DIV1	RGB_DIV0		

Table 114. Instruction Code – (F7 ~ FD)

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
RPGAMCTL	R/W	0	1	1	1	1	0	1	1	1	F7h	5.3.18
		1	RGLP1	RGLP0	RRFP5	RRFP4	RRFP3	RRFP2	RRFP1	RRFP0		
			-	-	ROSP5	ROSP4	ROSP3	ROSP2	ROSP1	ROSP0		
			-	-	RPKP 05	RPKP 04	RPKP 03	RPKP 02	RPKP 01	RPKP 00		
			-	-	RPKP 15	RPKP 14	RPKP 13	RPKP 12	RPKP 11	RPKP 10		
			-	-	RPKP 25	RPKP 24	RPKP 23	RPKP 22	RPKP 21	RPKP 20		
			-	-	RPKP 35	RPKP 34	RPKP 33	RPKP 32	RPKP 31	RPKP 30		
			-	-	RPKP 45	RPKP 44	RPKP 43	RPKP 42	RPKP 41	RPKP 40		
			-	-	RPKP 55	RPKP 54	PPKP 53	RPKP 52	RPKP 51	RPKP 50		
			-	-	RPKP 65	RPKP 64	RPKP 63	RPKP 62	RPKP 61	RPKP 60		
			-	-	RPKP 75	RPKP 74	RPKP 73	RPKP 72	RPKP 71	RPKP 70		
			-	-	RPKP 85	RPKP 84	RPKP 83	RPKP 82	RPKP 81	RPKP 80		
			-		RPKP 95	RPKP 94	RPKP 93	RPKP 92	RPKP 91	RPKP 90		
			-		RPKP 105	RPKP 104	RPKP 103	RPKP 102	RPKP 101	RPKP 100		
			RGSRP 03	RGSRP 02	RGSR P01	RGSR P00	RGSR P13	RGSR P12	RGSR P11	RGSR P10		
			RGSRP 23	RGSRP 22	RGSR P21	RGSR P20	RGSR P33	RGSR P32	RGSR P31	RGSR P30		
RNGAMCTL	R/W	0	1	1	1	1	1	0	0	0	F8h	5.3.19
		1	RGLN1	RGLN0	RRFN5	RRFN4	RRFN3	RRFN2	RRFN1	RRFN0		
			-	-	ROSN5	ROSN4	ROSN3	ROSN2	ROSN1	ROSN0		
			-	-	RPKN 05	RPKN 04	RPKN 03	RPKN 02	RPKN 01	RPKN 00		
			-	-	RPKN 15	RPKN 14	RPKN 13	RPKN 12	RPKN 11	RPKN 10		

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
			-	-	RPKN25	RPKN24	RPKN23	RPKN22	RPKN21	RPKN20		
			-	-	RPKN35	RPKN34	RPKN33	RPKN32	RPKN31	RPKN30		
			-	-	RPKN45	RPKN44	RPKN43	RPKN42	RPKN41	RPKN40		
			-	-	RPKN55	RPKN54	RPKN53	RPKN52	RPKN51	RPKN50		
			-	-	RPKN65	RPKN64	RPKN63	RPKN62	RPKN61	RPKN60		
			-	-	RPKN75	RPKN74	RPKN73	RPKN72	RPKN71	RPKN70		
			-	-	RPKN85	RPKN84	RPKN83	RPKN82	RPKN81	RPKN80		
			-	-	RPKN95	RPKN94	RPKN93	RPKN92	RPKN91	RPKN90		
			-	-	RPKN105	RPKN104	RPKN103	RPKN102	RPKN101	RPKN100		
			RGSRN03	RGSRN02	RGSRN01	RGSRN00	RGSRN13	RGSRN12	RGSRN11	RGSRN11		
			RGSRN23	RGSRN22	RGSRN21	RGSRN20	RGSRN33	RGSRN32	RGSRN31	RGSRN31		
GGAMCTL	R/W	0	1	1	1	1	1	0	0	1	F9h	5.3.20
		1	GGLP1	GGLP0	GRFP5	GRFP4	GRFP3	GRFP2	GRFP1	GRFP0		
			-	-	GOSP5	GOSP4	GOSP3	GOSP2	GOSP1	GOSP0		
			-	-	GPKP05	GPKP04	GPKP03	GPKP02	GPKP01	GPKP00		
			-	-	GPKP15	GPKP14	GPKP13	GPKP12	GPKP11	GPKP10		
			-	-	GPKP25	GPKP24	GPKP23	GPKP22	GPKP21	GPKP20		
			-	-	GPKP35	GPKP34	GPKP33	GPKP32	GPKP31	GPKP30		
			-	-	GPKP45	GPKP44	GPKP43	GPKP42	GPKP41	GPKP40		
			-	-	GPKP55	GPKP54	GPKP53	GPKP52	GPKP51	GPKP50		

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
			-	-	GPKP65	GPKP64	GPKP63	GPKP62	GPKP61	GPKP60		
			-	-	GPKP75	GPKP74	GPKP73	GPKP72	GPKP71	GPKP70		
			-	-	GPKP85	GPKP84	GPKP83	GPKP82	GPKP81	GPKP80		
			-		GPKP95	GPKP94	GPKP93	GPKP92	GPKP91	GPKP90		
			-		GPKP105	GPKP104	GPKP103	GPKP102	GPKP101	GPKP100		
			GGSRP03	GGSRP02	GGSRP01	GGSRP00	GGSRP13	GGSRP12	GGSRP11	GGSRP10		
			GGSRP23	GGSRP22	GGSRP21	GGSRP20	GGSRP33	GGSRP32	GGSRP31	GGSRP30		

Table 115. Instruction code – (F6 ~ FD) (continued)

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
GNGAMCTL	R/W	0	1	1	1	1	1	0	1	0	FAh	5.3.21
		1	GGLN1	GGLN0	GRFN5	GRFN4	GRFN3	GRFN2	GRFN1	GRFN0		
			-	-	GOSN5	GOSN4	GOSN3	GOSN2	GOSN1	GOSN0		
			-	-	GPKN 05	GPKN 04	GPKN 03	GPKN 02	GPKN 01	GPKN 00		
			-	-	GPKN 15	GPKN 14	GPKN 13	GPKN 12	GPKN 11	GPKN 10		
			-	-	GPKN 25	GPKN 24	GPKN 23	GPKN 22	GPKN 21	GPKN 20		
			-	-	GPKN 35	GPKN 34	GPKN 33	GPKN 32	GPKN 31	GPKN 30		
			-	-	GPKN 45	GPKN 44	GPKN 43	GPKN 42	GPKN 41	GPKN 40		
			-	-	GPKN 55	GPKN 54	GPKN 53	GPKN 52	GPKN 51	GPKN 50		
			-	-	GPKN 65	GPKN 64	GPKN 63	GPKN 62	GPKN 61	GPKN 60		
			-	-	GPKN 75	GPKN 74	GPKN 73	GPKN 72	GPKN 71	GPKN 70		
			-	-	GPKN 85	GPKN 84	GPKN 83	GPKN 82	GPKN 81	GPKN 80		
			-	-	GPKN 95	GPKN 94	GPKN 93	GPKN 92	GPKN 91	GPKN 90		
			-	-	GPKN 105	GPKN 104	GPKN 103	GPKN 102	GPKN 101	GPKN 100		
			GGSRN 03	GGSRN 02	GGSRN 01	GGSRN 00	GGSRN 13	GGSRN 12	GGSRN 11	GGSRN 11		
			GGSRN 23	GGSRN 22	GGSRN 21	GGSRN 20	GGSRN 33	GGSRN 32	GGSRN 31	GGSRN 31		
BGAMCTL	R/W	0	1	1	1	1	1	0	1	1	FBh	5.3.22
		1	BGLP1	BGLP0	BRFP5	BRFP4	BRFP3	BRFP2	BRFP1	BRFP0		
			-	-	BOSP5	BOSP4	BOSP3	BOSP2	BOSP1	BOSP0		
			-	-	BPKP 05	BPKP 04	BPKP 03	BPKP 02	BPKP 01	BPKP 00		

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
			-	-	BPKP 15	BPKP 14	BPKP 13	BPKP 12	BPKP 11	BPKP 10		
			-	-	BPKP 25	BPKP 24	BPKP 23	BPKP 22	BPKP 21	BPKP 20		
			-	-	BPKP 35	BPKP 34	BPKP 33	BPKP 32	BPKP 31	BPKP 30		
			-	-	BPKP 45	BPKP 44	BPKP 43	BPKP 42	BPKP 41	BPKP 40		
			-	-	BPKP 55	BPKP 54	BPKP 53	BPKP 52	BPKP 51	BPKP 50		
			-	-	BPKP 65	BPKP 64	BPKP 63	BPKP 62	BPKP 61	BPKP 60		
			-	-	BPKP 75	BPKP 74	BPKP 73	BPKP 72	BPKP 71	BPKP 70		
			-	-	BPKP 85	BPKP 84	BPKP 83	BPKP 82	BPKP 81	BPKP 80		
			-		BPKP 95	BPKP 94	BPKP 93	BPKP 92	BPKP 91	BPKP 90		
			-		BPKP 105	BPKP 104	BPKP 103	BPKP 102	BPKP 101	BPKP 100		
			BGSRP 03	BGSRP 02	BGSRP 01	BGSRP 00	BGRSP 13	BGRSP 12	BGRSP 11	BGRSP 10		
			BGSRP 23	BGSRP 22	BGSRP 21	BGSRP 20	BGRSP 33	BGRSP 32	BGRSP 31	BGRSP 30		
BNGAMCTL	R/W	0	1	1	1	1	1	1	0	0	FCh	5.3.23
		1	BGLN1	BGLN0	BRFN5	BRFN4	BRFN3	BRFN2	BRFN1	BRFN0		
			-	-	BOSN5	BOSN4	BOSN3	BOSN2	BOSN1	BOSN0		
			-	-	BPKN 05	BPKN 04	BPKN 03	BPKN 02	BPKN 01	BPKN 00		
			-	-	BPKN 15	BPKN 14	BPKN 13	BPKN 12	BPKN 11	BPKN 10		
			-	-	BPKN 25	BPKN 24	BPKN 23	BPKN 22	BPKN 21	BPKN 20		
			-	-	BPKN 35	BPKN 34	BPKN 33	BPKN 32	BPKN 31	BPKN 30		
			-	-	BPKN 45	BPKN 44	BPKN 43	BPKN 42	BPKN 41	BPKN 40		

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
			-	-	BPKN 55	BPKN 54	BPKN 53	BPKN 52	BPKN 51	BPKN 50		
			-	-	BPK N65	BPKN 64	BPKN 63	BPKN 62	BPKN 61	BPKN 60		
			-	-	BPKN 75	BPKN 74	BPKN 73	BPKN 72	BPKN 71	BPKN 70		
			-	-	BPKN 85	BPKN 84	BPKN 83	BPKN 82	BPKN 81	BPKN 80		
			-	-	BPKN 95	BPKN 94	BPKN 93	BPKN 92	BPKN 91	BPKN 90		
			-	-	BPKN 105	BPKN 104	BPKN 103	BPKN 102	BPKN 101	BPKN 100		
			BGRSN 03	BGRSN 02	BGRSN 01	BGRSN 00	BGRSN 13	BGRSN 12	BGRSN 11	BGRSN 11		
			BGRSN 23	BGRSN 22	BGRSN 21	BGRSN 20	BGRSN 33	BGRSN 32	BGRSN 31	BGSRN 31		
GATECTL	R/W	0	1	1	1	1	1	1	0	1	FDh	5.3.24
		1	-	IPNO2	IPNO1	IPNO0	-	NNO2	NNO1	NNO0		
		1	-	-	-	-	-	-	SEL_NL 1	SEL_NL 0		
DCON	R/W	0	1	1	0	1	1	0	0	1	D9h	5.3.25
		1	0	0	0	0	0	D_CON 2	D_CON 1	D_CON 0		
TESTKEY	W	0	1	1	1	1	0	0	0	0	F1h	5.3.26
		1	TESTK 7	TESTK6	TESTK5	TESTK4	TESTK 3	TESTK 2	TESTK1	TESTK0		
EDSTEST	R/W	0	1	1	1	1	1	1	1	1	FFh	5.3.27
		1	-	-	0	0	0	0	0	0		
			-	-	0	0	0	0	0	0		
			-	-	0	0	0	0	0	0		
			-	SD_EN	SD1	SD2	SD3	0	0	0		

Note1. In Level1 and Level 2 register read action, if Interface mode is 80 MCU, 1-byte Dummy Read will be needed,

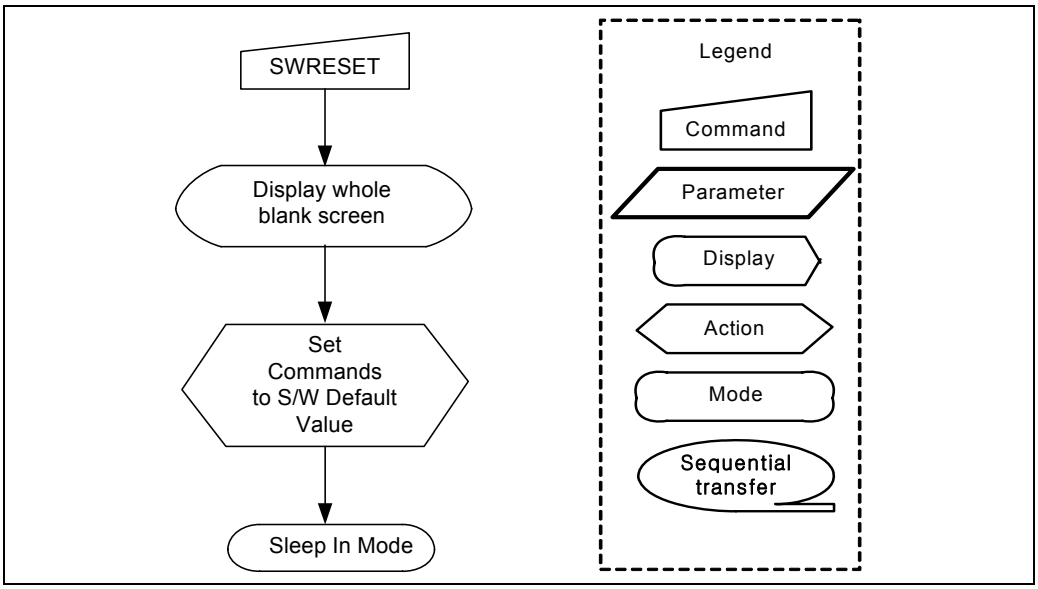
Note2. Level 2 registers are not readable in SPI mode.

5.2. DESCRIPTION OF LEVEL1 COMMAND

5.2.1. NOP (00h)

<table>
<tr><th>Inst/Para</th><th>R/W</th><th>DCX</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>NOP</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Parameter</td><td colspan="11">No Parameter</td></tr>
<tr><td>Description</td><td colspan="11">This is a null command. It does not have any effect on the display module.
However it can be used to terminate the write/read operation of RAM data as described in RAMWR (Memory Write), RAMRD (Memory Read) and parameter write commands.</td></tr>
<tr><td>Restriction</td><td colspan="11">-</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
</table>

5.2.2. SWRESET : Software Reset (01h)

<table>
<tr><th>Inst/Para</th><th>R/W</th><th>DCX</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>SWRESET</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>01h</td></tr>
<tr><td>Parameter</td><td colspan="11">No Parameter</td></tr>
<tr><td>Description</td><td colspan="11">The Software Reset command resets the commands and parameters to their S/W Reset default values, and all the source & gate outputs are set to VSS (display off). (See default tables in each command description)
Note: The Frame Memory contents are not affected by this command</td></tr>
<tr><td>Restriction</td><td colspan="11">It is necessary to wait for 5msec before sending new commands following the software reset.
The display module loads all of display supplier's factory default values to the registers during 5msec.
If Software Reset is applied during Sleep Out mode, it is necessary to wait 120msec before sending Sleep Out command.
Software Reset command cannot be sent during Sleep Out sequence.</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="11"> 
</td></tr>
</table>

5.2.3. RDDIDIF : Read Display ID (04h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDIDIF	R	0	0	0	0	0	0	1	0	0	04h
Dummy Read		1	X	X	X	X	X	X	X	X	X
2nd parameter		1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	xx
3rd parameter		1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	xx
4th parameter		1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	xx

Description

This read command returns 24-bit display identification information.

The 1st parameter is dummy data.

The 2nd parameter identifies the LCD module's manufacturers. It is specified by a user.

The 3rd parameter has 2 purposes. Bit7(MSB) defines the type of a panel. 0=Driver (STN B/W), 1=Module(Color). Bit 6..0 are used to track the LCD module/driver version. It is defined by a panel supplier and updated each time; a version of the display is updated.

The 4th parameter identifies the LCD module/driver. It is specified by a user.

Note.Commands RDID1/2/3(DAh, DBh, DCh) reads data corresponding to the parameters 2, 3, 4 of the command 04h, respectively.

"X" denotes "Don't care"

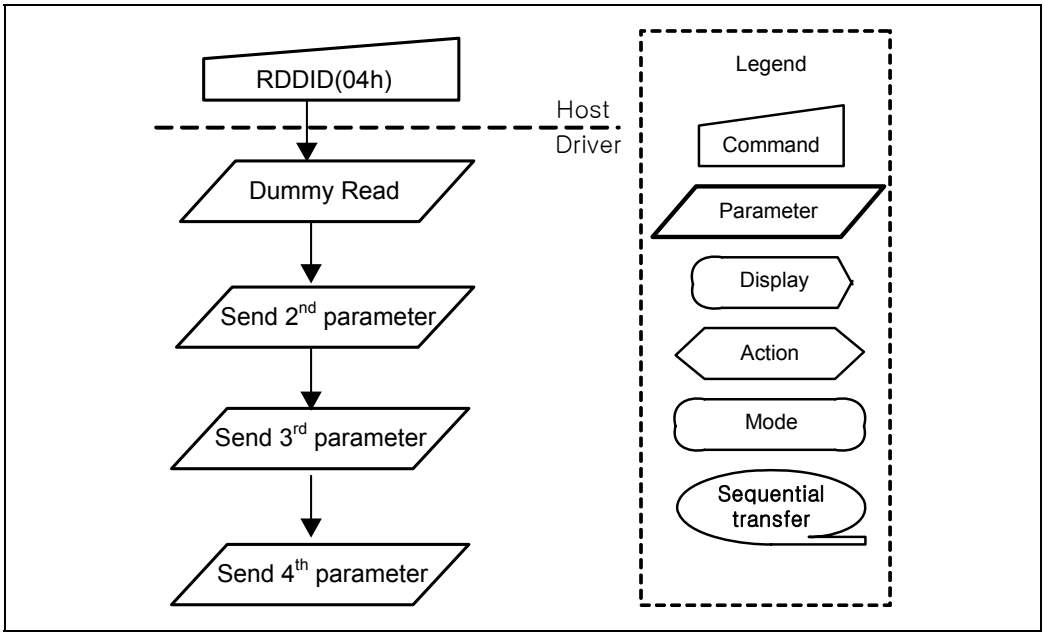
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	(MTP value)	(MTP value)	(MTP value)
S/W Reset	(MTP value)	(MTP value)	(MTP value)
H/W Reset	(MTP value)	(MTP value)	(MTP value)

Flow Chart	

RDDID(04h)
Host
Driver
Dummy Read
Send 2nd parameter
Send 3rd parameter
Send 4th parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

5.2.4. RDDST : Read Display Status (09h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDST	R	0	0	0	0	0	1	0	0	1	09h
Dummy Read		1	X	X	X	X	X	X	X	X	X
2nd parameter		1	D31	D30	D29	D28	D27	D26	D25	0	xx
3rd parameter		1	0	D22	D21	D20	D19	D18	D17	D16	xx
4th parameter		1	0	0	0	0	0	D10	D9	D8	xx
5th parameter		1	D7	D6	D5	0	0	0	0	0	xx

Description

This command indicates the current status of the display as described in the table below

Bit	Description	Value
D31	Booster Voltage Status	"1"=Booster on "0"=off
D30	Page Address Order (MY)	"1"=Decrement "0"=Increment
D29	Column Address Order (MX)	"1"=Decrement "0"=Increment
D28	Page/Column Exchange (MV)	"1"= Page/column exchange (MV=1) "0"= Normal (MV=0)
D27	Vertical Refresh Order (ML)	"1"=Decrement "0"=Increment
D26	RGB/BGR Order (RGB)	"1"=BGR "0"=RGB
D25	Display Data Latch Order(MH)	Refer to MADCTL
D24	Not Used	"0"
D23	Not Used	"0"
D22	Interface Color Pixel Format Definition (IFPF)	"101" =16-bits/pixel "110" =18-bits/pixel "111" = 24-bits/pixel Others = not defined
D21		
D20		
D19	Idle Mode On/Off	"1" = On, "0" = Off
D18	Partial Mode On/Off	"1" = On, "0" = Off
D17	Sleep In/Out	"1" = Out, "0" = In
D16	Display Normal Mode On/Off	"1" = Normal Display "0" = Partial Display
D15	Not Used	"0"
D14	Not Used	"0"
D13	Not Used	"0"
D12	Not Used	"0"

	D11	Not Used	“0”
	D10	Display On/Off	“1” = On “0” = Off
	D9	Tearing effect line on/off	“1” = On “0” = Off
	D8~D6	Gamma Curve Selection	Fixed “000”
	D5	Tearing effect line mode	“0” = mode1, V_Blanking only “1” = mode2, Both H & V-Blanking.
	D4	Not Used	“0”
	D3	Not Used	“0”
	D2	Not Used	“0”
	D1	Not Used	“0”
	D0	Not Used	“0”
	Note. “X“ denotes “Don’t care”		

Restriction

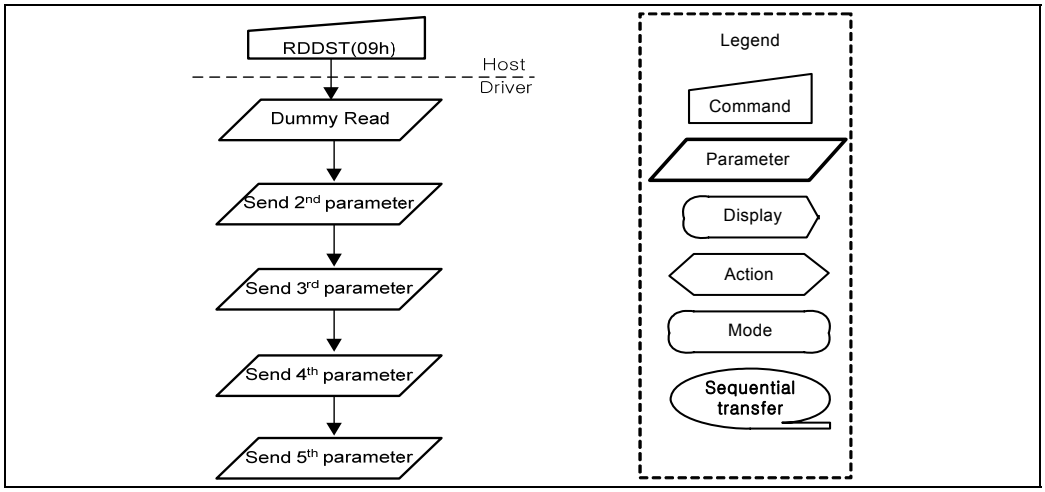
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D31 to D0)
Power On Sequence	0000_0000_0111_0001_0000 0000_0000_0000
S/W Reset	0xxx_xx00_0 xxx _0001_0000 0000_0000_0000
H/W Reset	0000_0000_0111_0001_0000 0000_0000_0000

Flow Chart



5.2.5. RDDPM : Read Display Power Mode (0Ah)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDPM	R	0	0	0	0	0	1	0	1	0	0Ah
Dummy Read		1	X	X	X	X	X	X	X	X	X
2nd parameter		1	D7	D6	D5	D4	D3	D2	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Booster Voltage Status	"1"=Booster on "0"=off
D6	Idle Mode On/Off	"1" = Idle Mode On "0"= idle Mode Off
D5	Partial Mode On/Off	"1" = Partial Mode On "0" = Partial Mode Off
D4	Sleep In/Out	"1" = Sleep Out "0" = Sleep In
D3	Display Normal Mode On/Off	"1" = Normal Display "0" = Partial Display
D2	Display On/Off	"1" = Display On "0" = Display Off
D1	Not Used	"0"
D0	Not Used	"0"

Note: "X" denotes "Don't care"

Restriction

If VGH level is lower than 12V according to VCI1 & BT settings, D7 register cannot be "1" even at sleep out mode.

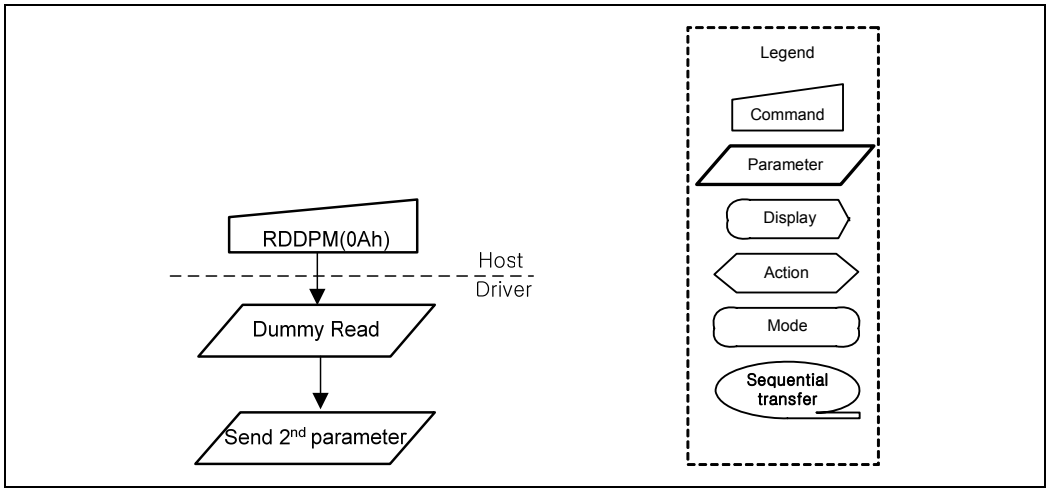
There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.5.2.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

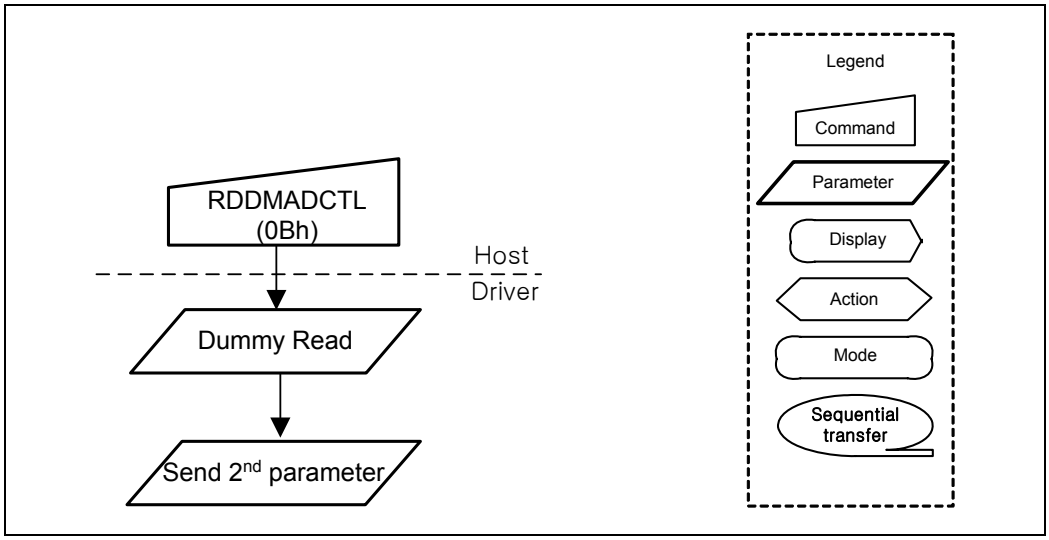
Status	Default Value (D7 to D0)
Power On Sequence	0000_1000 (08h)
S/W Reset	0000_1000 (08h)
H/W Reset	0000_1000 (08h)

Flow Chart	

RDDPM(0Ah)
Host
Driver
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

5.2.6. RDDMADCTL : Read Display MADCTL (0Bh)

<table>
<tr><th>Inst/Para</th><th>R/W</th><th>DCX</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>RDDMADCTL</td><td rowspan="3">R</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0Bh</td></tr>
<tr><td>Dummy Read</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>0</td><td>0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="11">This command indicates the current status of the display MADCTL(memory address control) as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>Page Address Order</td><td>“1”=Decrement
“0”=Increment</td></tr>
<tr><td>D6</td><td>Column Address Order</td><td>“1”=Decrement
“0”=Increment</td></tr>
<tr><td>D5</td><td>Page/Column Order (MV)</td><td>“1”= Page/column exchange (MV=1)
“0”= Normal (MV=0)</td></tr>
<tr><td>D4</td><td>Vertical fresh Order (ML)</td><td>“1”=Decrement
“0”=Increment</td></tr>
<tr><td>D3</td><td>RGB/BGR Order(RGB)</td><td>“1”=BGR
“0”=RGB</td></tr>
<tr><td>D2</td><td>Display Data Latch Order(MH)</td><td>Refer to MADCTL</td></tr>
<tr><td>D1</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D0</td><td>Not Used</td><td>“0”</td></tr>
</table>
Note: “X“ denotes “Don’t care”</td></tr>
<tr><td>Restriction</td><td colspan="11">D2 is Read/Write Register Only, It is not active Function.
There is not possible to avoid the tearing effect in normal display if D5 = 1
There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.5.2.</td></tr>
<tr><td>Register Availability</td><td colspan="11">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="11">
<table>
<tr><th>Status</th><th>Default Value (D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>0000_0000 (00h)</td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td>0000_0000 (00h)</td></tr>
</table></td></tr>
</table>

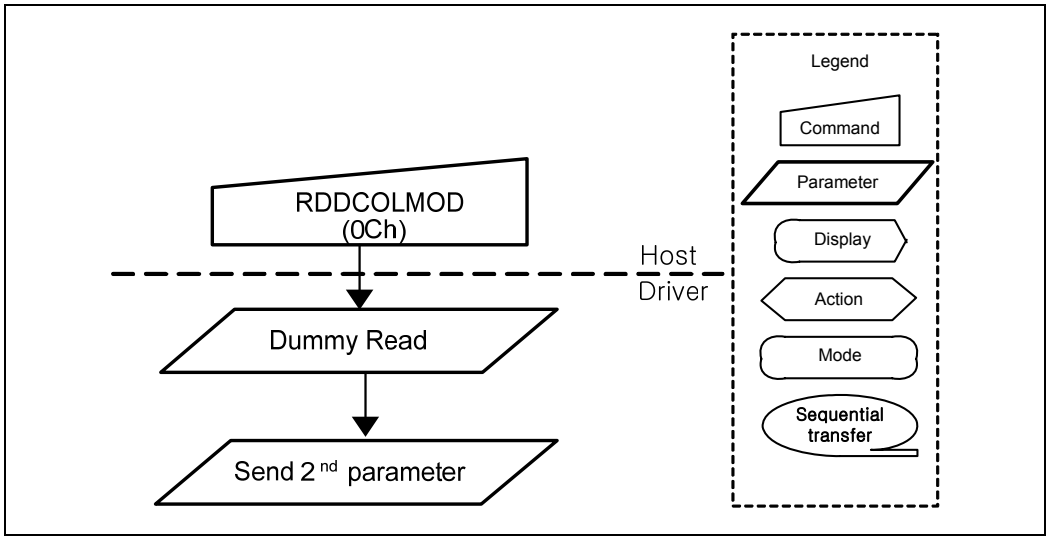
Flow Chart	

RDDMADCTL
(0Bh)
Host
Driver
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

5.2.7. RDDCOLMOD : Read Display Pixel Format (0Ch)

<table>
<tr><th>Inst/Para</th><th>R/W</th><th>DCX</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>RDDCOLMOD</td><td rowspan="3">R</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0Ch</td></tr>
<tr><td>Dummy Read</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>0</td><td>D6</td><td>D5</td><td>D4</td><td>0</td><td>D2</td><td>D1</td><td>D0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>-</td><td>“0” (Not Used)</td></tr>
<tr><td>D6</td><td rowspan="3">Control RGB Interface Color Format (VFPF)
-</td><td rowspan="3">“101”=16-bits/pixel
“110”=18-bits/pixel
"111"= 24-bits/pixel
Others = not defined</td></tr>
<tr><td>D5</td></tr>
<tr><td>D4</td></tr>
<tr><td>D3</td><td>-</td><td>“0” (Not Used)</td></tr>
<tr><td>D2</td><td rowspan="3">Control MPU Interface Color Format (IFPF)</td><td rowspan="3">“101”=16-bits/pixel
“110”=18-bits/pixel
"111"= 24-bits/pixel
Others = not defined</td></tr>
<tr><td>D1</td></tr>
<tr><td>D0</td></tr>
</table>
Bit D7: Set to’0’.
Bit D6~4 : Control RGB Interface Color Pixel Format Definition.
Bit D3 : Set to ‘0’.
Bit D2~0 : Control MPU Interface Color Pixel Format Definition..

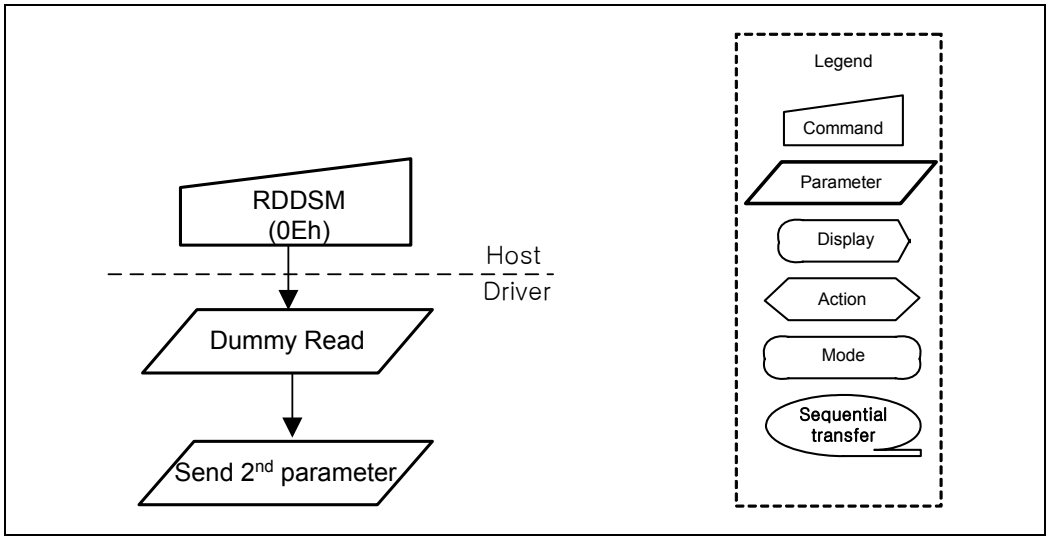
Note. “X“ denotes “Don’t care”</td></tr>
<tr><td>Restriction</td><td colspan="10">There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.5.2.</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value (D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>0111_0111 (77h)</td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td>0111_0111 (77h)</td></tr>
</table></td></tr>
</table>

Flow Chart	

RDDCOLMOD
(0Ch)
Host
Driver
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

5.2.8. RDDSM : Read Display Signal Mode (0Eh)

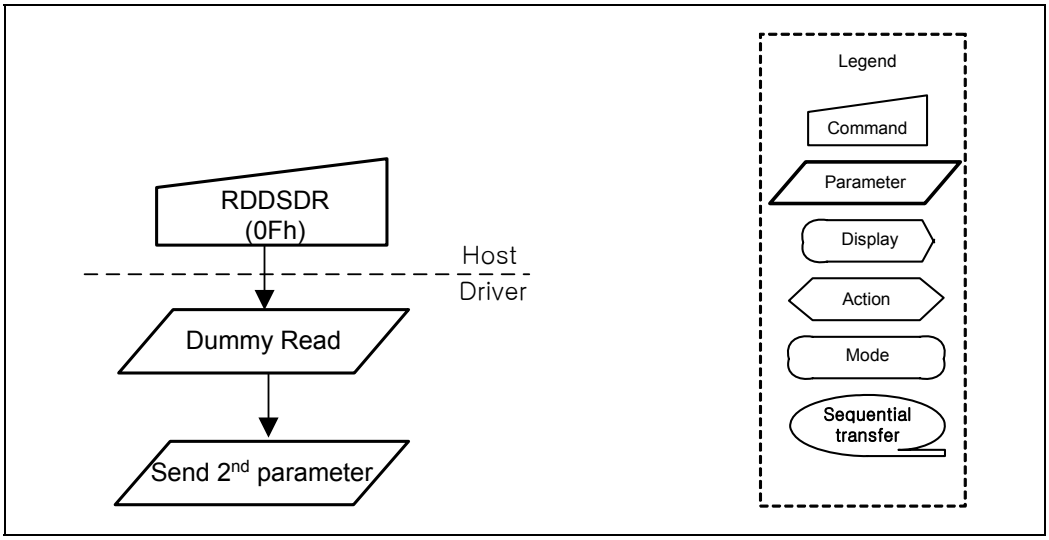
<table>
<tr><th>Inst/Para</th><th>R/W</th><th>DCX</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>RDDSM</td><td rowspan="3">R</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0Eh</td></tr>
<tr><td>Dummy Read</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>D7</td><td>D6</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display signal mode as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>Tearing Effect Line On/Off</td><td>“1” = On, “0” = Off</td></tr>
<tr><td>D6</td><td>Tearing effect line mode</td><td>“0” = Mode1
“1” = Mode2</td></tr>
<tr><td>D5</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D4</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D3</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D2</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D1</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D0</td><td>Not Used</td><td>“0”</td></tr>
</table>
Note: “X“ denotes “Don’t care”</td></tr>
<tr><td>Restriction</td><td colspan="10">There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.5.2.</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value (D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>0000_0000 (00h)</td></tr>
<tr><td>S/W Reset</td><td>0000_0000 (00h)</td></tr>
<tr><td>H/W Reset</td><td>0000_0000 (00h)</td></tr>
</table></td></tr>
</table>

Flow Chart	

RDDSM
(0Eh)
Host
Driver
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

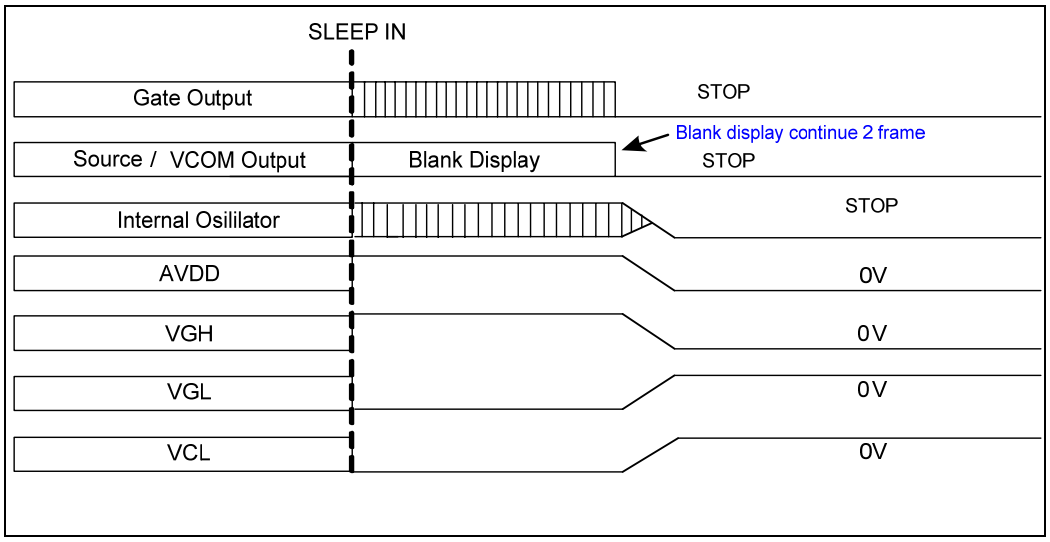
5.2.9. RDDSDR : Read Display Self-Diagnostic Result (0Fh)

<table>
<tr><th>Inst/Para</th><th>R/W</th><th>DCX</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>RDDSDR</td><td rowspan="3">R</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0Fh</td></tr>
<tr><td>Dummy Read</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>D7</td><td>D6</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="11">This command indicates the current status of the display self-diagnostics as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>Register Loading Detection</td><td rowspan="2">See section 4.7</td></tr>
<tr><td>D6</td><td>Functionality Detection</td></tr>
<tr><td>D5</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D4</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D3</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D2</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D1</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D0</td><td>Not Used</td><td>“0”</td></tr>
</table>
Note: “X“ denotes “Don’t care”</td></tr>
<tr><td>Restriction</td><td colspan="11">If VGH level is lower than 12V according to VCI1 & BT settings, D6 register cannot be inverted.
There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.5.2.</td></tr>
<tr><td>Register Availability</td><td colspan="11">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="11">
<table>
<tr><th>Status</th><th>Default Value (D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>0000_0000 (00h)</td></tr>
<tr><td>S/W Reset</td><td>0000_0000 (00h)</td></tr>
<tr><td>H/W Reset</td><td>0000_0000 (00h)</td></tr>
</table></td></tr>
</table>

Flow Chart	

RDDSDR
(0Fh)
Host
Driver
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

5.2.10. SLPIN : Sleep In (10h)

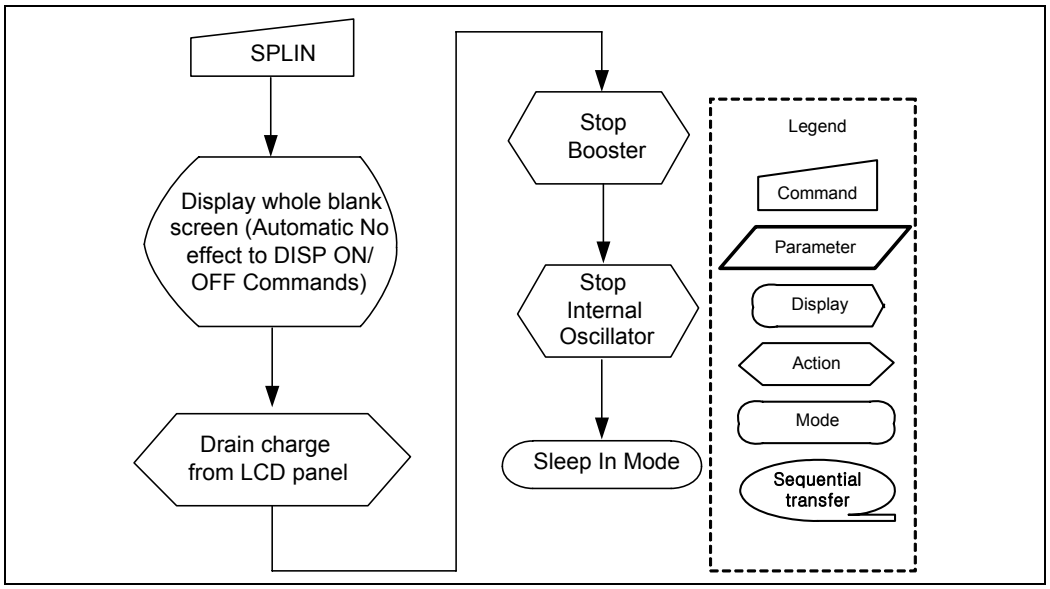
Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPIN	W	0	0	0	0	1	0	0	0	0	10h
Parameter	No Parameter										
Description	This command causes the LCD module to enter the power saving mode. During this mode, the Booster, Internal display oscillator and panel scanning are not in operation.  MCU interface and memory are still in normal operation and the memory keeps its contents.										
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only exit by the Sleep Out Command (11h). It is necessary to wait for 5msec before sending the next command, allowing time for the supply voltages and clock circuits to stabilize. It is necessary to wait for 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.										

Register Availability

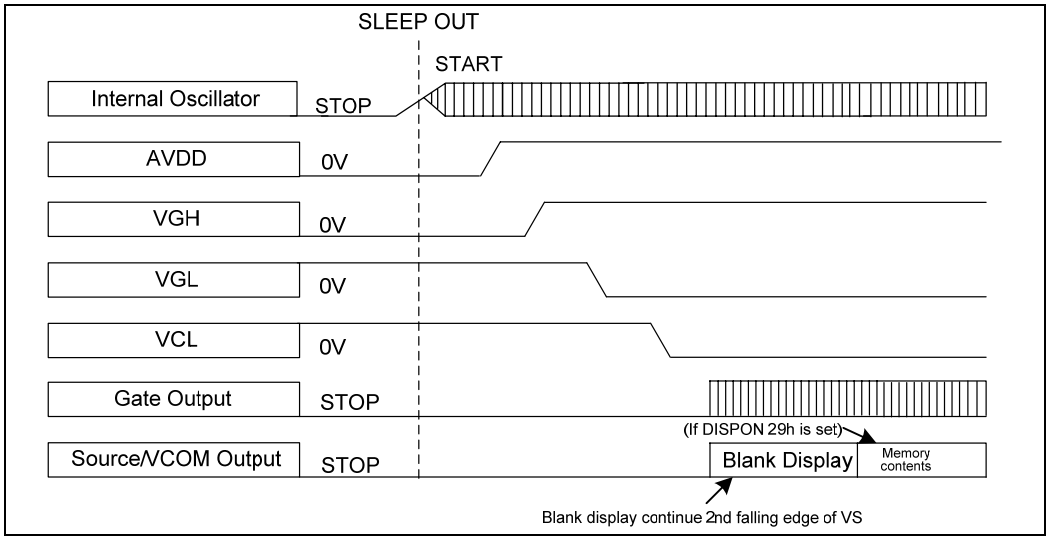
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart	It takes about 120msec before it goes into Sleep-in Mode (Booster off state) after SLPIN command. The Booster States can be checked by RDDST(09h) command Bit 31. 

5.2.11. SLPOUT : Sleep Out (11h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	W	0	0	0	0	1	0	0	0	1	11h
Parameter	No Parameter										
Description	This command turns off the sleep mode. During this mode, the Booster, the Internal display oscillator, and panel scanning are in normal operation.  										
Restriction	This command has no effect when the module is already in sleep out mode. Sleep Out Mode can only exit by the Sleep In Command (10h). It is necessary to wait for 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. S6D04D1 loads the default values of extended and test commands to the registers during this 5msec duration. There cannot be any abnormal visual effect on the display image if those default and register values are the same when this loading is done and when the S6D04D1 is already in Sleep Out –mode. S6D04D1 performs self-diagnostic during this 5msec. See also section 4.7. It is necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.										

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

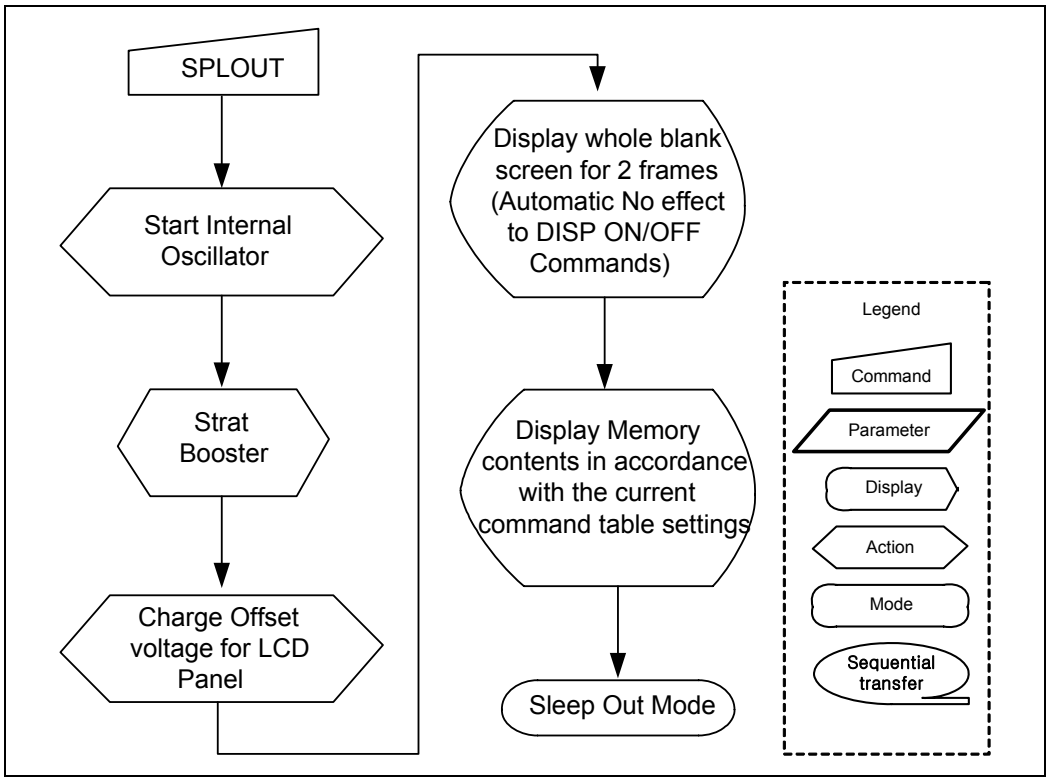
Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart

It takes 120msec to be in Sleep Out mode (booster on mode) after SLPOUT command is issued.

The booster on status can be checked by RDDST (09h) command Bit31.



5.2.12. PTLON : Partial Display Mode On (12h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLON	W	0	0	0	0	1	0	0	1	0	12h

Parameter

No Parameter

Description

This command turns on Partial mode. The partial mode window is described by the Partial Area command (30H).

To leave Partial mode, the Normal Display Mode On command (13H) should be written.

There is no abnormal visual effect during mode change between Normal mode On and Partial mode On.

Restriction

This command has no effect when Partial mode is active.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

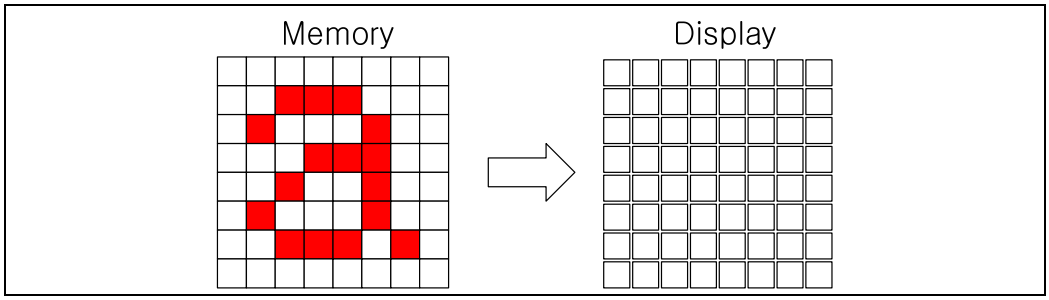
Flow Chart

See Partial Area (30h)

5.2.13. NORON : Normal Display Mode On (13h)

<table>
<tr><th>Inst/Para</th><th>R/W</th><th>DCX</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>NORON</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13h</td></tr>
<tr><td>Parameter</td><td colspan="11">No Parameter</td></tr>
<tr><td>Description</td><td colspan="11">This command returns the display to normal mode.
Turning normal display mode on means Partial mode off.
Exiting from NORON can be done by the Partial mode On command (12h).
There is no abnormal visual effect during the mode change from Normal mode On to Partial mode On.</td></tr>
<tr><td>Restriction</td><td colspan="11">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Mode On</td></tr><tr><td>S/W Reset</td><td>Normal Mode On</td></tr><tr><td>H/W Reset</td><td>Normal Mode On</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="11">See Partial Area for details of when to use this command.</td></tr>
</table>

5.2.14. DISPOFF : Display Off (28h)

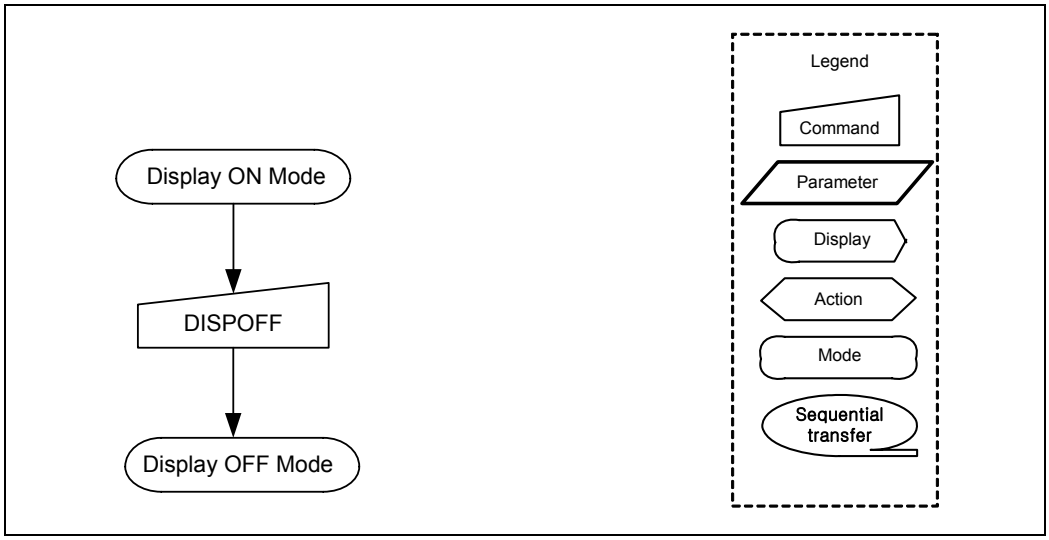
Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPOFF	W	0	0	0	1	0	1	0	0	0	28h
Parameter	No Parameter										
Description	This command turns on DISPLAY OFF mode. During this mode, the output from the Frame Memory is disabled and blank page is inserted. This command makes no change to the contents of frame memory. This command does not alter any other status. There will be no abnormal visible effect on the display. Exiting from this command can be done by Display On (29h) (Example) 										
Restriction	This command has no effect when module is already in Display Off mode.										

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart	

Display ON Mode
DISPOFF
Display OFF Mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

5.2.15. DISPON : Display On (29h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPON	W	0	0	0	1	0	1	0	0	1	29h

Parameter

No Parameter

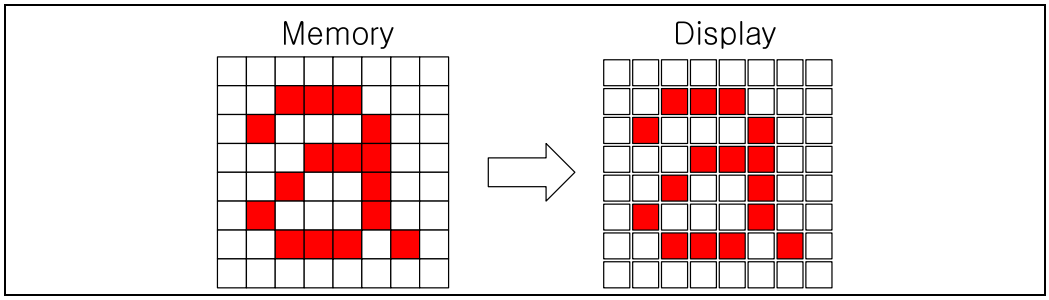
Description

This command enables DISPLAY ON mode. Output from the Frame Memory is enabled.

This command makes no change to the contents of frame memory.

This command does not alter any other status.

(Example)



Restriction

This command has no effect when the module is already in Display On mode.

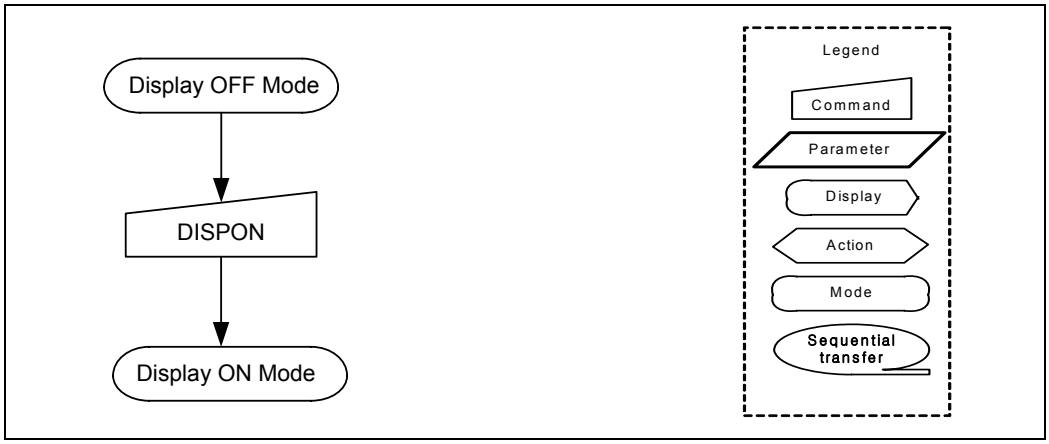
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



5.2.16. CASET : Column Address Set (2Ah)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CASET	W	0	0	0	1	0	1	0	1	0	2Ah
1st para		1	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	*Note1
2nd para		1	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	
3rd para		1	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	*Note1
4th para		1	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	

Description

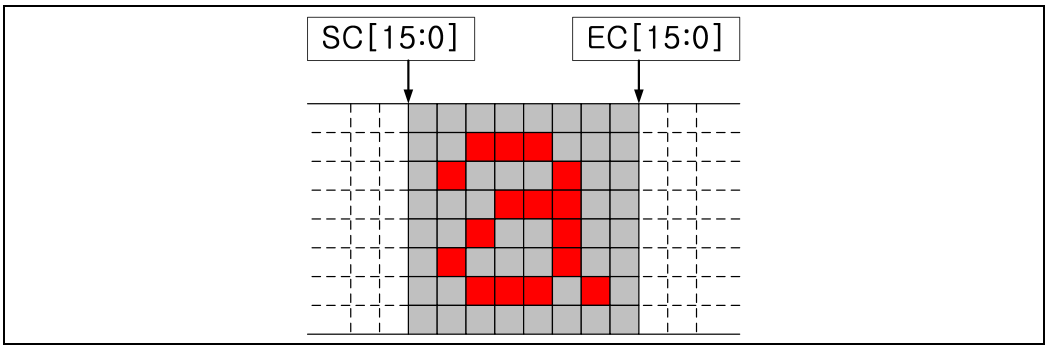
This command is used to define the area of the frame memory where MCU can access.

This command does not alter any other status.

The value of SC [15:0] and EC [15:0] are referred when RAMWR command is issued.

Each value represents one column line of the Frame Memory.

(Example)



Restriction

SC [15:0] always must be equal to or less than EC [15:0].

Note1. When SC [15:0] or EC [15:0] is greater than maximum address like below, data of out of range will be ignored.

(Parameter range: 0 ≤ SC [15:0] ≤ EC [15:0] ≤ 239 (00EFh)): MV=”0”

(Parameter range: 0 ≤ SC [15:0] ≤ EC [15:0] ≤ 431 (01AFh)): MV=”1”

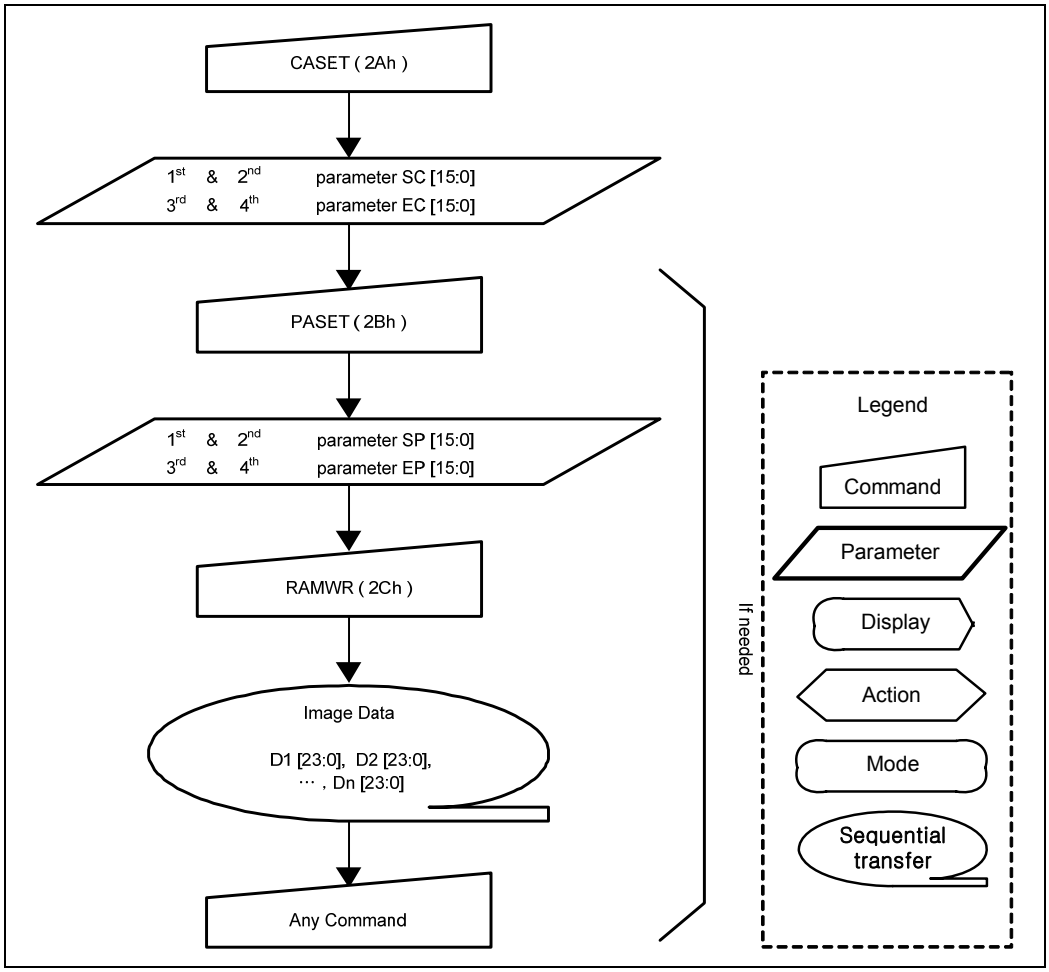
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	SC[15:0]	EC[15:0] (MV=0)	EC[15:0] (MV=1)
Power On Sequence	0000h	00EFh (239d)	
S/W Reset	0000h	00EFh(239d)	01AFh(431d)
H/W Reset	0000h	00EFh (239d)	

Flow Chart



5.2.17. PASET : Page Address Set (2Bh)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PASET	W	0	0	0	1	0	1	0	1	1	2Bh
1st para		1	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	*Note1
2nd para		1	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
3rd para		1	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	*Note1
4th para		1	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	

Description

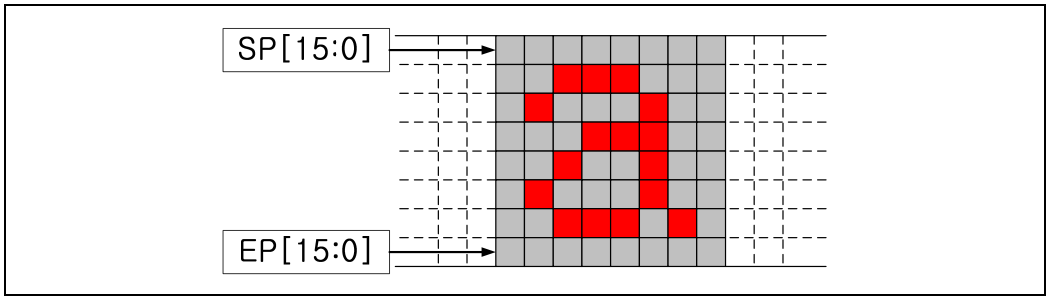
This command is used to define the area of the frame memory where MCU can access.

This command makes no change on the other driver status.

The value of SP [15:0] and EP [15:0] is referred when RAMWR command is issued.

Each value represents one column line of the Frame Memory.

(Example)



Restriction

SP [15:0] should be equal to or less than EP [15:0]

Note1. When SP [15:0] or EP [15:0] are greater than maximum Page address like below, any data out of range will be ignored.

(Parameter range: 0 ≤ SP [15:0] ≤ EP [15:0] ≤ 431 (01AFh)): MV="0"

(Parameter range: 0 ≤ SP [15:0] ≤ EP [15:0] ≤ 239 (00EFh)): MV="1"

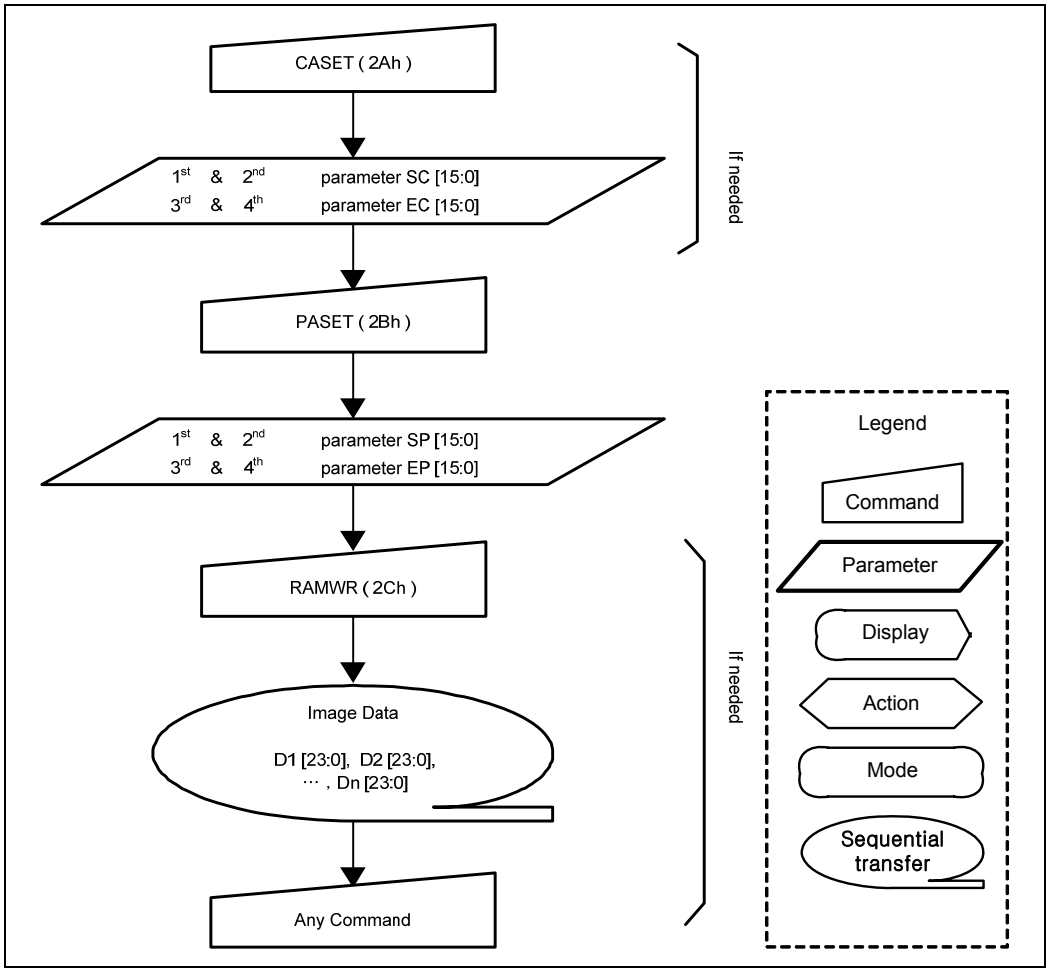
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	SP[15:0]	EP[15:0] (MV=0)	EP[15:0] (MV=1)
Power On Sequence	0000h	01AFh (431d)	
S/W Reset	0000h	01AFh (431d)	00EFh (239d)
H/W Reset	0000h	01AFh (431d)	

Flow Chart



5.2.18. RAMWR : Memory Write (2Ch)

Inst/Para	R/W	DCX	D23~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMWR	W	0	X	0	0	1	0	1	1	0	0	2Ch
1st para		1	D23~8	D17	D16	D15	D14	D13	D12	D11	D10	000000h ~ FFFFFFh
:		1	Dx~Dx	Dx	Dx	Dx	Dx	Dx	Dx	Dx	Dx	000000h ~ FFFFFFh
Nth para		1	Dn23~8	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	000000h ~ FFFFFFh

Description

This command is used to transfer data from MCU to the frame memory.

This command makes no change to the other status of the driver.

When this command is issued, the Column register and the Page register are programmed to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting. (See section 4.5.2)

Then D [23:0] is stored in the frame memory, the Column register and the Page register increments as in section 4.5.2

Sending any other command can stop the Frame Write.

Restriction

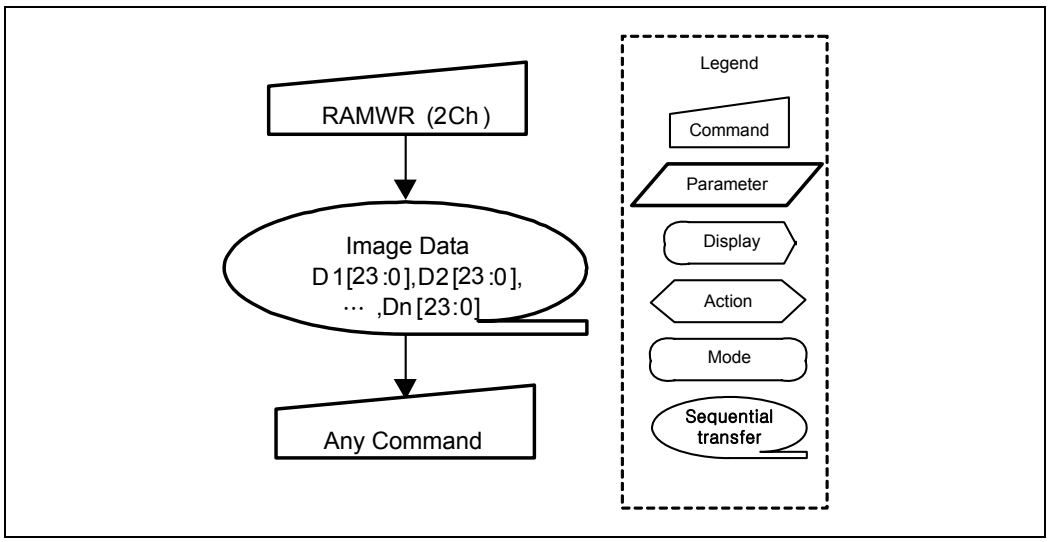
In all color modes, there is no restriction on the length of the parameters.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart	

RAMWR (2Ch)
Image Data
D1[23:0],D2[23:0],
… ,Dn[23:0]
Any Command
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

5.2.19. RAMRD : Memory Read (2Eh)

Inst/Para	R/W	DCX	D23~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMRD	R	0	X	0	0	1	0	1	1	1	0	2Eh
Dummy read		1	X	X	X	X	X	X	X	X	X	XX
2nd para		1	D123~8	D17	D16	D15	D14	D13	D12	D11	D10	000000h ~ FFFFFFh
:		1	Dx~Dx	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	000000h ~ FFFFFFh
(N+1)thpara		1	Dn23~8	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	000000h ~ FFFFFFh

Description

This command is used to transfer data from the frame memory to MCU.

This command makes no change to the other driver status.

With this command, the column register and the Page register are programmed to the Start Column/Start Page positions.The Start Column/Start Page positions are different in accordance with MADCTL setting. (See section 4.5.2)

Then D[23:0] is read back from the frame memory, and the column register and the Page register increments as in section 4.5.2

Frame Read can be cancelled by sending any other command.

See section 3.2 “Display Data Format” for color coding.

Note: “X“ denotes “Don’t care"

Restriction

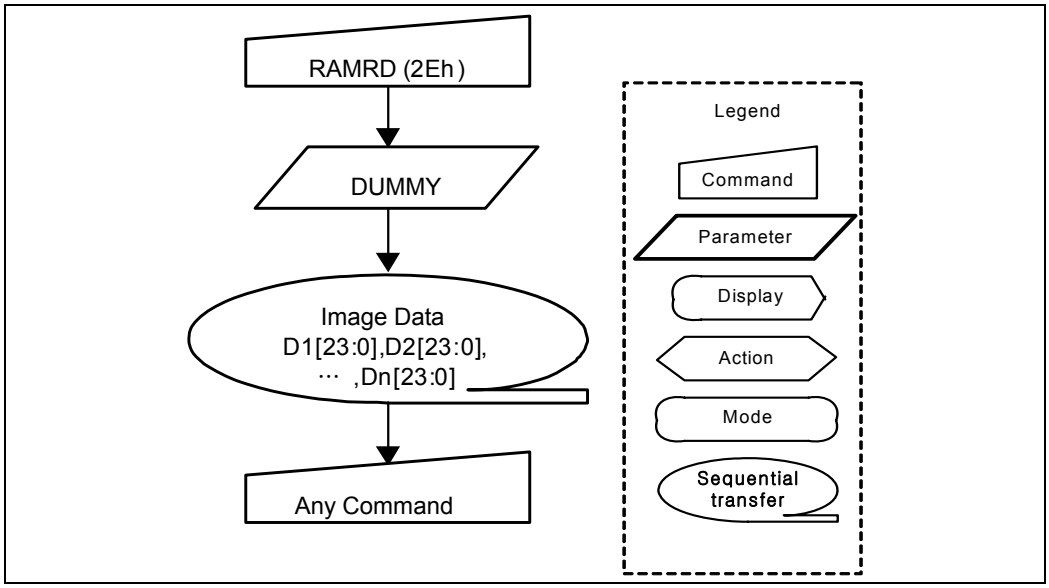
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart	

RAMRD (2Eh)
DUMMY
Image Data
D1[23:0],D2[23:0],
… ,Dn[23:0]
Any Command
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

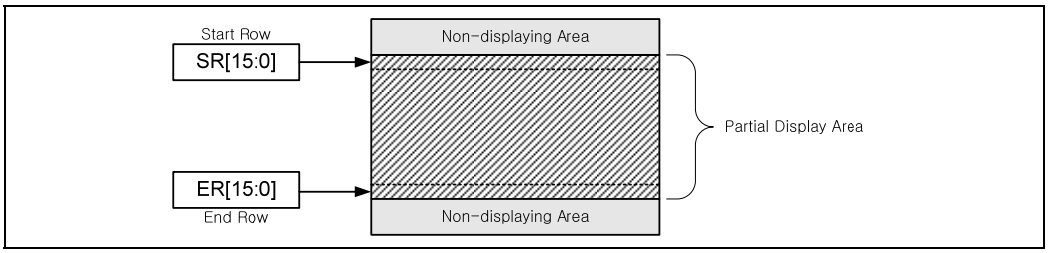
5.2.20. PTLAR : Partial Area (30h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PLTAR	W	0	0	0	0	1	1	0	0	0	30h
1st para		1	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	0000h ~ 01AFh
2nd para		1	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	
3rd para		1	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	0000h ~ 01AFh
4th para		1	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	

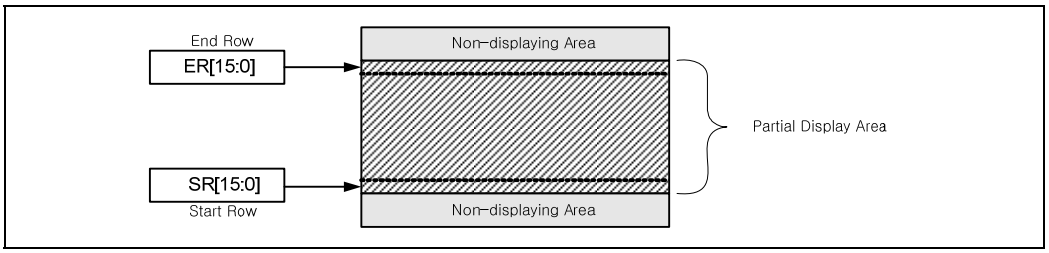
Description

This command defines the display area of the partial display mode. There are 4 parameters associated with this command. The 1'st & 2'nd parameters define the Start Row (SR) and the 3'rd and 4'th parameters define the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Row address counter. It is necessary to write 4 parameters to update the register.

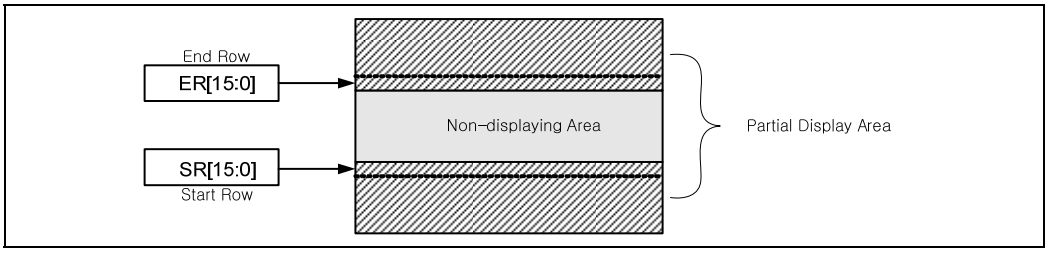
If End Row > Start Row when MADCTL D4=0



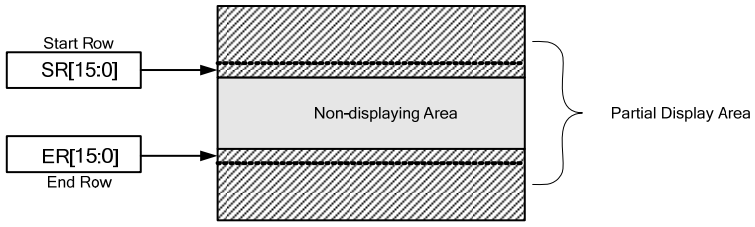
If End Row > Start Row when MADCTL D4=1:



If End Row < Start Row when MADCTL D4=0:



If End Row < Start Row when MADCTL D4=1:



If End Row = Start Row, then the Partial Area will be one Row.

Restriction

SR[15:0] and ER[15:0] should have the range below

(Parameter range: 0 ≤ SR[15:0], ER[15:0] ≤ 431(01AFh)

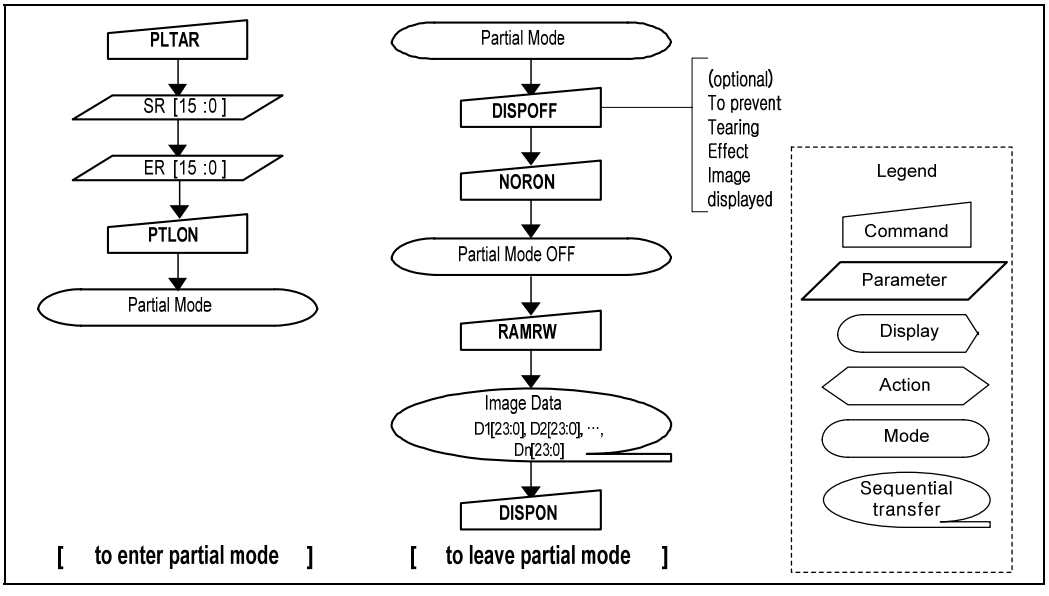
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	SR[15:0]	ER[15:0]
Power On Sequence	0000h	01AFh
S/W Reset	0000h	01AFh
H/W Reset	0000h	01AFh

Flow Chart



5.2.21. TEOFF : Tearing Effect Line OFF (34h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEOFF	W	0	0	0	1	1	0	1	0	0	34h
parameter	No Parameter										
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.										
Restriction	This command has no effect when Tearing Effect output is already OFF.										

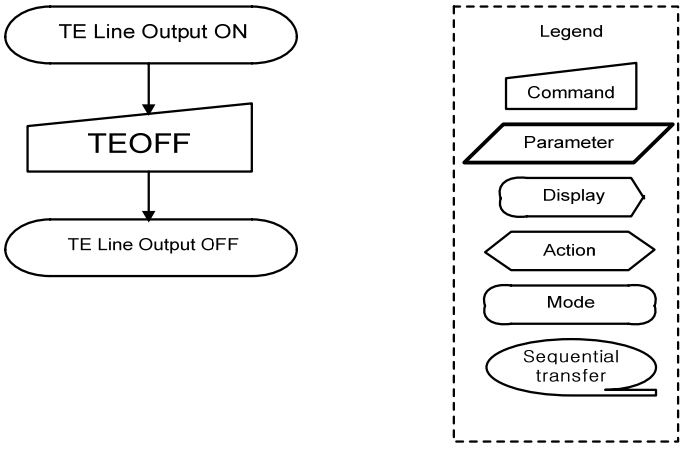
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

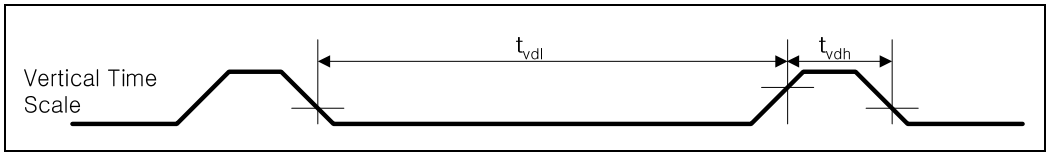
Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

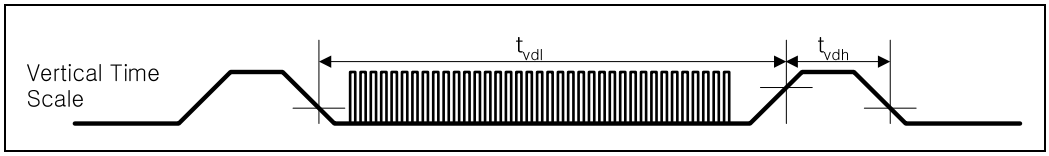
Flow Chart

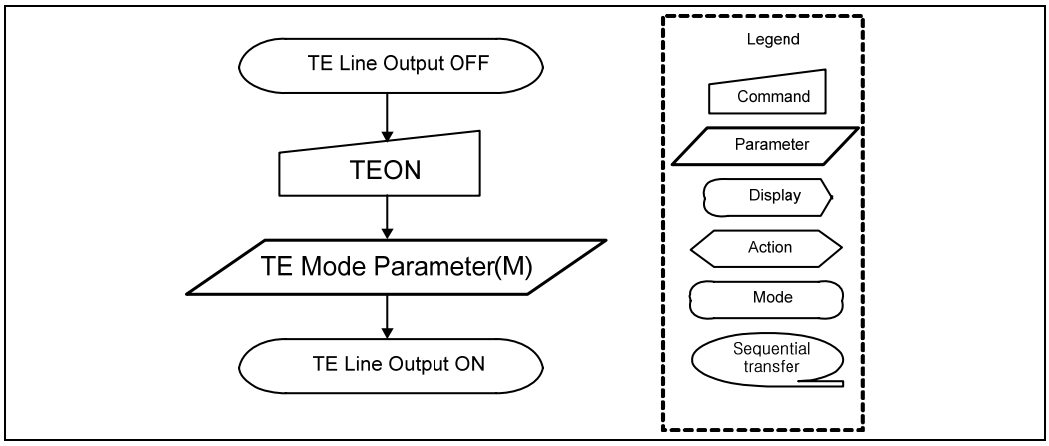


5.2.22. TEON : Tearing Effect Line ON (35h)

<table>
<tr><th>Inst / Para</th><th>R/W</th><th>DCX</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>TEON</td><td rowspan="2">W</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>35h</td></tr>
<tr><td>parameter</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>M0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="11">This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit D4.
The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. The TE has a different signal by interface mode.

1) MPU Type I interface
When M0=0: The Tearing Effect Output line consists of V-Blanking information only.
 

When M0=1: The Tearing Effect Output line consists of both V-Blanking and H-Blanking Information.
 
</td></tr>
<tr><td>Restriction</td><td colspan="11">This command has no effect when Tearing Effect output is already ON.</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Tearing effect off & M=0</td></tr><tr><td>S/W Reset</td><td>Tearing effect off & M=0</td></tr><tr><td>H/W Reset</td><td>Tearing effect off & M=0</td></tr></table></td></tr>
</table>

Flow Chart	

TE Line Output OFF
TEON
TE Mode Parameter(M)
TE Line Output ON
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

5.2.23. MADCTL : Memory Data Access Control (36h)

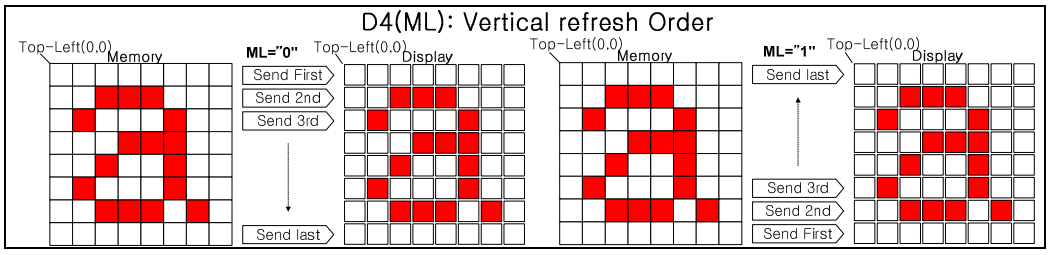
Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MADCTL	W	0	0	0	1	1	0	1	1	0	36h
parameter		1	D7	D6	D5	D4	D3	D2	0	0	xx

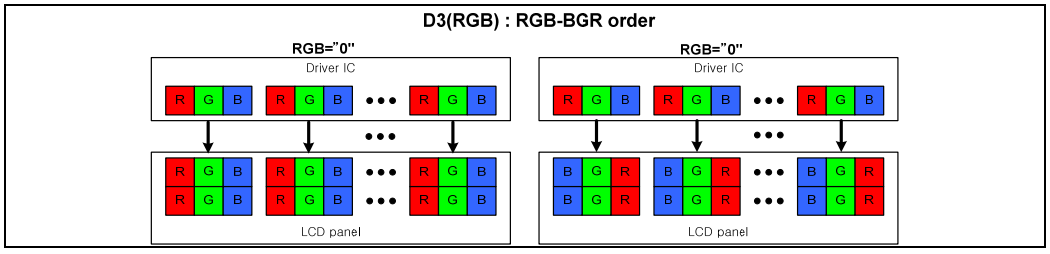
Description

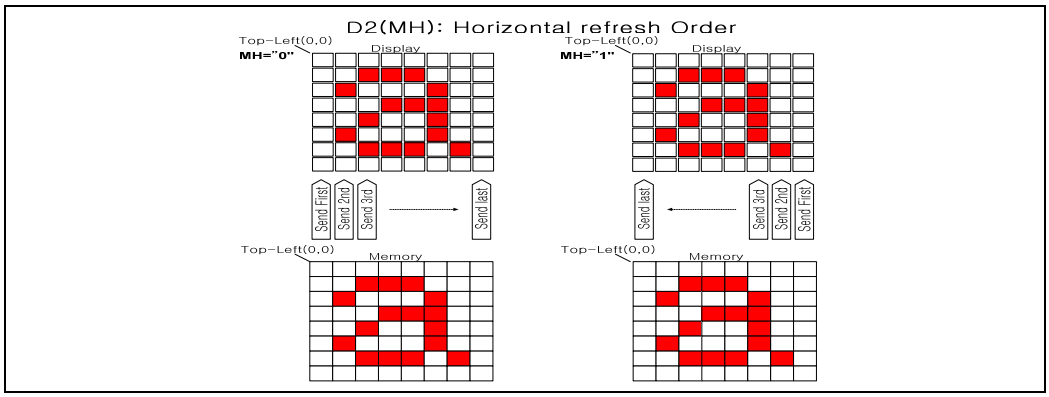
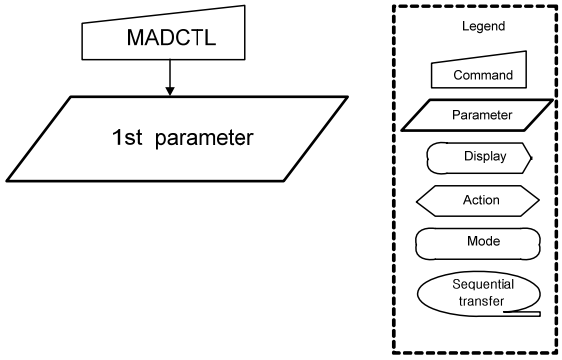
This command defines the read/write scanning direction of the frame memory.

This command makes no change on the other driver status.

Bit	Name	Description
D7	Page Address order(MY)	These 3-bits control MCU for the memory write/read direction.
D6	Column Address order(MX)	
D5	Page/Column exchange(MV)	
D4	Vertical refresh order(ML)	LCD Vertical refresh direction control
D3	RGB-BGR order(RGB)	Color selector refresh direction control (0=RGB color filter panel, 1=BGR color filter panel)
D2	Display Data Latch order(MH)	LCD horizontal refresh direction control





<table>
<tr><td></td><td> 
</td></tr>
<tr><td>Restriction</td><td>D1 and D0 of the 1st parameter are set to ‘00’internally.
D2 is Read/Write Register Only, It is not active Function.</td></tr>
<tr><td>Register Availability</td><td><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>D7=0, D6=0, D5=0, D4=0, D3=0, D2=0</td></tr>
<tr><td>S/W Reset</td><td>No Change</td></tr>
<tr><td>H/W Reset</td><td>D7=0, D6=0, D5=0, D4=0, D3=0, D2=0</td></tr>
</table></td></tr>
<tr><td>Flowchart</td><td> 
</td></tr>
</table>

5.2.24. IDMOFF : Idle Mode Off (38h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMOFF	W	0	0	0	1	1	1	0	0	0	38h

Parameter

No Parameter

Description

This command turns Idle mode off.

There will be no abnormal visible effect during the mode transition of the display.

During the idle off mode,

1. LCD can display maximum 16M-colors.
2. Normal frame frequency is applied.

Restriction

This command has no effect when module is already in idle off mode.

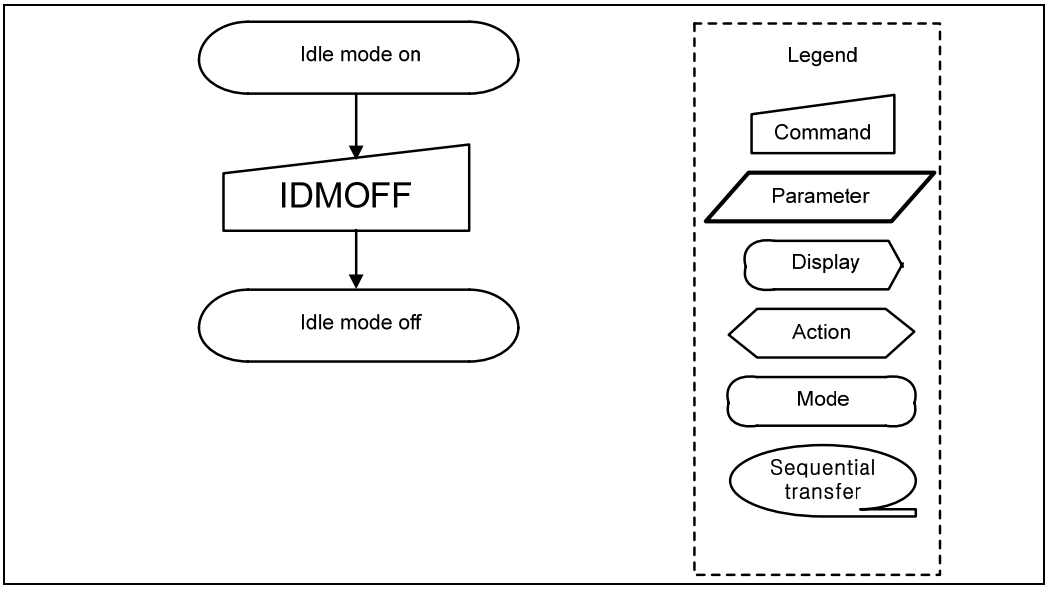
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flowchart



5.2.25. IDMON : Idle Mode On (39h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMON	W	0	0	0	1	1	1	0	0	1	39h
Parameter	No Parameter										

Description

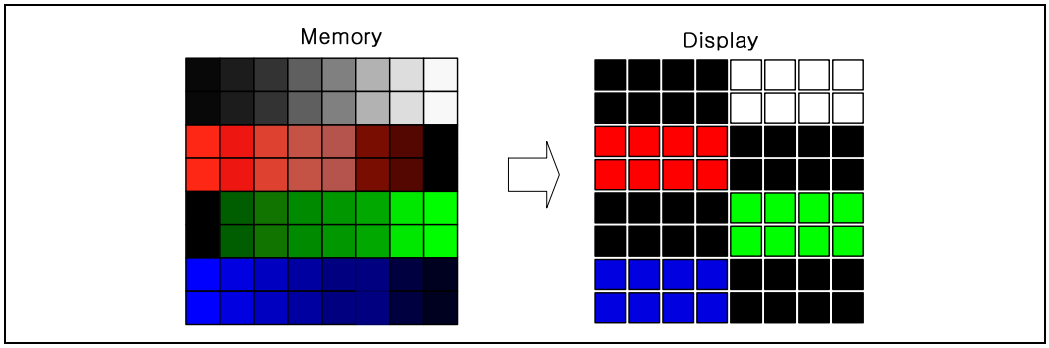
This command turns Idle mode on. (Refer to section 4.9 8-Color mode)

There will be no abnormal visible effect during mode transition.

During the idle on mode,

1. Color expression is reduced to 8-color. 8-color is displayed by MSB of each R, G, and B in the Frame Memory.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38h) command

(Example)



Color	$R_7R_6R_5R_4R_3R_2R_1R_0$	$G_7G_6G_5G_4G_3G_2G_1G_0$	$B_7B_6B_5B_4B_3B_2B_1B_0$
Black	0XXXXXXX	0XXXXXXX	0XXXXXXX
Blue	0XXXXXXX	0XXXXXXX	1XXXXXXX
Red	1XXXXXXX	0XXXXXXX	0XXXXXXX
Magenta	1XXXXXXX	0XXXXXXX	1XXXXXXX
Green	0XXXXXXX	1XXXXXXX	0XXXXXXX
Cyan	0XXXXXXX	1XXXXXXX	1XXXXXXX
Yellow	1XXXXXXX	1XXXXXXX	0XXXXXXX
White	1XXXXXXX	1XXXXXXX	1XXXXXXX

Note. “X“ denotes “Don’t care”

Restriction	This command has no effect when module is already in idle off mode.

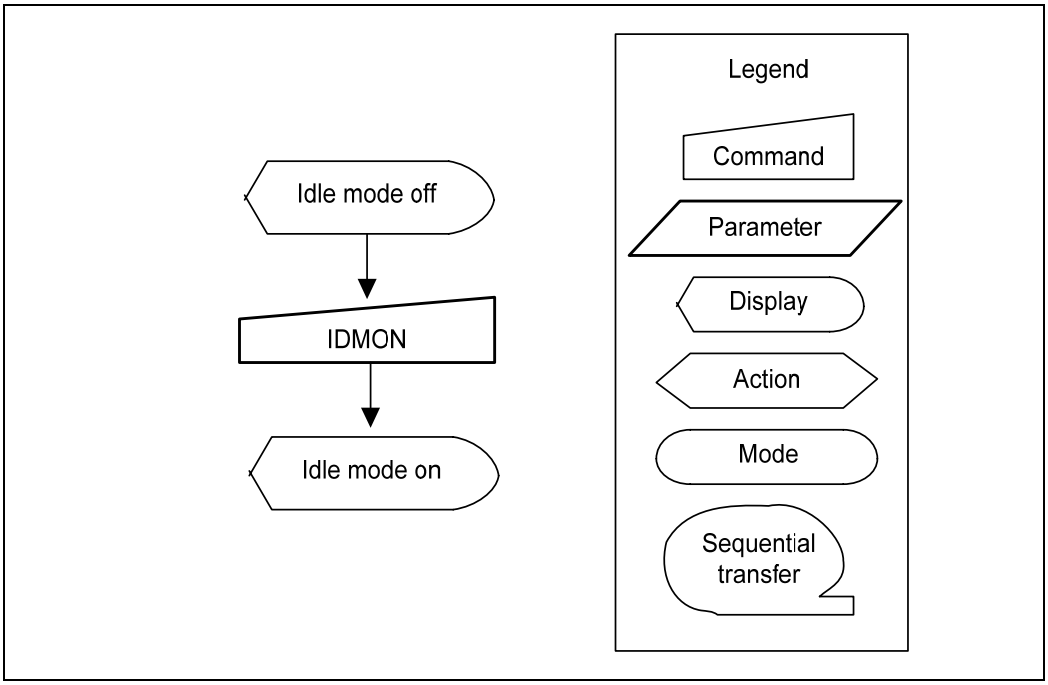
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

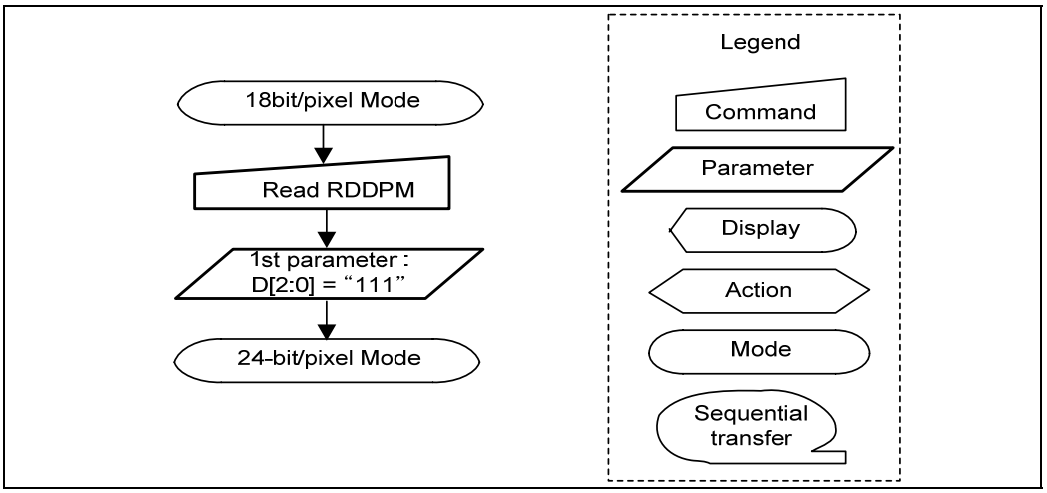
Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart



5.2.26. COLMOD : Interface Pixel Format (3Ah)

<table>
<tr><th>Inst / Para</th><th>R/W</th><th>DCX</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>COLMOD</td><td rowspan="2">W</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3Ah</td></tr>
<tr><td>Parameter</td><td>1</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="11">This command is used to define the format of RGB picture data, which is to be transferred via the MPU interface. The formats are as shown in the table below.
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>-</td><td>“0” (Not Used)</td></tr>
<tr><td>D6</td><td rowspan="3">RGB Interface Color Format (VFPF)</td><td rowspan="3">“101”=16-bits/pixel
“110”=18-bits/pixel
"111"= 24-bits/pixel
Others = not defined</td></tr>
<tr><td>D5</td></tr>
<tr><td>D4</td></tr>
<tr><td>D3</td><td>-</td><td>“0” (Not Used)</td></tr>
<tr><td>D2</td><td rowspan="3">Control Interface Color Format (IFPF)</td><td rowspan="3">“101”=16-bits/pixel
“110”=18-bits/pixel
"111"= 24-bits/pixel
Others = not defined</td></tr>
<tr><td>D1</td></tr>
<tr><td>D0</td></tr>
</table>
Note. In 16-bit/pixel or 18-bit/pixel mode, display data is expended to 24bit data. Refer to Section 3.2.1
12-bits/pixel (4096 color mode) is not supported.</td></tr>
<tr><td>Restrictions</td><td colspan="11">There is no visible effect until the frame memory is written.</td></tr>
<tr><td>Register Availability</td><td colspan="11">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal mode on, Idle mode off, Sleep out</td><td>Yes</td></tr>
<tr><td>Normal mode on, Idle mode on, Sleep out</td><td>Yes</td></tr>
<tr><td>Partial mode on, Idle mode off, Sleep out</td><td>Yes</td></tr>
<tr><td>Partial mode on, Idle mode on, Sleep out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="11">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>24-bits/pixel</td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td>24-bits/pixel</td></tr>
</table>
</td></tr>
</table>

Flow Chart	

18bit/pixel Mode
Read RDDPM
1st parameter :
D[2:0] = “111”
24-bit/pixel Mode
Legend
Command
Parameter
Display
Action
Mode
Sequential
transfer

5.2.27. RDID1 : Read ID1 Value (DAh)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID1	R	0	1	1	0	1	1	0	1	0	DAh
Dummy read		1	X	X	X	X	X	X	X	X	X
2nd Parameter		1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	xx
Description	This read byte identifies the LCD module's manufacturer. Note: "X" denotes "Don't care"										
Restrictions	There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.5.2.										

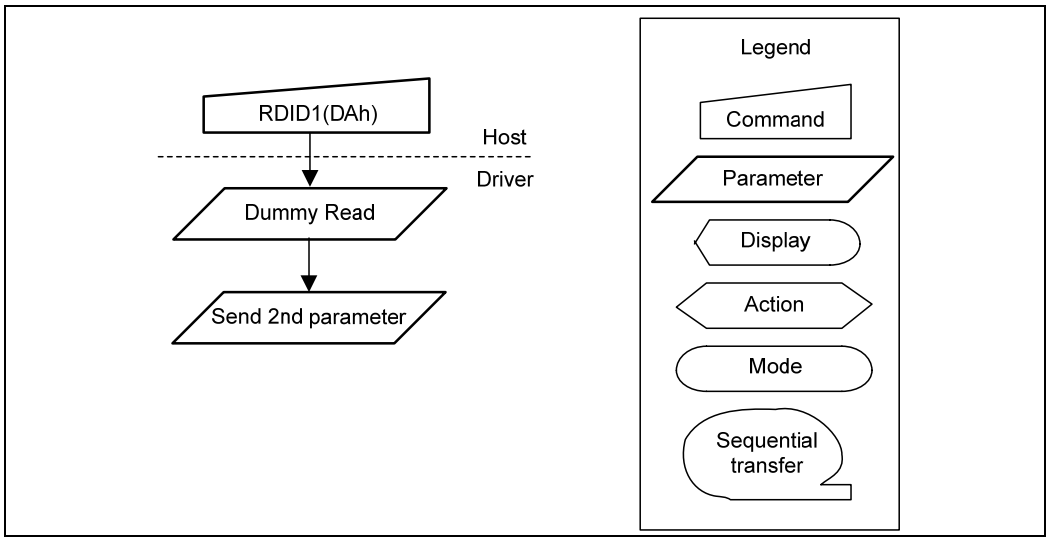
Register Availability

Status	Availability
Normal mode on, Idle mode off, Sleep out	Yes
Normal mode on, Idle mode on, Sleep out	Yes
Partial mode on, Idle mode off, Sleep out	Yes
Partial mode on, Idle mode on, Sleep out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	(MTP value)
S/W Reset	(MTP value)
H/W Reset	(MTP value)

Flow Chart



5.2.28. RDID2 : Read ID2 Value (DBh)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID2	R	0	1	1	0	1	1	0	1	1	DBh
Dummy read		1	X	X	X	X	X	X	X	X	X
2nd Parameter		1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	xx

Description

This read byte is used to track the LCD module/driver version. It is provided by a display supplier and updated each time a revision is made to the display, material or construction specifications.

Note. "X" denotes "Don't care"

Restrictions

There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.5.2.

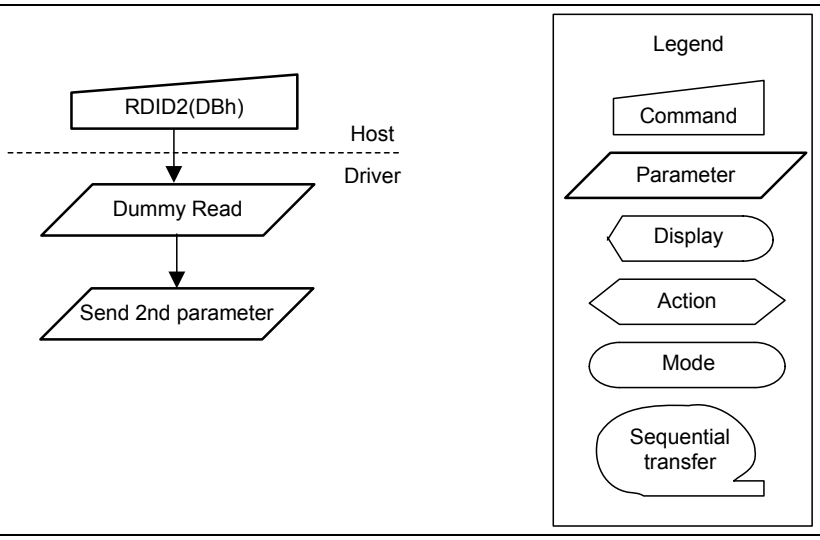
Register Availability

Status	Availability
Normal mode on, Idle mode off, Sleep out	Yes
Normal mode on, Idle mode on, Sleep out	Yes
Partial mode on, Idle mode off, Sleep out	Yes
Partial mode on, Idle mode on, Sleep out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	(MTP value)
S/W Reset	(MTP value)
H/W Reset	(MTP value)

Flow Chart



5.2.29. RDID3 : Read ID3 Value (DCh)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID3	R	0	1	1	0	1	1	1	0	0	DC
Dummy read		1	X	X	X	X	X	X	X	X	X
2nd Parameter		1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	xx
Description	This read byte identifies the LCD module/driver. It is specified by a user. Note: "X" denotes "Don't care"										
Restrictions	There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.5.2.										

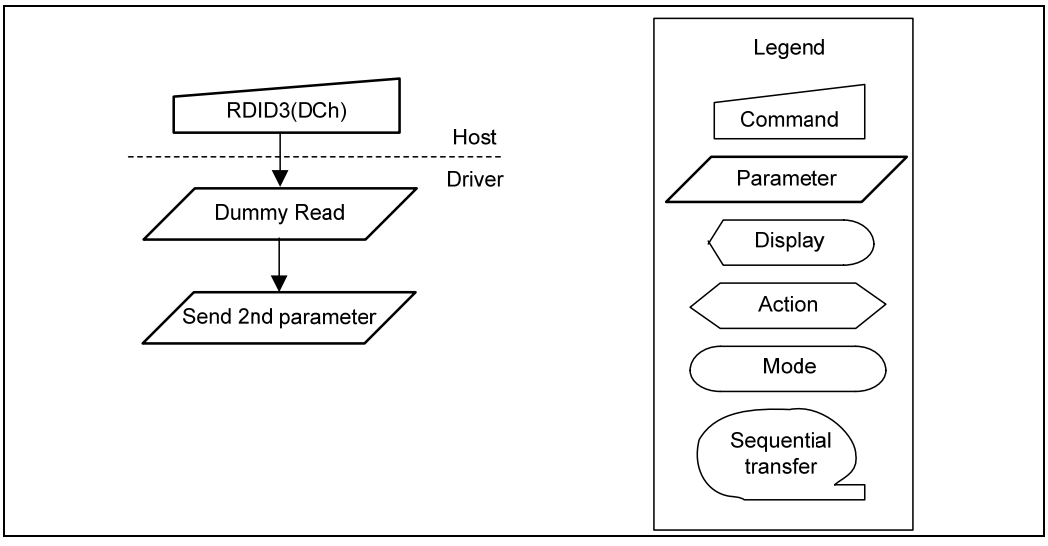
Register Availability

Status	Availability
Normal mode on, Idle mode off, Sleep out	Yes
Normal mode on, Idle mode on, Sleep out	Yes
Partial mode on, Idle mode off, Sleep out	Yes
Partial mode on, Idle mode on, Sleep out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	(MTP value)
S/W Reset	(MTP value)
H/W Reset	(MTP value)

Flow Chart



5.2.30. WRDISBV : Write Manual Brightness (51h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRDISBV	W	0	0	1	0	1	0	0	0	1	51
1st para		1	MAN_ BRIGHT[7]	MAN_ BRIGHT[6]	MAN_ BRIGHT[5]	MAN_ BRIGHT[4]	MAN_ BRIGHT[3]	MAN_ BRIGHT[2]	MAN_ BRIGHT[1]	MAN_ BRIGHT[0]	-

This command is used to set the manual brightness value. If the manual brightness is used (BC_MODE = “01” or “11”), the value of register “MAN_BRIGHT[7:0] is selected or merged with the MIE brightness to generate BC.

Table 116. MAN_BRIGHT[7:0]

MAN_BRIGHT[7:0]	Brightness Level
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
…	…
1111_1100	252
1111_1101	253
1111_1110	254
1111_1111	255

Status	Default Value
Initial	MAN_BRIGHT[7:0] = 0000_0000

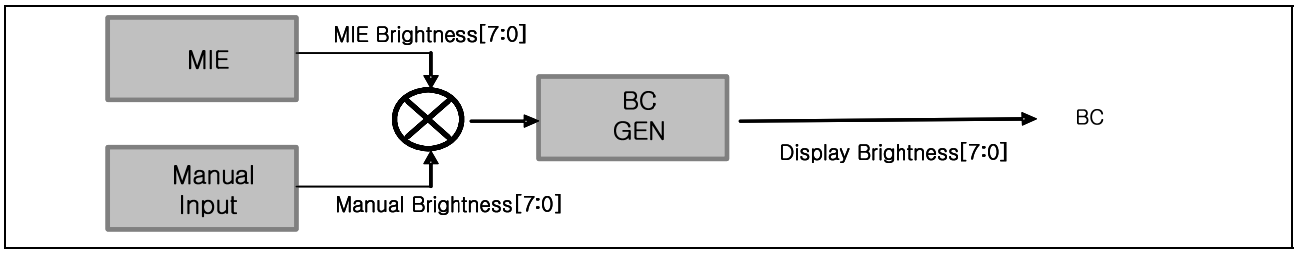


Figure 146. Manual brightness

The display brightness level is calculated with the following formula.

$$Display\_Brightness = MIE\_Brightness \; X \; Manual\_Brightness \; / \; 255$$

Figure 147. Calculation formula

The MIE brightness has transition time A and the manual brightness has transition time B.

The maximum transition time is transition time C (C ≤ A + B).

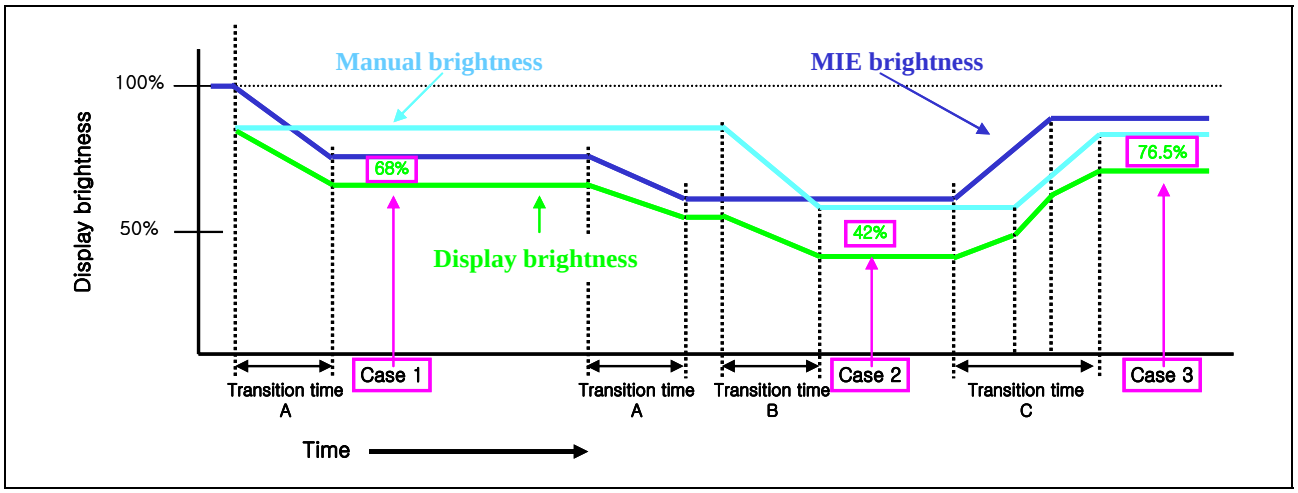


Figure 148. Example of manual brightness

Table 117. Example of manual brightness

Operation Mode	Manual Brightness	MIE Brightness	Display Brightness
Case 1	85 %	80 %	68 %
Case 2	60 %	70 %	42 %
Case 3	85 %	90 %	76.5 %

5.2.31. RDDISBV : Read Display Brightness (52h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDISBV	R	0	0	1	0	1	0	0	1	0	52
Dummy Read		1	X	X	X	X	X	X	X	X	X
2nd para		1	DISP_ BRIGHT [7]	DISP_ BRIGHT [6]	DISP _ BRIGHT [5]	DISP _ BRIGHT [4]	DISP _ BRIGHT [3]	DISP _ BRIGHT [2]	DISP _ BRIGHT [1]	DISP _ BRIGHT [0]	-

This command is used to read the display brightness value. It is a real brightness value of BC output which is calculated with MIE brightness and manual brightness. The value of this register is updated after display V-sync and host can read exact value after display V-sync. RDDISBV is valid in case that BCTRL(WRCTRLD 53h) = 1.

Note. There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.5.2.

Table 118. DISP_BRIGHT[7:0]

DISP_BRIGHT[7:0]	Brightness Level
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
…	…
1111_1100	252
1111_1101	253
1111_1110	254
1111_1111	255

Status	Default Value
Initial	DISP_BRIGHT[7:0] = 0000_0000

5.2.32. WRCTRLD : Write BL Control (53h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCTRLD	W	0	0	1	0	1	0	0	1	1	53
1st para		1	0	0	BCTRL	0	DD	BL	0	0	-

5.2.32.1. BCTRL

This register is used to enable the backlight control block. If BCTRL is turned off, the BL control block is not working and BC output is fixed to low.

Table 119. BCTRL

BCTRL	BL Control
0	Off
1	On

Note 1. When BCTRL does ON, establish VBP and VFP by same value.

Status	Default Value
Initial	BCTRL = 0

5.2.32.2. DD

This register is used to enable the manual brightness dimming function. The manual brightness should be changed smoothly for preventing a visible artifact, e.g. flicker. So the dimming function is needed when the transition of input manual brightness is fast to make a visible artifact. When the manual dimming is enabled, the new manual brightness value has to be changed after former dimming transition is finished. The transition time is controlled by DT[2:0].

Table 120. DD

DD	Manual Dimming Function
0	Off
1	On

Status	Default Value
Initial	DD = 0

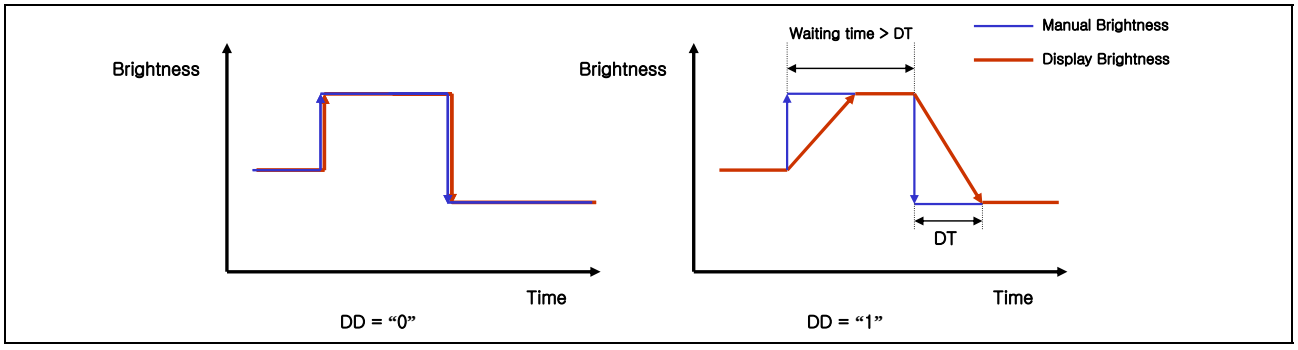


Figure 149. Manual dimming function

5.2.32.3. BL

This register is used to enable the BC output. Even if the value of BL is “0”, the backlight control block is working when BCTRL is “1”. And the host can read the display brightness value (DISP_BRIGHT[7:0]) and control the BLU directly.

Table 121. BL

BL	BC state
0	Low
1	Active

Status	Default Value
Initial	BL = 0

5.2.33. RDCTRLD : Read BL Control (54h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCTRLD	R	0	0	1	0	1	0	1	0	0	54
Dummy Read		1	X	X	X	X	X	X	X	X	X
2nd para		1	0	0	BCTRL	0	DD	BL	0	0	-

This command is used to Read BL Control register. For details, refer to Write BL Control (53h).

Note. There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.5.2

5.2.34. WRCABC : Write MIE Mode (55h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCABC	W	0	0	1	0	1	0	1	0	1	55
1st para		1	0	0	0	0	0	0	MIE_ MODE [1]	MIE_ MODE [0]	-

This command is used to select the operation mode of MIE. If the MIE is off mode, the BLU brightness value of MIE is set to 255.

Table 122. MIE_MODE[1:0]

MIE_MODE[1:0]	Operation Mode
00	Off
01	UI (User Interface)
10	Still Image
11	Moving Image

Status	Default Value
Initial	MIE_MODE[1:0] = 00

5.2.35. RDCABC : Read MIE Mode (56h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCABC	R	0	0	1	0	1	0	1	1	0	56
Dummy Read		1	X	X	X	X	X	X	X	X	X
2nd para		1	0	0	0	0	0	0	MIE_ MODE [1]	MIE_ MODE [0]	-

This command is used to read MIE mode register. For details, refer to Write MIE Mode (55h).

Note. There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.5.2

5.2.36. WRCABCMB : Write Minimum Brightness (5Eh)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCABCMB	W	0	0	1	0	1	1	1	1	0	5E
1st para		1	MIN_ BRIGHT[7]	MIN_ BRIGHT[6]	MIN_ BRIGHT[5]	MIN_ BRIGHT[4]	MIN_ BRIGHT[3]	MIN_ BRIGHT[2]	MIN_ BRIGHT[1]	MIN_ BRIGHT[0]	-

This command is used to set the minimum brightness value.

The MIE function is automatically reduced the backlight brightness based on the content of image. In the case of the combination with the manual brightness setting, the display brightness can be too dark. It must affect to image quality degradation. So the minimum brightness setting is used to avoid too much brightness reduction.

When the MIE is activated, the display brightness can not be reduced less than the value of minimum brightness setting. The image processing function is worked as normal, even if the display brightness can not be decreased by the minimum brightness setting.

This function of the manual brightness setting does not affect to the other functions. The smooth transition and dimming function can be worked as normal. The manual brightness shouldn't be set less than the minimum brightness. When the BL control block is turned off (BCTRL=0), the MIE minimum brightness setting is ignored.

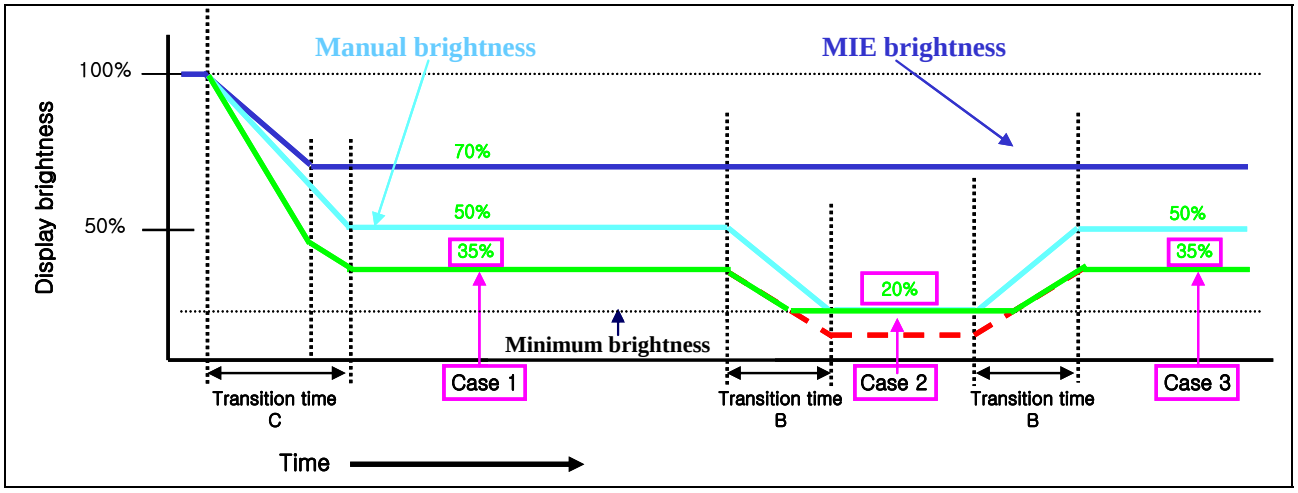


Figure 150. Example of minimum brightness

Table 123. Example of minimum brightness (Minimum brightness = 20%)

Operation Mode	Manual Brightness	MIE Brightness	Calculated Display Brightness	Display Brightness
Case 1	50 %	70 %	35%	35 %
Case 2	20 %	70 %	14%	20 %
Case 3	50 %	70 %	35%	35 %

Table 124. MIN_BRIGHT[7:0]

MIN_BRIGHT[7:0]	Brightness Level
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
…	…
1111_1100	252
1111_1101	253
1111_1110	254
1111_1111	255

Status	Default Value
Initial	MIN_BRIGHT[7:0] = 0000_0000

5.2.37. RDCABCMB : Read Minimum Brightness (5Fh)

5Fh	Read Minimum Brightness										
	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCABCMB	R	0	0	1	0	1	1	1	1	1	5F
Dummy Read		1	X	X	X	X	X	X	X	X	X
2nd para		1	MIN_ BRIGHT[7]	MIN_ BRIGHT [6]	MIN_ BRIGHT [5]	MIN_ BRIGHT[4]	MIN_ BRIGHT[3]	MIN_ BRIGHT[2]	MIN_ BRIGHT[1]	MIN_ BRIGHT[0]	-

This command is used to read Minimum Brightness register. For details, refer to Write Minimum Brightness (5Eh).

RDCABCMB is valid in case that BCTRL(WRCTRLD 53h) = 1.

Note. There is no dummy read parameter at serial I/F, refer to 3.1.4.2, 3.1.5.2

MIECTL1 : Write MIE Control 1 (CAh)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MIECTL1	W	0	1	1	0	0	1	0	1	0	CA
1st para		1	RRC [7]	RRC [6]	RRC [5]	RRC [4]	RRC [3]	RRC [2]	RRC [1]	RRC [0]	-
2nd para		1	IERC [7]	IERC [6]	IERC [5]	IERC [4]	IERC [3]	IERC [2]	IERC [1]	IERC [0]	-
3rd para		1	0	0	ONOFF_DIMM_EN	SERC [4]	SERC [3]	SERC [2]	SERC [1]	SERC [0]	-

5.2.37.1. RRC[7:0]

This register is used to adjust the reduction rate of the backlight power.

$$Adjusted\_Power\_Reduction\_Rate = Power\_Reduction\_Rate\ X\ \frac{RRC}{128}$$

Figure 151. Power reduction rate

The Power Reduction Rate is the power reduction rate by the MIE algorithm. The Reduction range is from '0' (no reduction) to two times of the contents adaptive backlight power. To increase the value of RRC, more backlight power can be reduced but the displayed image become darker. The other way, brighter image is obtained by decreasing the value of RRC.

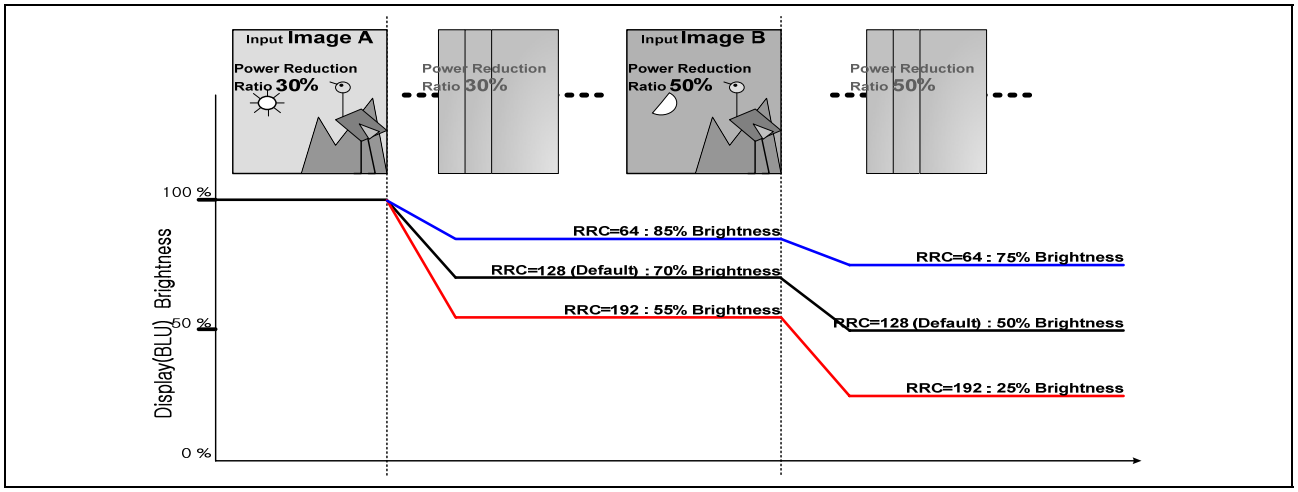


Figure 152. Example of RRC

Table 125. RRC[7:0]

RRC[7:0]	Adjusted Power Reduction Rate
0000_0000	Power Reduction Rate x 0/128
0000_0001	Power Reduction Rate x 1/128
0000_0010	Power Reduction Rate x 2/128
…	…
1000_0000	Power Reduction Rate x 128/128
…	…
1111_1101	Power Reduction Rate x 253/128
1111_1110	Power Reduction Rate x 254/128
1111_1111	Power Reduction Rate x 255/128

Status	Default Value
Initial	RRC[7:0] = 1000_0000

5.2.37.2. IERC[7:0]

This register is used to adjust the image enhancement rate.

$$Adjusted\_Image\_Enhancement\_Rate = Image\_Enhancement\_Rate \; X \; \frac{IERC}{128}$$

Figure 153. Image enhancement rate

If the value of IERC is '0', there is no enhancement in output image. If its value is '255', the enhancement rate is two times of Image Enhancement Rate. If the value of IERC is increased, brighter image is obtained but the quality of displayed image may be decreased. The other way, if the value of IERC register is decreased, the quality of image will be increased.

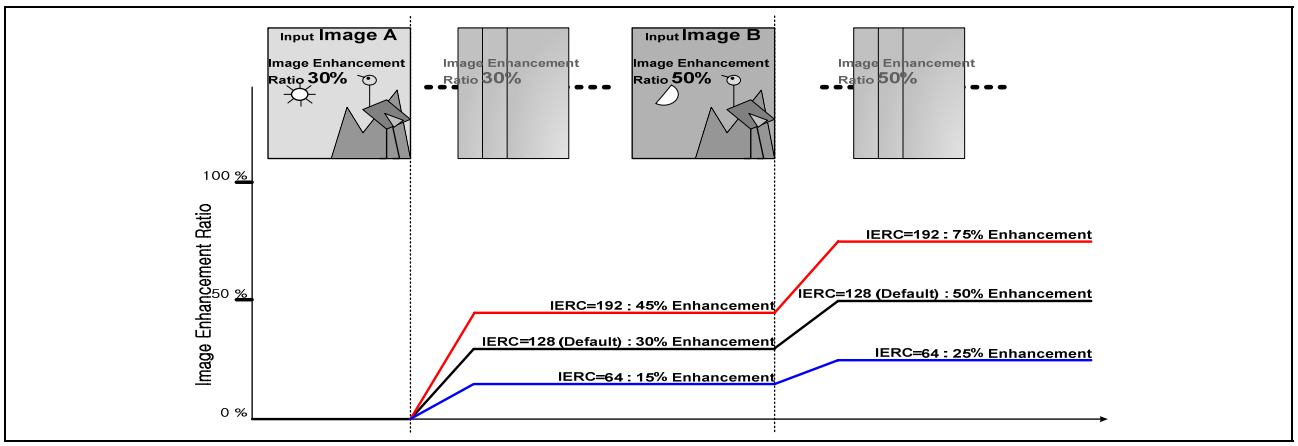


Figure 154. Example of IERC

Table 126. IERC[7:0]

IERC[7:0]	Adjust Image Enhancement Rate
0000_0000	Image Enhancement Rate x 0/128
0000_0001	Image Enhancement Rate x 1/128
0000_0010	Image Enhancement Rate x 2/128
…	…
1000_0000	Image Enhancement Rate x 128/128
…	…
1111_1101	Image Enhancement Rate x 253/128
1111_1110	Image Enhancement Rate x 254/128
1111_1111	Image Enhancement Rate x 255/128

Status	Default Value
Initial	IERC[7:0] = 1000_0000

5.2.37.3. ONOFF_DIMM_EN

This register is used to enable the on/off dimming function of MIE.

The MIE has a dimming function for preventing abnormal visible artifacts when the MIE is turning on or off.
If the ONOFF_DIMM_EN is “1”, the MIE is smoothly turning on or off. When the ONOFF_DIMM_EN is “0”, the MIE is turning on or off immediately. The transition time is controlled by CST[1:0].
If the MIE mode is changed during on/off dimming transition, it will be updated after finishing the dimming transition.

Table 127. ONOFF_DIMM_EN

ONOFF_DIMM_EN	On / Off Dimming Function
0	Disable
1	Enable

Status	Default Value
Initial	ONOFF_DIMM_EN = 0

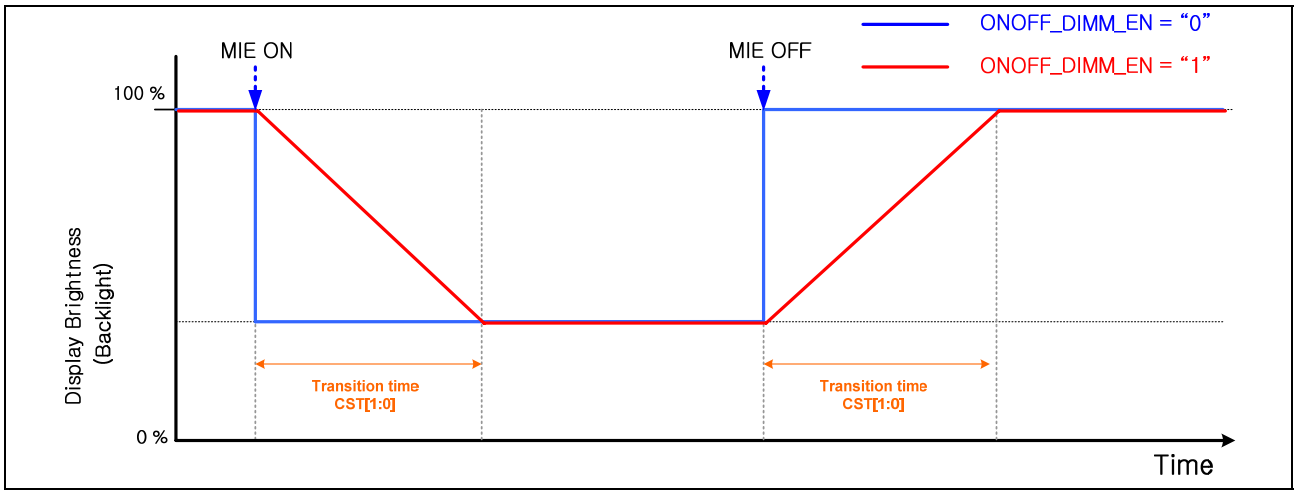


Figure 155. Example of MIE on / off dimming transition control

5.2.37.4. SERC[4:0]

This register is used to adjust the Image Saturation Enhancement Rate.

$$Adjusted\_Saturation\_Enhancement\_Rate = Saturation\_Enhancement\_Rate\ X\ \frac{SERC}{16}$$

Figure 156. Saturation enhancement rate

If the value of SERC is '0', there is no saturation enhancement in output image. If the value of SERC is increased, the saturation enhancement rate will be increased and more vivid image is obtained. The other way, if the value of SERC is decreased, the saturation enhancement rate will be decreased.

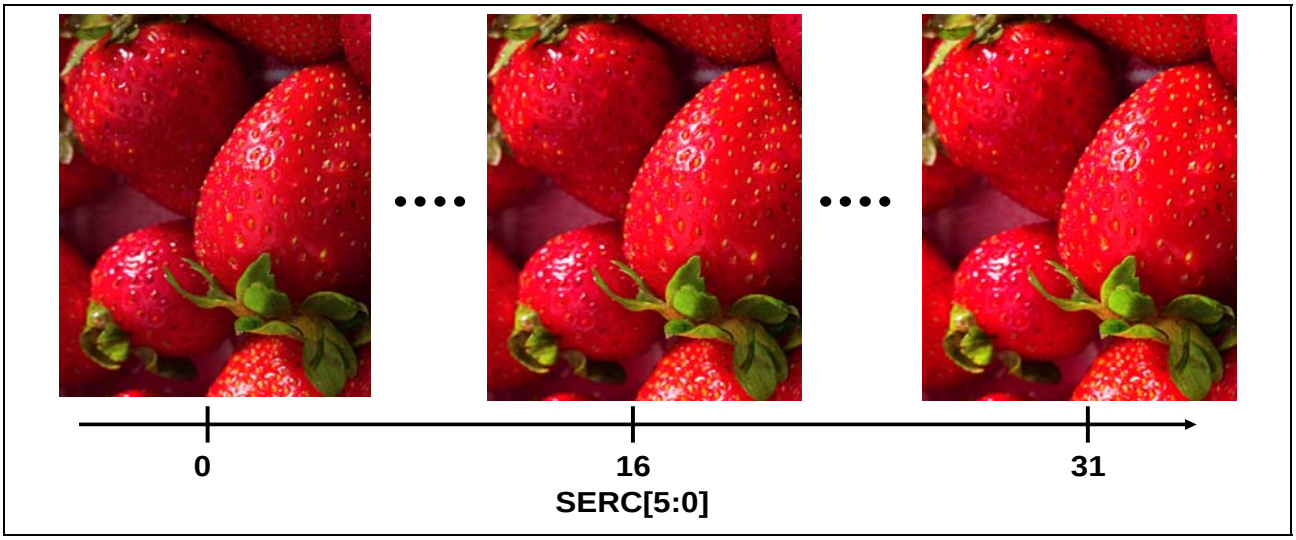


Figure 157. Example of SERC

Table 128. SERC[4:0]

SERC[4:0]	Adjust Saturation Enhancement Rate
00000	Saturation Enhancement Rate x 0/16
00001	Saturation Enhancement Rate x 1/16
00010	Saturation Enhancement Rate x 2/16
…	…
10000	Saturation Enhancement Rate x 16/16
…	…
11101	Saturation Enhancement Rate x 29/16
11110	Saturation Enhancement Rate x 30/16
11111	Saturation Enhancement Rate x 31/16

Status	Default Value
Initial	SERC[4:0] = 10000

5.2.38. BCMODE : Write BL Control Mode (CBh)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BCMODE	W	0	1	1	0	0	1	0	1	1	CB
1st para		1	0	0	0	0	0	0	BC_ MODE[1]	BC_ MODE[0]	-

This command is used to select the source of brightness value for the display brightness calculation.

Table 129. BCMODE[1:0]

BCMODE[1:0]	Brightness Source
00	Setting disabled
01	Manual Brightness
10	MIE Brightness
11	Merged Brightness (MIE + Manual)

Status	Default Value
Initial	BC_MODE[1:0] = 01

5.3. DESCRIPTION OF LEVEL2 COMMAND

Command Description Tables are explained by 80mode Interface standard.

Level2 Commands are not readable in SPI.

5.3.1. DSTB : Deep Stand By mode (B0h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DSTB	W	0	1	0	1	1	0	0	0	0	B0
1st para		1	0	0	0	0	0	0	0	DSTB	-

DSTB: When DSTB = 1, the S6D04D1 enters the deep standby mode, where the power supply for the internal logic is off to save more power than the standby mode. The GRAM data and the instruction sets are prohibited during the deep standby mode and they must be reset after releasing from the deep standby mode.

Status	Default Value
Intial	DSTB = 0

SE : Sharpness Enhancement (C6h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SE	W	0	1	1	0	0	0	1	1	0	C6
1st para		1	SE_ MODE	0	0	0	0	0	GAIN [1]	GAIN [0]	-

SE_MODE: sets sharpness enhancement mode when SE_MODE = 1.

GAIN[1 :0]: sets the added gain about edge information.

GAIN[1:0]	Weight
00	1
01	2
10	3
11	4

Status	Default Value
Intial	SE_MODE =0, GAIN[1:0] = 11

5.3.2. MIECTL2 : Write MIE Control 2 (CCh)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MIECTL2	R/W	0	1	1	0	0	1	1	0	0	CC
1st para		1	0	0	CAT [1]	CAT [0]	CST [1]	CST [0]	WIN VADD R0[8]	WIN VADD R0[7]	-
2nd para		1	WIN VADD R0[6]	WIN VADD R0[5]	WIN VADD R0[4]	WIN VADD R0[3]	WIN VADD R0[2]	WIN VADD R0[1]	WIN VADD R0[0]	WIN VADD R1[8]	-
3rd para		1	WIN VADD R1[7]	WIN VADD R1[6]	WIN VADD R1[5]	WIN VADD R1[4]	WIN VADD R1[3]	WIN VADD R1[2]	WIN VADD R1[1]	WIN VADD R1[0]	-
4th para		1	0	0	0	0	0	0	0	0	-
5th para		1	1	1	1	0	1	1	1	1	-

5.3.2.1. CAT[1:0]

This register is used to select the abrupt transition time. The MIE has two transition times based on image contents for preventing abnormal visible artifacts (e.g. flicker). The MIE controls transition time between CAT and CST automatically in moving mode (MIE_MODE = “11”).

- Abrupt transition time: If input image is changed abruptly, short transition time is needed.
- Smooth transition time: If input image is changed smoothly, long transition time is needed.

Table 130. CAT[1:0]

CAT[1:0]	Abrupt Transition Time
00	1 frame
01	2 frames
10	4 frames
11	8 frames

Status	Default Value
Initial	CAT[1:0] = 10

5.3.2.2. CST [1 :0]

This register is used to select the smooth transition time

Table 131. CST[1:0]

CST[1:0]	Smooth Transition Time
00	32 frames
01	64 frames
10	96 frames
11	128 frames

Status	Default Value
Initial	CST[1:0] = 00

An example of MIE transition time is illustrated as below. If the input image is changed abruptly, the MIE has an abrupt transition time “case (1)” and if the input image is changed smoothly, the MIE has a smooth transition time “case (2)”. The display brightness changes to target brightness abruptly “case (4)” when the abrupt change of image is happened during the smooth transition “case (3)”.

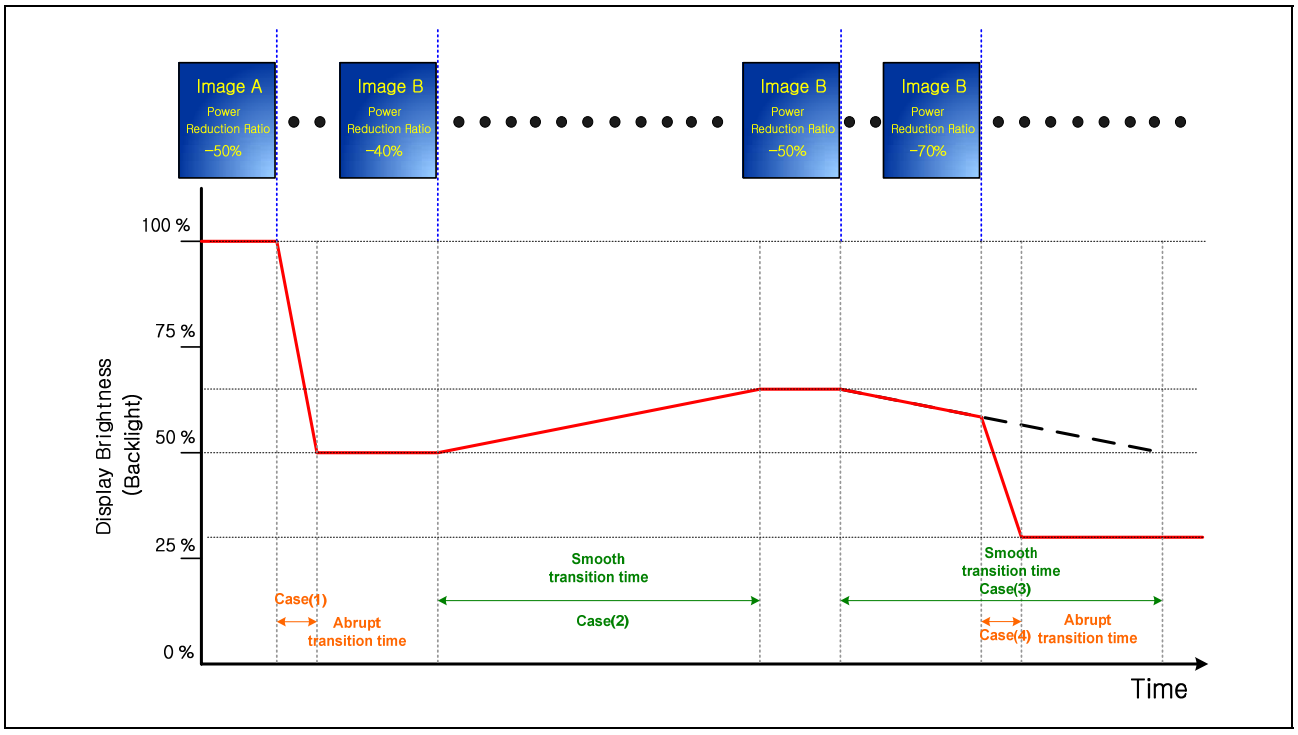


Figure 158. Example of MIE transition control

5.3.2.3. WINVADDR0[8:0]

This register is used to set the vertical start address of MIE window.

Table 132. WINVADDR0[8:0]

WINVADDR0[8:0]	Vertical Start Address of MIE Window
0_0000_0000	0
0_0000_0001	1
0_0000_0010	2
0_0000_0011	3
…	…
1_1010_0110	422
1_1010_0111	423
1_0011_1110	Setting disabled
…	…
1_1111_1111	Setting disabled

Status	Default Value
Initial	WINVADDR0[8:0] = 0_0000_0000

Note. WINVADDR1 – WINVADDR0 ≥100

5.3.2.4. WINVADDR1[8:0]

This register is used to set the vertical end address of MIE window.

Table 133. WINVADDR1[8:0]

WINVADDR1[8:0]	Vertical End Address of MIE Window
0_0000_0000	Setting disabled
0_0000_0001	Setting disabled
0_0000_0010	Setting disabled
0_0000_0011	Setting disabled
0_0000_0100	Setting disabled
0_0000_0101	Setting disabled
0_0000_0110	Setting disabled
0_0000_0111	Setting disabled
0_0000_1000	8
0_0000_1001	9
…	…
1_1010_1110	430
1_1010_1111	431
1_0100_0000	Setting disabled
…	…
1_1111_1111	Setting disabled

Status	Default Value
Initial	WINVADDR1[8:0] = 1_0011_1111

Note. WINVADDR1 – WINVADDR0 ≥ 100

The MIE can select the window area which is used to analysis and enhance input image. The outside area of the MIE window is not used to MIE analysis and there is no image enhancement.

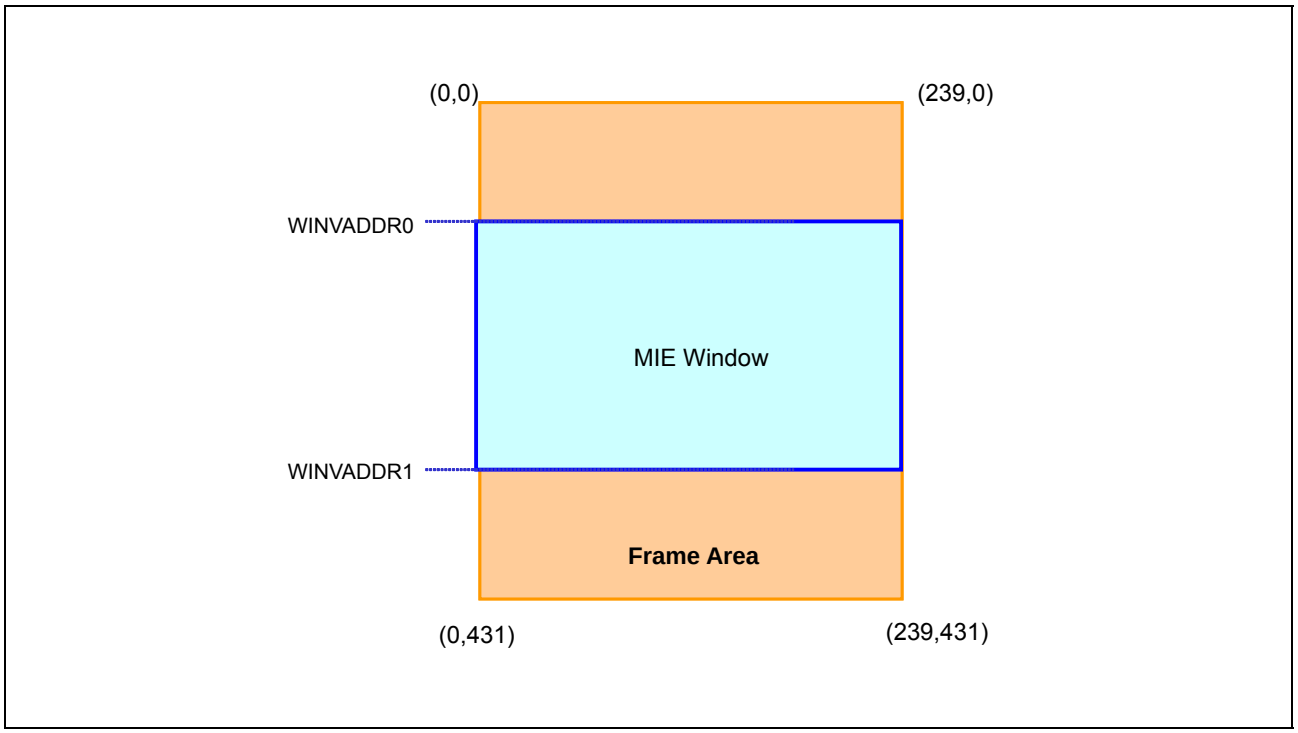


Figure 159. MIE window

MIECTL3 (CDh) : Write BL Control

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MIECTL3		0	1	1	0	0	1	1	0	1	CD
1st para		1	0	BC_ FRQ_ SEL[6]	BC_ FRQ_ SEL[5]	BC_ FRQ_ SEL[4]	BC_ FRQ_ SEL[3]	BC_ FRQ_ SEL[2]	BC_ FRQ_ SEL[1]	BC_ FRQ_ SEL[0]	-
2nd para		1	BL_ MODE_ INSLP	0	DT[2]	DT[1]	DT[0]	BL_ DRV_ EN	BL_ DIMM_ STEP[1]	BL_ DIMM_ STEP[0]	-

5.3.2.5. BC_FRQ_SEL[6:0]

This register is used to select the frequency of BC. To select the BC frequency, two registers are needed. Those register are BC_FRQ_SEL[6:0] and BL_DIMM_STEP[1:0].

For details, refer to the table of BC frequency.

Status	Default Value
Initial	BC_FRQ_SEL[6:0] = 000_0011

5.3.2.6. BL_MODE_IN_SLP

This register is used to select the state of BC when driver IC is sleep in mode.

Table 134. BL_MODE_IN_SLP

BL_MODE_IN_SLP	State of BC
0	Low
1	High

Status	Default Value
Initial	BL_MODE_IN_SLP = 0

Table 135. State of BC

PAD	State					
	Hard Reset	SW Reset	SLPIN		SPLOUT	
			Display On	Display Off	Display On	Display Off
BC	Low	Low	Fixed as BL_MODE_IN_SLP		Active	Low

5.3.2.7. DT[2:0]

This register is used to select the transition time of the manual dimming function.

Table 136. DT[2:0]

DT[2:0]	Transition Time	Dimming Step
000	16 frames	16
001	24 frames	24
010	32 frames	32
011	40 frames	40
100	48 frames	48
101	56 frames	56
110	64 frames	64
111	72 frames	72

$$※\ Transition\_Time = (DT[2:0] + 2)\ X\ 8\ X \frac{1}{Display\_Frequency}$$

Figure 160. Transition time of manual dimming function

Status	Default Value
Initial	DT[2:0] = 010

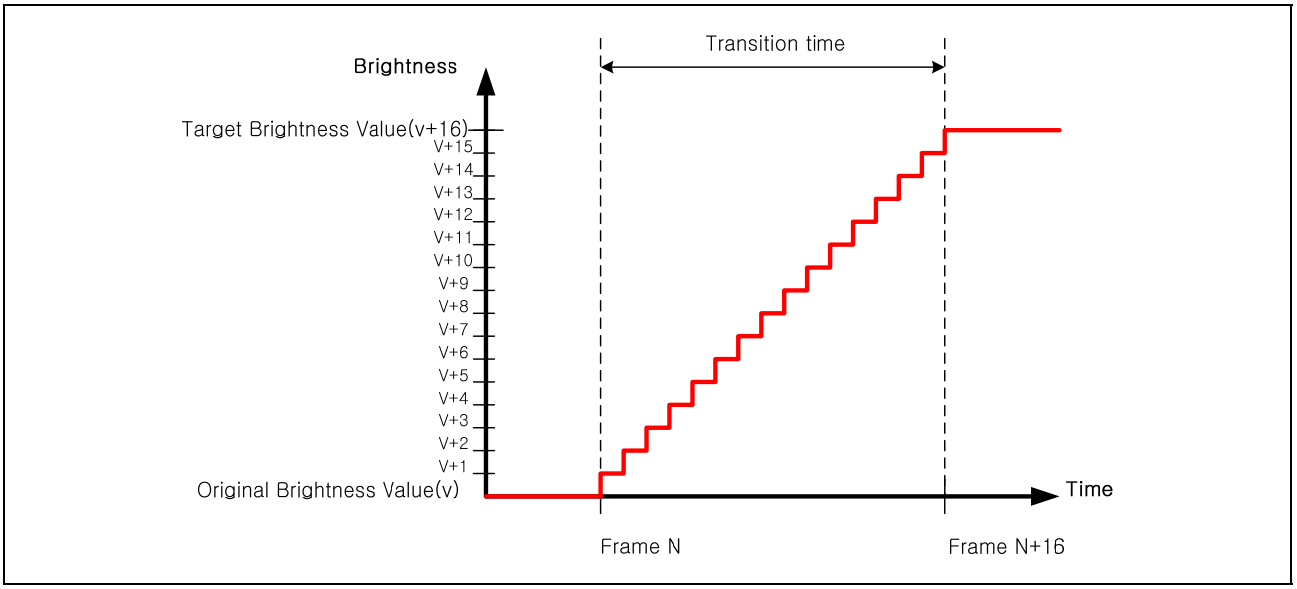


Figure 161. Example of dimming function (DT[2:0] = 000)

5.3.2.8. BL_DRV_EN

This register is used to enable the LED driver IC when the IC needs the chip enable signal. This signal is outputted to BC_CTL pad.

Table 137. BL_DRV_EN

BL_DRV_EN	State of BL_CTL PAD
0	Low
1	High

Status	Default Value
Initial	BL_DRV_EN = 1

5.3.2.9. BL_DIMM_STEP[1:0]

This register is used to select the dimming step of BC level. It is used to select the frequency of BC with BC_FRQ_SEL[6:0].

Table 138. BL_DIMM_STEP[1:0]

BL_DIMM_STEP[1:0]	Dimming Steps of BC
00	256
01	128
10	64
11	32

Status	Default Value
Initial	BL_DIMM_STEP[1:0] = 00

The BC frequency is calculated with the following formula.

$$Num.\ of\ BC/\ 1\ frame = (BC\_FRQ\_SEL + 1)\ X\ 2^{BL\_DIMM\_SETP}$$

Figure 162. Calculation formula of BC frequency

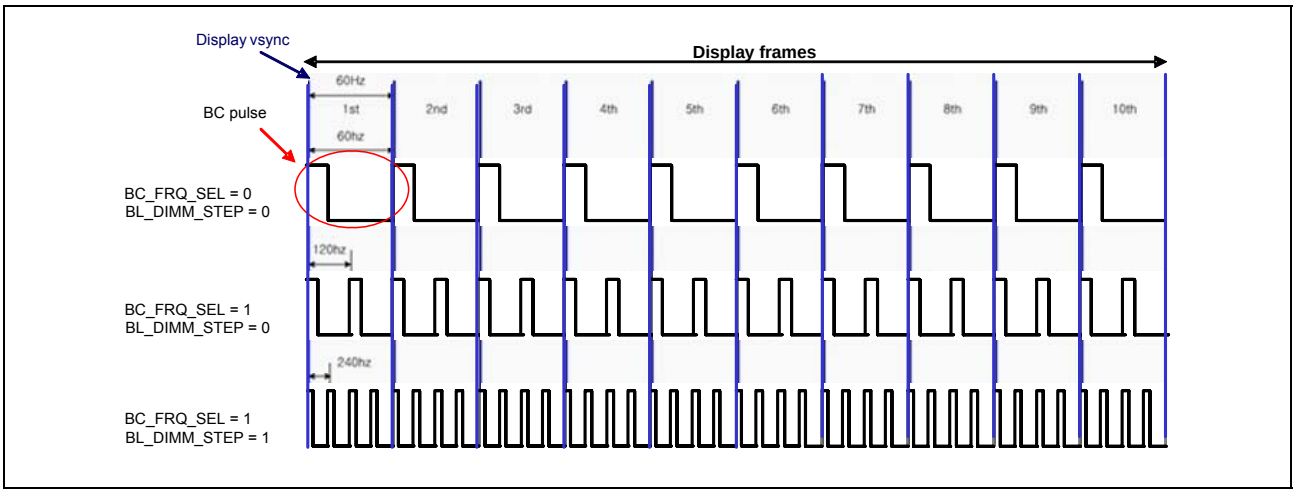


Figure 163. Example of BC frequency selection

Table 139. BC frequency

BC_FRQ_SEL[6:0]	BC Frequency [Hz]		
BL_DIMM_STEP[1:0]	00	01	10
Dimming Step No.	256	128	64
0000000	F.F. x 1	F.F. x 2	F.F. x 4
0000001	F.F. x 2	F.F. x 4	F.F. x 8
0000010	F.F. x 3	F.F. x 6	F.F. x 12
0000011	F.F. x 4	F.F. x 8	F.F. x 16
0000100	F.F. x 5	F.F. x 10	F.F. x 20
0000101	F.F. x 6	F.F. x 12	F.F. x 24
0000110	F.F. x 7	F.F. x 14	F.F. x 28
0000111	F.F. x 8	F.F. x 16	F.F. x 32
0001000	F.F. x 9	F.F. x 18	F.F. x 36
0001001	F.F. x 10	F.F. x 20	F.F. x 40
0001010	F.F. x 11	F.F. x 22	F.F. x 44
0001011	F.F. x 12	F.F. x 24	F.F. x 48
0001100	F.F. x 13	F.F. x 26	F.F. x 52
0001101	F.F. x 14	F.F. x 28	F.F. x 56
0001110	F.F. x 15	F.F. x 30	F.F. x 60
0001111	F.F. x 16	F.F. x 32	F.F. x 64
0010000	F.F. x 17	F.F. x 34	F.F. x 68
0010001	F.F. x 18	F.F. x 36	F.F. x 72
0010010	F.F. x 19	F.F. x 38	F.F. x 76
0010011	F.F. x 20	F.F. x 40	F.F. x 80
0010100	F.F. x 21	F.F. x 42	F.F. x 84
0010101	F.F. x 22	F.F. x 44	F.F. x 88
0010110	F.F. x 23	F.F. x 46	F.F. x 92
0010111	F.F. x 24	F.F. x 48	F.F. x 96
0011000	F.F. x 25	F.F. x 50	F.F. x 100
0011001	F.F. x 26	F.F. x 52	F.F. x 104
0011010	F.F. x 27	F.F. x 54	F.F. x 108
0011011	F.F. x 28	F.F. x 56	F.F. x 112
0011100	F.F. x 29	F.F. x 58	F.F. x 116
0011101	F.F. x 30	F.F. x 60	F.F. x 120
0011110	F.F. x 31	F.F. x 62	F.F. x 124
0011111	F.F. x 32	F.F. x 64	F.F. x 128
0100000	F.F. x 33	F.F. x 66	F.F. x 132
0100001	F.F. x 34	F.F. x 68	F.F. x 136
0100010	F.F. x 35	F.F. x 70	F.F. x 140
0100011	F.F. x 36	F.F. x 72	F.F. x 144
0100100	F.F. x 37	F.F. x 74	F.F. x 148
0100101	F.F. x 38	F.F. x 76	F.F. x 152
0100110	F.F. x 39	F.F. x 78	F.F. x 156
0100111	F.F. x 40	F.F. x 80	F.F. x 160
0101000	F.F. x 41	F.F. x 82	F.F. x 164
0101001	F.F. x 42	F.F. x 84	F.F. x 168
0101010	F.F. x 43	F.F. x 86	F.F. x 172
0101011	F.F. x 44	F.F. x 88	F.F. x 176
0101100	F.F. x 45	F.F. x 90	F.F. x 180
0101101	F.F. x 46	F.F. x 92	F.F. x 184
0101110	F.F. x 47	F.F. x 94	F.F. x 188
0101111	F.F. x 48	F.F. x 96	F.F. x 192
0110000	F.F. x 49	F.F. x 98	F.F. x 196
0110001	F.F. x 50	F.F. x 100	F.F. x 200
0110010	F.F. x 51	F.F. x 102	F.F. x 204
0110011	F.F. x 52	F.F. x 104	F.F. x 208
0110100	F.F. x 53	F.F. x 106	F.F. x 212
0110101	F.F. x 54	F.F. x 108	F.F. x 216
0110110	F.F. x 55	F.F. x 110	F.F. x 220
0110111	F.F. x 56	F.F. x 112	F.F. x 224
0111000	F.F. x 57	F.F. x 114	F.F. x 228
0111001	F.F. x 58	F.F. x 116	F.F. x 232
0111010	F.F. x 59	F.F. x 118	F.F. x 236
0111011	F.F. x 60	F.F. x 120	F.F. x 240
0111100	F.F. x 61	F.F. x 122	F.F. x 244
0111101	F.F. x 62	F.F. x 124	F.F. x 248
0111110	F.F. x 63	F.F. x 126	F.F. x 252
0111111	F.F. x 64	F.F. x 128	F.F. x 256

BC_FRQ_SEL[6:0]	BC Frequency [Hz]		
BL_DIMM_STEP[1:0]	00	01	10
Dimming Step No.	256	128	64
1000000	F.F. x 65	F.F. x 130	F.F. x 260
1000001	F.F. x 66	F.F. x 132	F.F. x 264
1000010	F.F. x 67	F.F. x 134	F.F. x 268
1000011	F.F. x 68	F.F. x 136	F.F. x 272
1000100	F.F. x 69	F.F. x 138	F.F. x 276
1000101	F.F. x 70	F.F. x 140	F.F. x 280
1000110	F.F. x 71	F.F. x 142	F.F. x 284
1000111	F.F. x 72	F.F. x 144	F.F. x 288
1001000	F.F. x 73	F.F. x 146	F.F. x 292
1001001	F.F. x 74	F.F. x 148	F.F. x 296
1001010	F.F. x 75	F.F. x 150	F.F. x 300
1001011	F.F. x 76	F.F. x 152	F.F. x 304
1001100	F.F. x 77	F.F. x 154	F.F. x 308
1001101	F.F. x 78	F.F. x 156	F.F. x 312
1001110	F.F. x 79	F.F. x 158	F.F. x 316
1001111	F.F. x 80	F.F. x 160	F.F. x 320
1010000	F.F. x 81	F.F. x 162	F.F. x 324
1010001	F.F. x 82	F.F. x 164	F.F. x 328
1010010	F.F. x 83	F.F. x 166	F.F. x 332
1010011	F.F. x 84	F.F. x 168	F.F. x 336
1010100	F.F. x 85	F.F. x 170	F.F. x 340
1010101	F.F. x 86	F.F. x 172	F.F. x 344
1010110	F.F. x 87	F.F. x 174	F.F. x 348
1010111	F.F. x 88	F.F. x 176	F.F. x 352
1011000	F.F. x 89	F.F. x 178	F.F. x 356
1011001	F.F. x 90	F.F. x 180	F.F. x 360
1011010	F.F. x 91	F.F. x 182	F.F. x 364
1011011	F.F. x 92	F.F. x 184	F.F. x 368
1011100	F.F. x 93	F.F. x 186	F.F. x 372
1011101	F.F. x 94	F.F. x 188	F.F. x 376
1011110	F.F. x 95	F.F. x 190	F.F. x 380
1011111	F.F. x 96	F.F. x 192	F.F. x 384
1100000	F.F. x 97	F.F. x 194	F.F. x 388
1100001	F.F. x 98	F.F. x 196	F.F. x 392
1100010	F.F. x 99	F.F. x 198	F.F. x 396
1100011	F.F. x 100	F.F. x 200	F.F. x 400
1100100	F.F. x 101	F.F. x 202	F.F. x 404
1100101	F.F. x 102	F.F. x 204	F.F. x 408
1100110	F.F. x 103	F.F. x 206	F.F. x 412
1100111	F.F. x 104	F.F. x 208	F.F. x 416
1101000	F.F. x 105	F.F. x 210	F.F. x 420
1101001	F.F. x 106	F.F. x 212	F.F. x 424
1101010	F.F. x 107	F.F. x 214	F.F. x 428
1101011	F.F. x 108	F.F. x 216	F.F. x 432
1101100	F.F. x 109	F.F. x 218	F.F. x 436
1101101	F.F. x 110	F.F. x 220	F.F. x 440
1101110	F.F. x 111	F.F. x 222	F.F. x 444
1101111	F.F. x 112	F.F. x 224	F.F. x 448
1110000	F.F. x 113	F.F. x 226	F.F. x 452
1110001	F.F. x 114	F.F. x 228	F.F. x 456
1110010	F.F. x 115	F.F. x 230	F.F. x 460
1110011	F.F. x 116	F.F. x 232	F.F. x 464
1110100	F.F. x 117	F.F. x 234	F.F. x 468
1110101	F.F. x 118	F.F. x 236	F.F. x 472
1110110	F.F. x 119	F.F. x 238	F.F. x 476
1110111	F.F. x 120	F.F. x 240	F.F. x 480
1111000	F.F. x 121	F.F. x 242	F.F. x 484
1111001	F.F. x 122	F.F. x 244	F.F. x 488
1111010	F.F. x 123	F.F. x 246	F.F. x 492
1111011	F.F. x 124	F.F. x 248	F.F. x 496
1111100	F.F. x 125	F.F. x 250	F.F. x 500
1111101	F.F. x 126	F.F. x 252	F.F. x 504
1111110	F.F. x 127	F.F. x 254	F.F. x 508
1111111	F.F. x 128	F.F. x 256	F.F. x 512

Note. F.F. means Frame Frequency.

When the display frame frequency is 60Hz, BC frequency is represented at the table below.

Table 140. Example of BC frequency selection

BC_FRQ_SEL[6:0]	BC Frequency [Hz]		
BL_DIMM_STEP[1:0]	00	01	10
Dimming Step No.	256	128	64
0000000	60	120	240
0000001	120	240	480
0000010	180	360	720
0000011	240	480	960
0000100	300	600	1200
0000101	360	720	1440
0000110	420	840	1680
0000111	480	960	1920
0001000	540	1080	2160
0001001	600	1200	2400
0001010	660	1320	2640
0001011	720	1440	2880
0001100	780	1560	3120
0001101	840	1680	3360
0001110	900	1800	3600
0001111	960	1920	3840
0010000	1020	2040	4080
0010001	1080	2160	4320
0010010	1140	2280	4560
0010011	1200	2400	4800
0010100	1260	2520	5040
0010101	1320	2640	5280
0010110	1380	2760	5520
0010111	1440	2880	5760
0011000	1500	3000	6000
0011001	1560	3120	6240
0011010	1620	3240	6480
0011011	1680	3360	6720
0011100	1740	3480	6960
0011101	1800	3600	7200
0011110	1860	3720	7440
0011111	1920	3840	7680
0100000	1980	3960	7920
0100001	2040	4080	8160
0100010	2100	4200	8400
0100011	2160	4320	8640
0100100	2220	4440	8880
0100101	2280	4560	9120
0100110	2340	4680	9360
0100111	2400	4800	9600
0101000	2460	4920	9840
0101001	2520	5040	10080
0101010	2580	5160	10320
0101011	2640	5280	10560
0101100	2700	5400	10800
0101101	2760	5520	11040
0101110	2820	5640	11280
0101111	2880	5760	11520
0110000	2940	5880	11760
0110001	3000	6000	12000
0110010	3060	6120	12240
0110011	3120	6240	12480
0110100	3180	6360	12720
0110101	3240	6480	12960
0110110	3300	6600	13200
0110111	3360	6720	13440
0111000	3420	6840	13680
0111001	3480	6960	13920
0111010	3540	7080	14160
0111011	3600	7200	14400
0111100	3660	7320	14640
0111101	3720	7440	14880
0111110	3780	7560	15120
0111111	3840	7680	15360

BC_FRQ_SEL[6:0]	BC Frequency [Hz]		
BL_DIMM_STEP[1:0]	00	01	10
Dimming Step No.	256	128	64
1000000	3900	7800	15600
1000001	3960	7920	15840
1000010	4020	8040	16080
1000011	4080	8160	16320
1000100	4140	8280	16560
1000101	4200	8400	16800
1000110	4260	8520	17040
1000111	4320	8640	17280
1001000	4380	8760	17520
1001001	4440	8880	17760
1001010	4500	9000	18000
1001011	4560	9120	18240
1001100	4620	9240	18480
1001101	4680	9360	18720
1001110	4740	9480	18960
1001111	4800	9600	19200
1010000	4860	9720	19440
1010001	4920	9840	19680
1010010	4980	9960	19920
1010011	5040	10080	20160
1010100	5100	10200	20400
1010101	5160	10320	20640
1010110	5220	10440	20880
1010111	5280	10560	21120
1011000	5340	10680	21360
1011001	5400	10800	21600
1011010	5460	10920	21840
1011011	5520	11040	22080
1011100	5580	11160	22320
1011101	5640	11280	22560
1011110	5700	11400	22800
1011111	5760	11520	23040
1100000	5820	11640	23280
1100001	5880	11760	23520
1100010	5940	11880	23760
1100011	6000	12000	24000
1100100	6060	12120	24240
1100101	6120	12240	24480
1100110	6180	12360	24720
1100111	6240	12480	24960
1101000	6300	12600	25200
1101001	6360	12720	25440
1101010	6420	12840	25680
1101011	6480	12960	25920
1101100	6540	13080	26160
1101101	6600	13200	26400
1101110	6660	13320	26640
1101111	6720	13440	26880
1110000	6780	13560	27120
1110001	6840	13680	27360
1110010	6900	13800	27600
1110011	6960	13920	27840
1110100	7020	14040	28080
1110101	7080	14160	28320
1110110	7140	14280	28560
1110111	7200	14400	28800
1111000	7260	14520	29040
1111001	7320	14640	29280
1111010	7380	14760	29520
1111011	7440	14880	29760
1111100	7500	15000	30000
1111101	7560	15120	30240
1111110	7620	15240	30480
1111111	7680	15360	30720

5.3.3. MTPCTL : MTP Control Command (D0h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MTPCTL	R/W	0	1	1	0	1	0	0	0	0	D0h
1st para		1	0	0	0	0	ID_ SEL	MTP_ SEL	MTP_ MODE	MTP_ EX	
2nd para		1	0	0	0	0	0	MTP_ ERB	MTP_ LOAD	MTP_ WRB	

5.3.3.1. ID_SEL/ MTP_SEL/ MTP_MODE/ MTP_EX

ID_SEL: Select the ID register.

Table 141. ID_SEL

ID_SEL	ID1/ID2/ID3 Data
0	ID1/ID2/ID3 Register
1	MTP data

MTP_SEL: Select the VCOMH voltage setting register.

Table 142. MTP_SEL

MTP_SEL	VCOMH Control Data
0	VCMOC/VMLOC/GVDDOC Register
1	MTP data

MTP_MODE: Set the 2nd booster operating condition. When MTP_MODE = 0, the 2nd booster operates as a user-specified condition. VGH/VGL voltages are generated as a designated level by BT2-0 setting. If MTP_MODE = 1, available BT2-0 settings are limited only '010' & '101'.

Table 143. MTP_MODE

MTP_MODE	MTP operation mode
0	All BT2-0 settings are available (Normal operating condition)
1	Setting of BT2-0 is limited. (An MTP-programming / erasing condition)

Note. Do not execute MTP programming / erasing operation when MTP_MODE = 0.

MTP_EX: Select MTP power supply source.

When MTP_EX = 0, Internally generated VGH voltage is used as a MTP-programming / erasing potential.

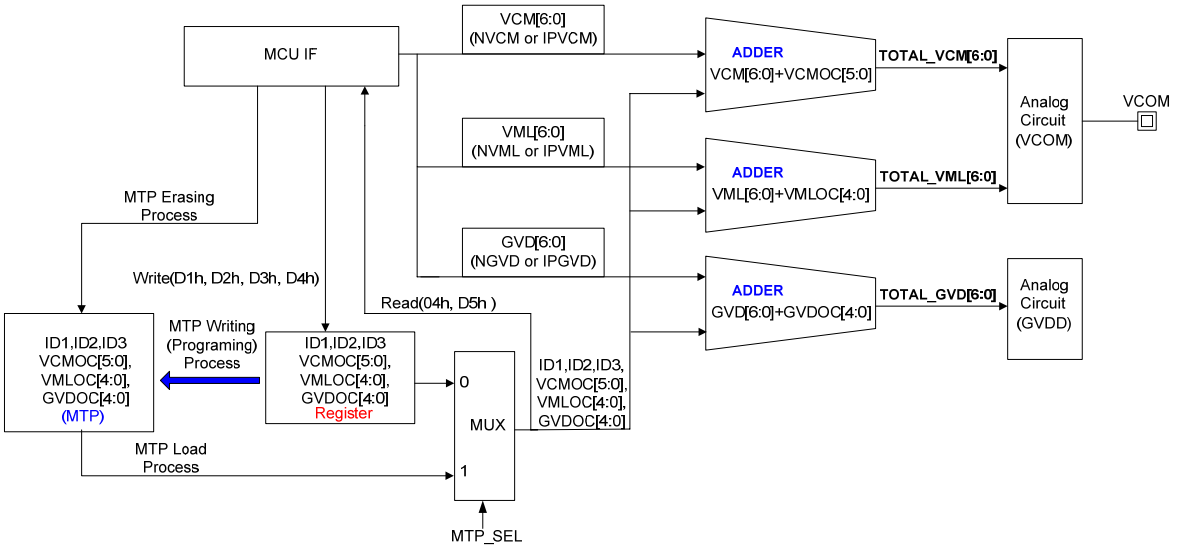
If MTP_EX = 1, External power should be applied for programming / erasing MTP via VGH pad.

Table 144. MTP_EX

MTP_EX	Erase / Initial / Program supply
0	Used internally generated VGH
1	Needed external power supply

Note. MTP_EX register is valid only in case that MTP_MODE = 1. Do not access MTP_EX register when MTP_MODE = 0.

Status	Default Value
Initial	ID_SEL = 1 MTP_SEL = 1 MTP_MODE = 0 MTP_EX = 0



5.3.3.2. MTP_ERB/ MTP_LOAD/ MTP_WRB

MTP_ERB: Enable bit for MTP initialization or erasure.

When MTP_ERB = 0, MTP initialization or erasure is enabled.

MTP_LOAD: When MTP_LOAD is High, MTP data is loaded into an internal register.

MTP_WRB: MTP Write enable bit. If MTP cell is to be written, set MTP_WRB = 0

Status	Default Value
Initial	MTP_ERB = 1 MTP_LOAD = 0 MTP_WRB = 1

5.3.4. WRVCMOC : Set VCOM Offset Control (D1h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRVCM OC	R/W	0	1	1	0	1	0	0	0	1	D1h
1st para		1	0	0	VCM OC5	VCM OC4	VCM OC3	VCM OC2	VCM OC1	VCM OC0	

5.3.4.1. VCOMC[5:0]

VCMOC5-0 contains VCM Offset data. This MTP data and VCM register determine VCOMH level.

TOTAL_VCM[6:0] = VCM[6:0](NVCM or IPVCM) + VCMOC5-0

Table 145. VCOMC[5:0]

VCMOC5-0	VCM_OFFSET	VCMOC5-0	VCM_OFFSET
000000	0	100000	0
000001	+1	100001	-1
000010	+2	100010	-2
000011	+3	100011	-3
000100	+4	100100	-4
000101	+5	100101	-5
000110	+6	100110	-6
000111	+7	100111	-7
…	…	…	…
…	…	…	…
011010	+25	111010	-26
011011	+26	111011	-27
011100	+28	111100	-28
011101	+29	111101	-29
011110	+30	111110	-30
011111	+31	111111	-31

For example, if VCM[6:0] = 0001011 and VCMOC5-0 = 100001 are selected, then VCM_OFFSET is “-1,” and therefore TOTAL_VCM is “0001010,” which results in VCOMH voltage = 2.6969 from NVCM6-0/IPVCM6-0 table.

Note1. TOTAL_VCM [6:0] cannot be set to the value above “1111111” or below “0000000,” that is, 128 ≥ VCM[6:0] + VCMOC5-0 ≥ 0.

Note2. TOTAL_VCM[6:0] is VCM[6:0] + VCM_OFFSET_MTP[5:0] when MTP_SEL=1 and is VCM[6:0] + VCMOC5-0 when MTP_SEL= 0.

Status	Default Value
Initial	VCMOC[5:0] = 000000

5.3.5. WRVMLOC : Set VCOML Offset Control (D2h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRVMLOC	R/W	0	1	1	0	1	0	0	1	0	D2h
1st para	R/W	1	0	0	0	VMLOC4	VMLOC3	VMLOC2	VMLOC1	VMLOC0	

5.3.5.1. VMLOC[4:0]

VMLOC4-0 contain VCOM amplitude Offset data. This MTP data and VML register determine VCOML amplitude.

TOTAL_VML[6:0] = VML[6:0](NVML or IPVML) + VMLOC4-0.

Table 146. VMLOC[4:0]

VMLOC4-0	VML_OFFSET	VMLOC4-0	VML_OFFSET
00000	0	10000	0
00001	+1	10001	-1
00010	+2	10010	-2
00011	+3	10011	-3
00100	+4	10100	-4
00101	+5	10101	-5
00110	+6	10110	-6
00111	+7	10111	-7
01000	+8	11000	-8
01001	+9	11001	-9
01010	+10	11010	-10
01011	+11	11011	-11
01100	+12	11100	-12
01101	+13	11101	-13
01110	+14	11110	-14
01111	+15	11111	-15

For example, if VML[6:0] = 0010101 and VMLOC4-0 = 10001 are selected, then VML_OFFSET is “-1,” and therefore TOTAL_VML is “0010100,” which results in VCOM amplitude voltage = 3.4724V from NVML6-0/IPVML6-0 table.

Note1. TOTAL_VML[6:0] cannot be set to the value above “1111111” or below “0000000,” that is, 127 ≥ VML[6:0] + VMLOC4-0 ≥ 0.

Note2. TOTAL_VML[6:0] is VML[6:0] + VML_OFFSET_MTP[4:0] when MTP_SEL=1 and is VML[6:0] + VMLOC4-0 when MTP_SEL=0

Status	Default Value
Initial	VMLOC[4:0] = 00000

5.3.6. WRGVDOC : Set GVDD Offset Control (D3h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRGVDOC	R/W	0	1	1	0	1	0	0	1	1	D3h
1st param		1	0	0	0	GVDOC4	GVDOC3	GVDOC2	GVDOC1	GVDOC0	

5.3.6.1. GVDOC[4:0]

GVDOC4-0 contains GVD Offset data. This MTP data and GVD register determine GVDD level.

TOTAL_GVD[6:0] = GVD[6:0](NGVD or IPGVD) + GVDOC4-0.

Table 147. GVDOC[4:0]

GVDOC4-0	GVD_OFFSET	GVDOC4-0	GVD_OFFSET
00000	0	10000	0
00001	+1	10001	-1
00010	+2	10010	-2
00011	+3	10011	-3
00100	+4	10100	-4
00101	+5	10101	-5
00110	+6	10110	-6
00111	+7	10111	-7
01000	+8	11000	-8
01001	+9	11001	-9
01010	+10	11010	-10
01011	+11	11011	-11
01100	+12	11100	-12
01101	+13	11101	-13
01110	+14	11110	-14
01111	+15	11111	-15

For example, if GVD[6:0] = 0001011 and GVCOC4-0 = 10001 are selected, then MTP_OFFSET is “-1,” and therefore TOTAL_GVD is “0001010,” which results in GVDD voltage = 2.6969V from NGVD6-0/IPGVD6-0 table.

Note1. TOTAL_GVD[6:0] cannot be set to the value above “1111111” or below “0000000,” that is, 127 ≥ GVD[6:0] + GVDOC4-0 ≥ 0.

Note2. TOTAL_GVD[6:0] is GVD[6:0] + GVD_OFFSET_MTP[4:0] when MTP_SEL=1 and is GVD[6:0]+ GVDOC4-0 when MTP_SEL=0.

Status	Default Value
Initial	GVDOC[4:0] = 00000

5.3.7. WRID : ID Definition (D4h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRID	R/W	0	1	1	0	1	0	1	0	0	D4h
1st para		1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
2nd para		1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
3rd para		1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	

5.3.7.1. ID1/ ID2/ ID3

ID1: LCD module/driver manufacturers ID (specified by user)

ID2: LCD module/driver version ID(specified by module supplier)

ID3 : Project ID(specified by handset company)

Status	Default Value
Intial	ID1 = 00h ID2 = 00h ID3 = 00h

5.3.8. RDOFFSETC : Read Offset Control (D5h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDOFFSETC	R	0	1	1	0	1	0	1	0	1	D5h
Dummy Read		1	X	X	X	X	X	X	X	X	X
1st para		1	0	0	VCMOC_MTP5	VCMOC_MTP4	VCMOC_MTP3	VCMOC_MTP2	VCMOC_MTP1	VCMOC_MTP0	
2nd para		1	0	0	0	VMLOC_MTP4	VMLOC_MTP3	VMLOC_MTP2	VMLOC_MTP1	VMLOC_MTP0	
3rd para		1	0	0	0	GVDOC_MTP4	GVDOC_MTP3	GVDOC_MTP2	GVDOC_MTP1	GVDOC_MTP0	

Note: "X" denotes "Don't care"

5.3.8.1. VCMOC_MTP/ VMLOC_MTP/ GVDOC_MTP

VCMOC_MTP: Read VCMOC Values from MTP

VMLOC_MTP: Read VMLOC Values from MTP

GVDOC_MTP: Read GVDOC Values from MTP

Status	Default Value
Initial	MTP[39:24]

5.3.9. MDDICTL1 : MDDI Control 1 (E0h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MDDICTL1	R/W	0	1	1	1	0	0	0	0	0	E0h
1st para		1	0	0	0	0	0	0	MDDI_SLP	VWAKE_EN	

5.3.9.1. MDDI_SLP

MDDI_SLP: When MDDI_SLP is high, MDDI operating state is STOP state.

To release STOP state, input reset signal.

5.3.9.2. VWAKE_EN

VWAKE_EN: When VWAKE_EN is 1, client initiated wake-up is enabled

Status	Default Value
Initial	MDDI_SLP = 0, VWAKE_EN = 0

5.3.10. MDDILIK : MDDI Link Wake-Up Start Position (E1h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MDDILIK	R/W	0	1	1	1	0	0	0	0	1	E1h
1st para		1	WKL9	WKL8	WKL7	WKL6	WKL5	WKL4	WKL3	WKL2	
2nd para		1	WKL1	WKL0	WKF3	WKF2	WKF1	WKF0	0	0	

5.3.10.1. WKL[9:0]

WKL[9:0]: The register for defining at which number of line the client-initiaed wakeup would start. If WKL is updated to '000h', client-initiated wakeup starts automatically at the first line of display during scanning. The range of WKL is from '000h' to '3FFh'.

5.3.10.2. WKF[3:0]

WKF[3:0]: The register for defining after which number of frame the client-initiated wakeup states at the starts of next frame, and if '1111b', wakeup starts after 16th frame.

Setting of WKF and WKL works together for client-initiated wakeup.
For example, if WKF is '0010b' and WKL is '001h', wakeup starts at the second line of third frame.

Status	Default Value
Initial	WKL[9:0] = 00_0000_0000 WKF[3:0] = 0000

5.3.11. WRPWD : MTP Control Test Key (F0h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRPWD	R/W	0	1	1	1	1	0	0	0	0	F0h
1st para		1	TEST 7	TEST 6	TEST 5	TEST 4	TEST 3	TEST 2	TEST 1	TEST 0	

5.3.11.1. TEST[7:0]

TEST7-0: MTP Function Protection TEST_KEY. When Test [7:0]=5Ah, MTP_WRB and MTP_ERB are valid.

Status	Default Value
Initial	TEST[7:0] = 30h

5.3.12. DISCTL : Display Control Register (F2h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISCTL	R/W	0	1	1	1	1	0	0	1	0	F2h
1st para		1	0	0	0	NRTN 4	NRTN 3	NRTN 2	NRTN 1	NRTN 0	
2nd para		1	0	0	0	IPRTN 4	IPRTN 3	IPRTN 2	IPRTN 1	IPRTN 0	
3rd para		1	0	0	0	0	IPINV	IINV	PINV	NINV	
4th para		1	NVBP 7	NVBP 6	NVBP 5	NVBP 4	NVBP 3	NVBP 2	NVBP 1	NVBP 0	
5th para		1	NVFP 7	NVFP 6	NVFP 5	NVFP 4	NVFP 3	NVFP 2	NVFP 1	NVFP 0	
6th para		1	IPVBP	IPVBP	IPVBP	IPVBP	IPVBP	IPVBP	IPVBP	IPVBP	
7th para		1	IPVFP 7	IPVFP 6	IPVFP 5	IPVFP 4	IPVFP 3	IPVFP 2	IPVFP 1	IPVFP 0	
8th para		1	0	HBP 6	HBP 5	HBP 4	HBP 3	HBP 2	HBP 1	HBP 0	
9th para		1	0	0	0	0	0	SM	GS	REV	
10th para		1	0	0	0	NCRT N4	NCRT N3	NCRT N2	NCRT N1	NCRT N0	
11th para		1	0	0	0	IPCRT N4	IPCRT N3	IPCRT N2	IPCRT N1	IPCRT N0	

5.3.12.1. NRTN[4:0] / IPRTN[4:0]

Set the 1H period (1 raster-row) register. NRTN is valid in Normal mode, and IPRTN is applied in Idle Partial mode.

Table 148. NRTN[4:0]/IPRTN[4:0]

NRTN4/IPRTN4	NRTN3/IPRTN3	NRTN2/IPRTN2	NRTN1/IPRTN1	NRTN0/IPRTN0	1 Horizontal clock cycle (CL1)
0	0	0	0	0	Setting Disable
0	0	0	0	1	Setting Disable
0	0	0	1	0	Setting Disable
0	0	0	1	1	Setting Disable
0	0	1	0	0	Setting Disable
0	0	1	0	1	Setting Disable
0	0	1	1	0	Setting Disable
0	0	1	1	1	Setting Disable
0	1	0	0	0	8 INCLK
0	1	0	0	1	9 INCLK
0	1	0	1	0	10 INCLK
0	1	0	1	1	11 INCLK
0	1	1	0	0	12 INCLK
0	1	1	0	1	13 INCLK
0	1	1	1	0	14 INCLK
0	1	1	1	1	15 INCLK
1	0	0	0	0	16 INCLK
1	0	0	0	1	17 INCLK
1	0	0	1	0	18 INCLK
1	0	0	1	1	19 INCLK
1	0	1	0	0	20 INCLK
1	0	1	0	1	21 INCLK
1	0	1	1	0	22 INCLK
1	0	1	1	1	23 INCLK
1	1	0	0	0	24 INCLK
1	1	0	0	1	25 INCLK
1	1	0	1	0	26 INCLK
1	1	0	1	1	27 INCLK
1	1	1	0	0	28 INCLK
1	1	1	0	1	29 INCLK
1	1	1	1	0	30 INCLK
1	1	1	1	1	31 INCLK

Note1. RTN x CRTN must bigger than 260.

- 24/ 18/ 16-bit RGB-IF : DOTCLK >= 260
- 9/ 8-bit RGB-IF : DOTCLK >= 260 x 3

Note2. INCLK : Internal clock (= OSC_CK x CRTN)

Note3. IPNO, IPSDT, VCIRA, VCIR register values must be smaller than the half of IPRTN values.

NNO, NSDT, VCIRA, VCIR register values must be smaller than the half of NRTN values.

Status	Default Value
Initial	NRTN[4:0] = 10110 IPRTN[4:0] = 10110

5.3.12.2. IPINV/IINV/PINV/INV

Display inversion mode control register.

IPINV : Inversion setting on partial idle mode (Partial mode on / Idle mode on)

IINV : Inversion setting on Idle mode (Idle mode on)

PINV : Inversion setting on partial mode (Partial mode on)

NINV : Inversion setting on full color normal mode (Normal mode on)

Table 149. IPINV/IINV/PINV/NINV

IPINV/IINV/PINV/NINV	Inversion
0	Frame inversion
1	Line inversion

Status	Default Value
Initial	IPINV = 0 IINV = 0 PINV = 1 NINV = 1

5.3.12.3. NVBP[7:0]/ IPVBP[7:0]/ NVFP[7:0]/ IPVFP[7:0]

Control vertical back and front porch in MCU I/F or RGB I/F mode

NVBP/ IPVBP : The number of lines for the back porch of VS(Vertical Sync) register.

IPVBP is applied in Idle Partial mode

Table 150. NVBP[7:0]/IPVBP[7:0]

NVBP[7:0] / IPVBP[7:0]	No. of clock cycle of HS (horizontal Sync)
00d	Setting Disable
01d	Setting Disable
02d	2
03d	3
04d	4
05d	5
. . .	. . .
254d	254
255d	255

Note 1. When BCTRL does ON, establish VBP and VFP by same value.

NVFP/ IPVFP: The number of lines for the front porch of VS. NVFP/IPVFP must be bigger than 2.

IPVFP is applied in Idle Partial mode.

Table 151. NVFP[7:0]/IPVFP[7:0]

NVFP[7:0] / IPVFP[7:0]	No. of clock cycle of HS
00d	Setting Disable
01d	Setting Disable
02d	Setting Disable
03d	3
04d	4
05d	5
. . .	. . .
254d	254
255d	255

Status	Default Value
Initial	NVBP[7:0] = 08h IPVBP[7:0] = 08h NVFP[7:0] = 08h IPVFP[7:0] = 08h

5.3.12.4. HBP[6:0]

The number of internal clocks for TE's Horizontal timing high width

Table 152. HBP[6:0]

HBP[6:0]	No. of clock cycle of INCLK
00d	2
01d	3
02d	4
03d	5
. . .	. . .
26d	28
27d	29
28d	30
29d	Don't use
..	Don't use
127d	Don't use

Status	Default Value
Initial	HBP[6:0] = 01_0000

Note : HBP must be set lower than RTN -2.

5.3.12.5. SM/ GS/ REV

SM : Select the division drive method of the gate driver. When SM=0, even/odd division is selected; SM =1, upper/lower division drive is selected by (total gate line)/2 and (total gate line)/2. Various connections between TFT panel and the IC can be supported with the combination of SM and GS bit.

GS : Set the order of Gate Clock generation. When GS = 0, the order of GATE_ON is from G1 to G432, and then GS = 1, from G432 to G1.

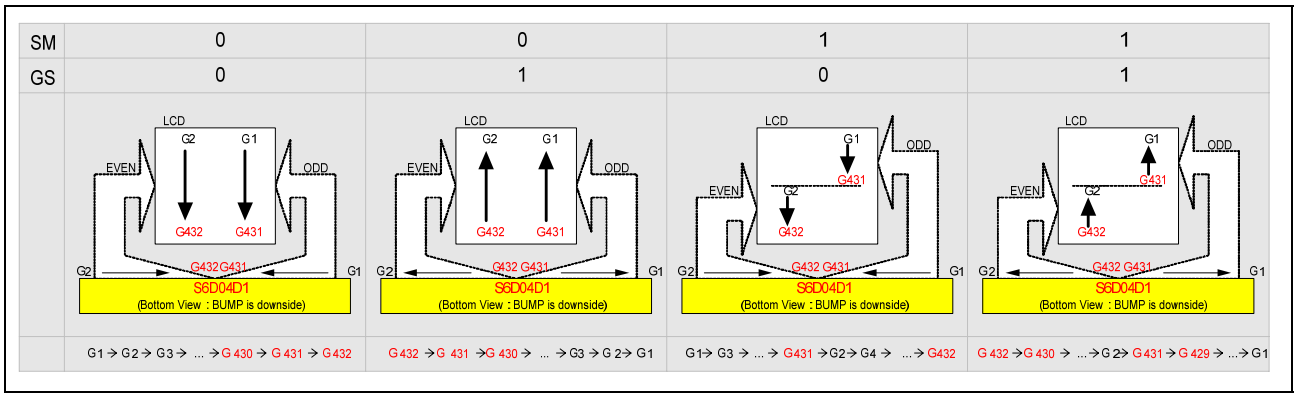


Figure 164. Gate clock generation order selection using GS and SM

REV: Display all character and graphics display sections with reversal when REV=1.

Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels.

Table 153. REV

REV	GRAM Data	Display Area	
		Positive	Negative
0	8'b000000 : 8'b111111	V255 : V0	V0 : V255
1	8'b000000 : 8'b111111	V0 : V255	V255 : V0

Status	Default Value
Initial	SM = 0 GS = 0 REV = 0

5.3.12.6. NCRTN[4:0] / IPCRTN[4:0]

Set the 1 raster-row. IPCRTN is applied in Idle Partial mode.

Table 154. NCRTN[4:0] / IPCRTN[4:0]

NCRTN4/ IPCRTN4	NCRTN3/ IPCRTN3	NCRTN2/ IPCRTN2	NCRTN1/ IPCRTN1	NCRTN0/ IPCRTN0	INCLK
0	0	0	0	0	Setting Disable
0	0	0	0	1	Setting Disable
0	0	0	1	0	Setting Disable
0	0	0	1	1	Setting Disable
0	0	1	0	0	Setting Disable
0	0	1	0	1	Setting Disable
0	0	1	1	0	Setting Disable
0	0	1	1	1	Setting Disable
0	1	0	0	0	8 OSC_CLK
0	1	0	0	1	9 OSC_CLK
0	1	0	1	0	10 OSC_CLK
0	1	0	1	1	11 OSC_CLK
0	1	1	0	0	12 OSC_CLK
0	1	1	0	1	13 OSC_CLK
0	1	1	1	0	14 OSC_CLK
0	1	1	1	1	15 OSC_CLK
1	0	0	0	0	16 OSC_CLK
1	0	0	0	1	17 OSC_CLK
1	0	0	1	0	18 OSC_CLK
1	0	0	1	1	19 OSC_CLK
1	0	1	0	0	20 OSC_CLK
1	0	1	0	1	21 OSC_CLK
1	0	1	1	0	22 OSC_CLK
1	0	1	1	1	23 OSC_CLK
1	1	0	0	0	24 OSC_CLK
1	1	0	0	1	25 OSC_CLK
1	1	0	1	0	26 OSC_CLK
1	1	0	1	1	27 OSC_CLK
1	1	1	0	0	28 OSC_CLK
1	1	1	0	1	29 OSC_CLK
1	1	1	1	0	30 OSC_CLK
1	1	1	1	1	31 OSC_CLK

Note. RTN x CRTN must be bigger than 260.

Status	Default Value
Initial	NCRTN[4:0] = 10110 IPCRTN[4:0] = 10110

5.3.13. PWRCTL : Power Control Register (F3h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWRCTL	R/W	0	1	1	1	1	0	0	1	1	F3h
1st para		1	APON	GON	AON	PON3	PON2	PON1	PON	VCI1_EN	
2nd para		1	0	0	NDC31	NDC30	NDC21	NDC20	NDC11	NDC10	
3rd para		1	0	0	IPDC31	IPDC30	IPDC21	IPDC20	IPDC11	IPDC10	
4th para		1	0	0	0	0	VC3	VC2	VC1	VC0	
5th para		1	0	IPBT2	IPBT1	IPBT0	0	NBT2	NBT1	NBT0	
6th para		1	0	GVD6	GVD5	GVD4	GVD3	GVD2	GVD1	GVD0	
7th para		1	0	IPGVD6	IPGVD5	IPGVD4	IPGVD3	IPGVD2	IPGVD1	IPGVD0	
8th para		1	0	0	VGH_FLAG_EN	AB_VCI1	NAB2A_G	IPAB2A_G	NAB2A	IPAB2A	

5.3.13.1. APON

APON: This is an automatic-boosting-operation-starting bit for the booster circuits. In case of APON=0, the automatic boosting sequence starter is halted and the booster circuits are operated independently by PON, PON1, PON2 and PON3 bits. In case of APON=1, booster circuits are operated automatically and sequentially. For further information about timing, please refer to the Section 4.1.6, 4.1.7

Status	Default Value
Initial	APON = 1

5.3.13.2. GON/AON/PON3/PON2/PON1/PON/VCI1_EN

GON: Gate on/off control bit. All gate outputs are set to be VSS level when PON2 = 0.

When PON2 = 1 and GON = 1, gate driver is working: G1 to G432 output is either VGH or VGL level.

See the Instruction set-up flow for further description on the display on/off flow.

Table 155. GON

GON	Gate Output	
0	PON2 = 0	All gates goes to VSS
	PON2 = 1	All gates goes to VGL
1	Gate on(VGH / VGL)	

AON: This is an operation-starting bit for GVDD/VCOMH/VCOML amplifiers. In case of AON = 0, the amplifier circuits are stopped. On the other hand, the operation of the amplifiers is getting started when AON = 1. For further information about timing for adjusting to AON= 1, refer to the Section 4.1.6, 4.1.7

PON3: This is an operation-starting bit for the booster circuit 3(VCL). In case of PON3 = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the PON3= 1, please refer to the Section 4.1.6, 4.1.7

PON2: This is an operation-starting bit for the booster circuit 2(VGL). In case of PON2 = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the PON2= 1, please refer to the Section 4.1.6, 4.1.7

PON1: This is an operation-starting bit for the booster circuit 2(VGH). In case of PON1 = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the PON1= 1, please refer to the Section 4.1.6, 4.1..7

PON: This is an operation-starting bit for the booster circuit1. In case of PON = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the PON = 1, please refer to the Section 4.1.6, 4.1.7

VCI1_EN: Internal VCI1 generation amplifier operation control bit. When VCI1_EN=0, VCI1 voltage is not generated.

Status	Default Value
Initial	GON = 0 AON = 0 PON3 = 0 PON2 =0 PON1 = 0 PON = 0 VCI1_EN = 0

5.3.13.3. NDC3/IPNDC3/NDC2/IPNDC2/NDC1/IPDC1

NDC31-30/ IPNDC31-30: The operating frequency in the booster circuit 3 is selected.

IPNDC3 is applied in Idle Partial mode.

Table 156. NDC3[1:0]/ IPNDC3[1:0]

NDC31/ IPDC	NDC30/ IPDC	Internal Operation (synchronized with internal clock)
		f(CL1) : f(DCCLK3)
0	0	1:4
0	1	1:2
1	0	1:1
1	1	Setting disabled

Note. DCCLK3 is pumping clock for booster circuit3

NDC21-20/ IPDC21-20: The operating frequency in the booster circuit 2 is selected.

IPNDC2 is applied in Idle Partial mode.

Table 157. NDC2[1:0]/ IPNDC2[1:0]

NDC21/ IPDC21	NDC20/ IPDC20	Internal Operation (synchronized with internal clock)
		f(CL1) : f(DCCLK2)
0	0	1:2
0	1	1:1
1	0	1:0.5
1	1	1:0.25

Note. DCCLK2 is pumping clock for booster circuit2

NDC11-10/IPDC11-10: The operating frequency in the booster circuit1 is selected. When the boosting operating frequency is high, the driving ability of the booster circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

IPNDC1 is applied in Idle Partial mode.

Table 158. NDC2[1:0]/ IPNDC2[1:0]

NDC11/ IPDC11	NDC10 IPDC11	Internal Operation (synchronized with internal clock)
		f(CL1) : f(DCCLK1)
0	0	1:4
0	1	1:2
1	0	1:1
1	1	Setting disabled

Note. DCCLK1 is pumping clock for booster circuit1. f(1H) is horizontal frequency (1 raster-row)

Status	Default Value
Initial	NDC3[1 :0] = 10, NDC2[1 :0] = 10, NDC1[1 :0] = 10 IPDC3[1 :0] = 10,IPDC2[1 :0] = 10, IPDC1[1 :0] = 10

5.3.13.4. VC[3:0]

VC3-0 : Set the VCI1 voltage. These bits set the VCI1 voltage up to 3V as the nominal output (upper limit value may depend on VCI voltage)

Table 159. VC[3:0]

VC[3]	VC[2]	VC[1]	VC[0]	VCI1
0	0	0	0	Don't use
0	0	0	1	1.75
0	0	1	0	2.07
0	0	1	1	2.16
0	1	0	0	2.25
0	1	0	1	2.34
0	1	1	0	2.43
0	1	1	1	2.52
1	0	0	0	2.58
1	0	0	1	2.64
1	0	1	0	2.70
1	0	1	1	2.76
1	1	0	0	2.82
1	1	0	1	2.88
1	1	1	0	2.94
1	1	1	1	3

Note. Do not set any higher VCI1 level than VCI -0.15V.

Status	Default Value
Initial	VC[3:0] = 0001

5.3.13.5. NBT[2:0]/ IPBT[2:0]

NBT/ IPBT : The output factor of booster is switched. Adjust scale factor of the booster circuit by the voltage used. When the boosting operating frequency is high, the driving ability of the booster circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

IPBT is applied in Idle Partial mode.

Table 160. NBT[2:0]/IPBT[2:0]

IPBT1/NBT2	IPBT1/NBT1	IPBP0/NBT0	VGH	VGL	Notes*	
0	0	0	Setting disabled			
0	0	1	Setting disabled			
0	1	0	6 X VCI1	-3X VCI1	16.5V	-8.25V
0	1	1	6 X VCI1	-4X VCI1	16.5V	-11V
1	0	0	6 X VCI1	-5X VCI1	16.5V	-13.75V
1	0	1	7 X VCI1	-4X VCI1	19.25V	-11V
1	1	0	7 X VCI1	-5X VCI1	19.25V	-13.75V
1	1	1	Setting disabled			

Note. The values in table above are example of nominal upper-limit by register setting when VCI1=2.75V.

Do not set any higher VGH level than 16.5V. Do not set | VGH – VGL | voltage difference over 30.0V.

Status	Default Value
Initial	NBT[2:0] = 010, IPBT[2:0] = 010

5.3.13.6. NGVD[6:0]/IPGVD[6:0]

NGVD6-0: Set the amplifying factor of the GVDD voltage on Normal Mode (the voltage for the Gamma voltage). It allows ranging from 2.5V to 5.0V.

Table 161. NGVD[6:0]

NGVD6-0	GVDD Voltage	NGVD6-0	GVDD Voltage	NGVD6-0	GVDD Voltage	NGVD6-0	GVDD Voltage
0000000	2.5000	0100000	3.1299	1000000	3.7598	1100000	4.3898
0000001	2.5197	0100001	3.1496	1000001	3.7795	1100001	4.4094
0000010	2.5394	0100010	3.1693	1000010	3.7992	1100010	4.4291
0000011	2.5591	0100011	3.1890	1000011	3.8189	1100011	4.4488
0000100	2.5787	0100100	3.2087	1000100	3.8386	1100100	4.4685
0000101	2.5984	0100101	3.2283	1000101	3.8583	1100101	4.4882
0000110	2.6181	0100110	3.2480	1000110	3.8780	1100110	4.5079
0000111	2.6378	0100111	3.2677	1000111	3.8976	1100111	4.5276
0001000	2.6575	0101000	3.2874	1001000	3.9173	1101000	4.5472
0001001	2.6772	0101001	3.3071	1001001	3.9370	1101001	4.5669
0001010	2.6969	0101010	3.3268	1001010	3.9567	1101010	4.5866
0001011	2.7165	0101011	3.3465	1001011	3.9764	1101011	4.6063
0001100	2.7362	0101100	3.3661	1001100	3.9961	1101100	4.6260
0001101	2.7559	0101101	3.3858	1001101	4.0157	1101101	4.6457
0001110	2.7756	0101110	3.4055	1001110	4.0354	1101110	4.6654
0001111	2.7953	0101111	3.4252	1001111	4.0551	1101111	4.6850
0010000	2.8150	0110000	3.4449	1010000	4.0748	1110000	4.7047
0010001	2.8346	0110001	3.4646	1010001	4.0945	1110001	4.7244
0010010	2.8543	0110010	3.4843	1010010	4.1142	1110010	4.7441
0010011	2.8740	0110011	3.5039	1010011	4.1339	1110011	4.7638
0010100	2.8937	0110100	3.5236	1010100	4.1535	1110100	4.7835
0010101	2.9134	0110101	3.5433	1010101	4.1732	1110101	4.8031
0010110	2.9331	0110110	3.5630	1010110	4.1929	1110110	4.8228
0010111	2.9528	0110111	3.5827	1010111	4.2126	1110111	4.8425
0011000	2.9724	0111000	3.6024	1011000	4.2323	1111000	4.8622
0011001	2.9921	0111001	3.6220	1011001	4.2520	1111001	4.8819
0011010	3.0118	0111010	3.6417	1011010	4.2717	1111010	4.9016
0011011	3.0315	0111011	3.6614	1011011	4.2913	1111011	4.9213
0011100	3.0512	0111100	3.6811	1011100	4.3110	1111100	4.9409
0011101	3.0709	0111101	3.7008	1011101	4.3307	1111101	4.9606
0011110	3.0906	0111110	3.7205	1011110	4.3504	1111110	4.9803
0011111	3.1102	0111111	3.7402	1011111	4.3701	1111111	5.0000

Note. Do not set any higher GVDD level than AVDD-0.3V

IPGVD6-0: Set the amplifying factor of the GVDD voltage on partial idle mode.

Table 162. IPGVD[6:0]

IPGVD6-0	GVDD Voltage	IPGVD6-0	GVDD Voltage	IPGVD6-0	GVDD Voltage	IPGVD6-0	GVDD Voltage
0000000	2.5000	0100000	3.1299	1000000	3.7598	1100000	4.3898
0000001	2.5197	0100001	3.1496	1000001	3.7795	1100001	4.4094
0000010	2.5394	0100010	3.1693	1000010	3.7992	1100010	4.4291
0000011	2.5591	0100011	3.1890	1000011	3.8189	1100011	4.4488
0000100	2.5787	0100100	3.2087	1000100	3.8386	1100100	4.4685
0000101	2.5984	0100101	3.2283	1000101	3.8583	1100101	4.4882
0000110	2.6181	0100110	3.2480	1000110	3.8780	1100110	4.5079
0000111	2.6378	0100111	3.2677	1000111	3.8976	1100111	4.5276
0001000	2.6575	0101000	3.2874	1001000	3.9173	1101000	4.5472
0001001	2.6772	0101001	3.3071	1001001	3.9370	1101001	4.5669
0001010	2.6969	0101010	3.3268	1001010	3.9567	1101010	4.5866
0001011	2.7165	0101011	3.3465	1001011	3.9764	1101011	4.6063
0001100	2.7362	0101100	3.3661	1001100	3.9961	1101100	4.6260
0001101	2.7559	0101101	3.3858	1001101	4.0157	1101101	4.6457
0001110	2.7756	0101110	3.4055	1001110	4.0354	1101110	4.6654
0001111	2.7953	0101111	3.4252	1001111	4.0551	1101111	4.6850
0010000	2.8150	0110000	3.4449	1010000	4.0748	1110000	4.7047
0010001	2.8346	0110001	3.4646	1010001	4.0945	1110001	4.7244
0010010	2.8543	0110010	3.4843	1010010	4.1142	1110010	4.7441
0010011	2.8740	0110011	3.5039	1010011	4.1339	1110011	4.7638
0010100	2.8937	0110100	3.5236	1010100	4.1535	1110100	4.7835
0010101	2.9134	0110101	3.5433	1010101	4.1732	1110101	4.8031
0010110	2.9331	0110110	3.5630	1010110	4.1929	1110110	4.8228
0010111	2.9528	0110111	3.5827	1010111	4.2126	1110111	4.8425
0011000	2.9724	0111000	3.6024	1011000	4.2323	1111000	4.8622
0011001	2.9921	0111001	3.6220	1011001	4.2520	1111001	4.8819
0011010	3.0118	0111010	3.6417	1011010	4.2717	1111010	4.9016
0011011	3.0315	0111011	3.6614	1011011	4.2913	1111011	4.9213
0011100	3.0512	0111100	3.6811	1011100	4.3110	1111100	4.9409
0011101	3.0709	0111101	3.7008	1011101	4.3307	1111101	4.9606
0011110	3.0906	0111110	3.7205	1011110	4.3504	1111110	4.9803
0011111	3.1102	0111111	3.7402	1011111	4.3701	1111111	5.0000

Status	Default Value
Initial	GVD[6:0] = 00_0000 IPGVD[6:0] = 00_0000

5.3.13.7. VGH_FLAG_EN/ AB_VCI1

VGH_FLAG_EN : VGH-level-detecting-function enables register.

AB_VCI1: Set VCI1 output equal to VCI. VCI1 output is internally connected to VCI via switching circuit when AB_VCI1="H", it must be set in 120ms after Sleep Out command sent.

Status	Default Value
Initial	VGH_FLAG_EN = 1 AB_VCI1 = 0

5.3.13.8. NAB2A_G/ IPAB2A_G/ NAB2A/ IPAB2A

NAB2A_G/ IPAB2A_G : GVDD amplifier output stage selection register.

IPAB2A_G is applied in Idle Partial mode.

NAB2A_G/IPAB2A_G	Description
0	The output stage of GVDD amplifier operates as a Class-AB type
1	The output stage of GVDD amplifier operates as a Class-A type

NAB2A/ IPAB2A : VCOMH amplifier output stage selection register.

IPAB2A is applied in Idle Partial mode.

NAB2A/ IPAB2A	Description
0	The output stage of VCOMH amplifier operates as a Class-AB type
1	The output stage of VCOMH amplifier operates as a Class-A type

Status	Default Value
Initial	NAB2A_G = 1, IPAB2A_G = 1 NAB2A = 0, IPAB2A = 0

5.3.14. VCMCTL : VCOM Control Register (F4h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VCMCTL	R/W	0	1	1	1	1	0	1	0	0	F4h
1st para		1	0	VCM 6	VCM 5	VCM 4	VCM 3	VCM 2	VCM 1	VCM 0	
2nd para		1		IPVCM 6	IPVCM 5	IPVCM 4	IPVCM 3	IPVCM 2	IPVCM 1	IPVCM 0	
3rd para		1	VCOMG	VML 6	VML 5	VML 4	VML 3	VML 2	VML 1	VML 0	
4th para		1	0	IPVML 6	IPVML 5	IPVML 4	IPVML 3	IPVML 2	IPVML 1	IPVML 0	
5th para		1	0	VCIRA 2	VCIRA 1	VCIRA 0	0	VCIR 2	VCIR 1	VCIR 0	

5.3.14.1. VCM[6:0]/ IPVCM[6:0]

VCM6-0: Set the upper level of VCOM on Normal Mode (VCOMH).

Table 163. VCM[6:0] (Vref=2.0V, unit =V)

VCM[6:0]	VCOMH Voltage	VCM[6:0]	VCOMH Voltage	VCM[6:0]	VCOMH Voltage	VCM[6:0]	VCOMH Voltage
0000000	2.5000	0100000	3.1299	1000000	3.7598	1100000	4.3898
0000001	2.5197	0100001	3.1496	1000001	3.7795	1100001	4.4094
0000010	2.5394	0100010	3.1693	1000010	3.7992	1100010	4.4291
0000011	2.5591	0100011	3.1890	1000011	3.8189	1100011	4.4488
0000100	2.5787	0100100	3.2087	1000100	3.8386	1100100	4.4685
0000101	2.5984	0100101	3.2283	1000101	3.8583	1100101	4.4882
0000110	2.6181	0100110	3.2480	1000110	3.8780	1100110	4.5079
0000111	2.6378	0100111	3.2677	1000111	3.8976	1100111	4.5276
0001000	2.6575	0101000	3.2874	1001000	3.9173	1101000	4.5472
0001001	2.6772	0101001	3.3071	1001001	3.9370	1101001	4.5669
0001010	2.6969	0101010	3.3268	1001010	3.9567	1101010	4.5866
0001011	2.7165	0101011	3.3465	1001011	3.9764	1101011	4.6063
0001100	2.7362	0101100	3.3661	1001100	3.9961	1101100	4.6260
0001101	2.7559	0101101	3.3858	1001101	4.0157	1101101	4.6457
0001110	2.7756	0101110	3.4055	1001110	4.0354	1101110	4.6654
0001111	2.7953	0101111	3.4252	1001111	4.0551	1101111	4.6850
0010000	2.8150	0110000	3.4449	1010000	4.0748	1110000	4.7047
0010001	2.8346	0110001	3.4646	1010001	4.0945	1110001	4.7244
0010010	2.8543	0110010	3.4843	1010010	4.1142	1110010	4.7441
0010011	2.8740	0110011	3.5039	1010011	4.1339	1110011	4.7638
0010100	2.8937	0110100	3.5236	1010100	4.1535	1110100	4.7835
0010101	2.9134	0110101	3.5433	1010101	4.1732	1110101	4.8031
0010110	2.9331	0110110	3.5630	1010110	4.1929	1110110	4.8228
0010111	2.9528	0110111	3.5827	1010111	4.2126	1110111	4.8425
0011000	2.9724	0111000	3.6024	1011000	4.2323	1111000	4.8622
0011001	2.9921	0111001	3.6220	1011001	4.2520	1111001	4.8819
0011010	3.0118	0111010	3.6417	1011010	4.2717	1111010	4.9016
0011011	3.0315	0111011	3.6614	1011011	4.2913	1111011	4.9213
0011100	3.0512	0111100	3.6811	1011100	4.3110	1111100	4.9409
0011101	3.0709	0111101	3.7008	1011101	4.3307	1111101	4.9606
0011110	3.0906	0111110	3.7205	1011110	4.3504	1111110	4.9803
0011111	3.1102	0111111	3.7402	1011111	4.3701	1111111	5.0000

Note. Don't set any higher VCOMH level than AVDD-0.3V

IPVCM6-0: Set the upper level of VCOM (VCOMH) on partial idle mode.

Table 164. IPVCM[6:0] (Vref=2.0V, unit =V)

IPVCM[6:0]	VCOMH Voltage	IPVCM[6:0]	VCOMH Voltage	IPVCM[6:0]	VCOMH Voltage	IPVCM[6:0]	VCOMH Voltage
0000000	2.5000	0100000	3.1299	1000000	3.7598	1100000	4.3898
0000001	2.5197	0100001	3.1496	1000001	3.7795	1100001	4.4094
0000010	2.5394	0100010	3.1693	1000010	3.7992	1100010	4.4291
0000011	2.5591	0100011	3.1890	1000011	3.8189	1100011	4.4488
0000100	2.5787	0100100	3.2087	1000100	3.8386	1100100	4.4685
0000101	2.5984	0100101	3.2283	1000101	3.8583	1100101	4.4882
0000110	2.6181	0100110	3.2480	1000110	3.8780	1100110	4.5079
0000111	2.6378	0100111	3.2677	1000111	3.8976	1100111	4.5276
0001000	2.6575	0101000	3.2874	1001000	3.9173	1101000	4.5472
0001001	2.6772	0101001	3.3071	1001001	3.9370	1101001	4.5669
0001010	2.6969	0101010	3.3268	1001010	3.9567	1101010	4.5866
0001011	2.7165	0101011	3.3465	1001011	3.9764	1101011	4.6063
0001100	2.7362	0101100	3.3661	1001100	3.9961	1101100	4.6260
0001101	2.7559	0101101	3.3858	1001101	4.0157	1101101	4.6457
0001110	2.7756	0101110	3.4055	1001110	4.0354	1101110	4.6654
0001111	2.7953	0101111	3.4252	1001111	4.0551	1101111	4.6850
0010000	2.8150	0110000	3.4449	1010000	4.0748	1110000	4.7047
0010001	2.8346	0110001	3.4646	1010001	4.0945	1110001	4.7244
0010010	2.8543	0110010	3.4843	1010010	4.1142	1110010	4.7441
0010011	2.8740	0110011	3.5039	1010011	4.1339	1110011	4.7638
0010100	2.8937	0110100	3.5236	1010100	4.1535	1110100	4.7835
0010101	2.9134	0110101	3.5433	1010101	4.1732	1110101	4.8031
0010110	2.9331	0110110	3.5630	1010110	4.1929	1110110	4.8228
0010111	2.9528	0110111	3.5827	1010111	4.2126	1110111	4.8425
0011000	2.9724	0111000	3.6024	1011000	4.2323	1111000	4.8622
0011001	2.9921	0111001	3.6220	1011001	4.2520	1111001	4.8819
0011010	3.0118	0111010	3.6417	1011010	4.2717	1111010	4.9016
0011011	3.0315	0111011	3.6614	1011011	4.2913	1111011	4.9213
0011100	3.0512	0111100	3.6811	1011100	4.3110	1111100	4.9409
0011101	3.0709	0111101	3.7008	1011101	4.3307	1111101	4.9606
0011110	3.0906	0111110	3.7205	1011110	4.3504	1111110	4.9803
0011111	3.1102	0111111	3.7402	1011111	4.3701	1111111	5.0000

Note. Don't set any higher VCOMH level than AVDD-0.3V

Status	Default Value
Initial	VCM[6:0] = 00_0000 IPVCM [6:0]= 00_0000

5.3.14.2. VCOMG/ VML[6:0]/ IPVML[6:0]

VCOMG: When VCOMG = 1, low level of VCOM signal is to be fixed at AVSS. Therefore, the amplitude of VCOM signal is determined as |VCOMH – AVSS| regardless of VML setting. In this case, VCOML pad should be connected to GND, because VCOML amp is off and VCOML output is floated. When VCOMG=0, the amplitude of VCOM signal is determined as |VCOMH – VCOML|

VML6-0 : Set the Amplitude of the VCOM voltage on Normal Mode. VCOML is adjusted automatically by setting the Amplitude of VCOM voltage.

Table 165. VML[6:0] (Vref=2.0V, unit =V)

VML[6:0]	Amplitude Voltage	VML[6:0]	Amplitude Voltage	VML[6:0]	Amplitude Voltage	VML[6:0]	Amplitude Voltage
0000000	3.0000	0100000	3.7559	1000000	4.5118	1100000	5.2677
0000001	3.0236	0100001	3.7795	1000001	4.5354	1100001	5.2913
0000010	3.0472	0100010	3.8031	1000010	4.5591	1100010	5.3150
0000011	3.0709	0100011	3.8268	1000011	4.5827	1100011	5.3386
0000100	3.0945	0100100	3.8504	1000100	4.6063	1100100	5.3622
0000101	3.1181	0100101	3.8740	1000101	4.6299	1100101	5.3858
0000110	3.1417	0100110	3.8976	1000110	4.6535	1100110	5.4094
0000111	3.1654	0100111	3.9213	1000111	4.6772	1100111	5.4331
0001000	3.1890	0101000	3.9449	1001000	4.7008	1101000	5.4567
0001001	3.2126	0101001	3.9685	1001001	4.7244	1101001	5.4803
0001010	3.2362	0101010	3.9921	1001010	4.7480	1101010	5.5039
0001011	3.2598	0101011	4.0157	1001011	4.7717	1101011	5.5276
0001100	3.2835	0101100	4.0394	1001100	4.7953	1101100	5.5512
0001101	3.3071	0101101	4.0630	1001101	4.8189	1101101	5.5748
0001110	3.3307	0101110	4.0866	1001110	4.8425	1101110	5.5984
0001111	3.3543	0101111	4.1102	1001111	4.8661	1101111	5.6220
0010000	3.3780	0110000	4.1339	1010000	4.8898	1110000	5.6457
0010001	3.4016	0110001	4.1575	1010001	4.9134	1110001	5.6693
0010010	3.4252	0110010	4.1811	1010010	4.9370	1110010	5.6929
0010011	3.4488	0110011	4.2047	1010011	4.9606	1110011	5.7165
0010100	3.4724	0110100	4.2283	1010100	4.9843	1110100	5.7402
0010101	3.4961	0110101	4.2520	1010101	5.0079	1110101	5.7638
0010110	3.5197	0110110	4.2756	1010110	5.0315	1110110	5.7874
0010111	3.5433	0110111	4.2992	1010111	5.0551	1110111	5.8110
0011000	3.5669	0111000	4.3228	1011000	5.0787	1111000	5.8346
0011001	3.5906	0111001	4.3465	1011001	5.1024	1111001	5.8583
0011010	3.6142	0111010	4.3701	1011010	5.1260	1111010	5.8819
0011011	3.6378	0111011	4.3937	1011011	5.1496	1111011	5.9055
0011100	3.6614	0111100	4.4173	1011100	5.1732	1111100	5.9291
0011101	3.6850	0111101	4.4409	1011101	5.1969	1111101	5.9528
0011110	3.7087	0111110	4.4646	1011110	5.2205	1111110	5.9764
0011111	3.7323	0111111	4.4882	1011111	5.2441	1111111	6.0000

Note. Available setting range of VCOML is from VCL+0.5V to 0V. The Amplitude of VCOM cannot exceed 6V.

IPVML6-0 : Set the Amplitude of the VCOM voltage on partial idle mode.

Table 166. IPVML[6:0] (Vref=2.0V, unit =V)

IPVML[6:0]	Amplitude Voltage	IPVML[6:0]	Amplitude Voltage	IPVML[6:0]	Amplitude Voltage	IPVML[6:0]	Amplitude Voltage
0000000	3.0000	0100000	3.7559	1000000	4.5118	1100000	5.2677
0000001	3.0236	0100001	3.7795	1000001	4.5354	1100001	5.2913
0000010	3.0472	0100010	3.8031	1000010	4.5591	1100010	5.3150
0000011	3.0709	0100011	3.8268	1000011	4.5827	1100011	5.3386
0000100	3.0945	0100100	3.8504	1000100	4.6063	1100100	5.3622
0000101	3.1181	0100101	3.8740	1000101	4.6299	1100101	5.3858
0000110	3.1417	0100110	3.8976	1000110	4.6535	1100110	5.4094
0000111	3.1654	0100111	3.9213	1000111	4.6772	1100111	5.4331
0001000	3.1890	0101000	3.9449	1001000	4.7008	1101000	5.4567
0001001	3.2126	0101001	3.9685	1001001	4.7244	1101001	5.4803
0001010	3.2362	0101010	3.9921	1001010	4.7480	1101010	5.5039
0001011	3.2598	0101011	4.0157	1001011	4.7717	1101011	5.5276
0001100	3.2835	0101100	4.0394	1001100	4.7953	1101100	5.5512
0001101	3.3071	0101101	4.0630	1001101	4.8189	1101101	5.5748
0001110	3.3307	0101110	4.0866	1001110	4.8425	1101110	5.5984
0001111	3.3543	0101111	4.1102	1001111	4.8661	1101111	5.6220
0010000	3.3780	0110000	4.1339	1010000	4.8898	1110000	5.6457
0010001	3.4016	0110001	4.1575	1010001	4.9134	1110001	5.6693
0010010	3.4252	0110010	4.1811	1010010	4.9370	1110010	5.6929
0010011	3.4488	0110011	4.2047	1010011	4.9606	1110011	5.7165
0010100	3.4724	0110100	4.2283	1010100	4.9843	1110100	5.7402
0010101	3.4961	0110101	4.2520	1010101	5.0079	1110101	5.7638
0010110	3.5197	0110110	4.2756	1010110	5.0315	1110110	5.7874
0010111	3.5433	0110111	4.2992	1010111	5.0551	1110111	5.8110
0011000	3.5669	0111000	4.3228	1011000	5.0787	1111000	5.8346
0011001	3.5906	0111001	4.3465	1011001	5.1024	1111001	5.8583
0011010	3.6142	0111010	4.3701	1011010	5.1260	1111010	5.8819
0011011	3.6378	0111011	4.3937	1011011	5.1496	1111011	5.9055
0011100	3.6614	0111100	4.4173	1011100	5.1732	1111100	5.9291
0011101	3.6850	0111101	4.4409	1011101	5.1969	1111101	5.9528
0011110	3.7087	0111110	4.4646	1011110	5.2205	1111110	5.9764
0011111	3.7323	0111111	4.4882	1011111	5.2441	1111111	6.0000

Note. Available setting range of VCOML is from VCL+0.5V to 0V. The Amplitude of VCOM cannot exceed 6V.

Status	Default Value
Initial	VCOMG = 0 VML[6:0] = 00_0000 IPVML[6:0] = 00_0000

5.3.14.3. VCIRA[2:0]/ VCIR[2:0]

VCIRA2-0 : VCI recycling period of Source is sustained for the number of clock cycle which is set on VCIRA2-0.

VCIR2-0 : VCI recycling period of VCOM is sustained for the number of clock cycle which is set on VCIR2-0.

Table 167. VCIRA[2:0]/ VCIR[2:0]

*unit : INCLK

VCIRA2/ VCIR2	VCIRA1/ VCIR1	VCIRA0/ VCIR0	VCIR / VCI recycling period (Synchronized with INCLK)		
			Sn	Vcom1	Vcom2
0	0	0	0	0	0
0	0	1	1	0.5 / 1	1 / 0.5
0	1	0	2	1 / 2	2 / 1
0	1	1	3	1.5 / 3	3 / 1.5
1	0	0	4	2 / 4	4 / 2
1	0	1	5	2.5 / 5	5 / 2.5
1	1	0	6	3 / 6	6 / 3
1	1	1	7	3.5 / 7	7 / 3.5

Note1. When VCI Recycling is used, VCOMH level must be larger than VCI level.

Note2. INCLK means internal clock for display.

Note3. Do not use VCI Recycling at source driver block in case of Frame Inversion mode.(VCIRA2-0 = 000)

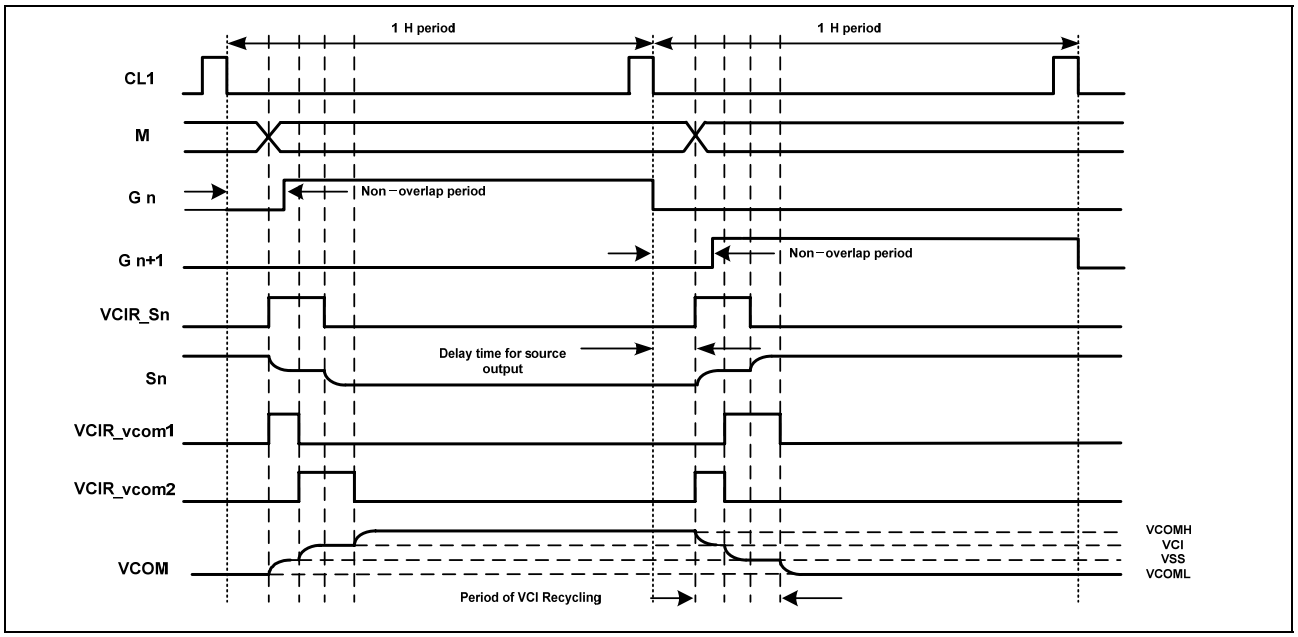


Figure 165. Set delay from gate output to source output and VCIR signal

Status	Default Value
Initial	VCIRA[2:0] = 100 VCIR[2:0] = 100

5.3.15. SRCCTL : Source Output Control Register (F5h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SRCCTL	R/W	0	1	1	1	1	0	1	0	1	F5h
1st para		1	0	0	0	GS_EN	0	0	NGF	XSG	
2nd para		1	0	IPSDT2	IPSDT1	IPSDT0	0	NSDT2	NSDT1	NSDT0	
3rd para		1	0	0	0	0	SAP3	SAP2	SAP1	SAP0	
4th para		1	NBLK_VCIR1	NBLK_VCIR0	IPBLK_VCIR1	IPBLK_VCIR0	NDISP_CON1	NDISP_CON0	IPDISP_CON1	IPDISP_CON0	
5th para		1	0	VCOM_BLK_OFF	1	1	NBLK_CON1	NBLK_CON0	IPBLK_CON1	IPBLK_CON0	
6th para		1	0	0	0	GOCM2	GOCM1	GOCM0	OCM1	OCM0	

5.3.15.1. GS_EN/ NGF/XSG

GS_EN: Set the separated Gamma mode.

Table 168. GS_EN

GS_EN	Gamma set	Description
0	Non- separated Gamma	Red Gamma apply to Green and Blue.
1 (default)	R/G/B Seperated Gamma	Use R/G/B separated gamma.

NGF: Set the negative polarity gamma register to positive polarity gamma register or user setting value. Pleae refer to the section 4.2

Table 169. NGF

NGF	Description
0(Default)	The nagetive gamma is set along with positive gamma
1	The nagetive gamma is user setting registers

XSG: Set the symmetric way of negative polarity gamma voltage to positive, X-axis or Y-axis.

Pleae refer to the section 4.2

Table 170. XSG

XSG	Description
0(Default)	Wnen NGF = 0, Positive and negative gamma are symmetrical along Y-axis
1	Wnen NGF = 0, Positive and negative gamma are symmetrical along Y-axis

Status	Default Value
Initial	GS_EN = 1 NGF = 0 XSG = 0

5.3.15.2. IPSDT[2:0]/ NSDT[2:0]

IPSDT/ NSDT : Set delay amount from gate edge (end) to source output

IPSDT is applied in Idle Partial mode.

Table 171. IPSDT[2:0]/NSDT[2:0]

NSDT2/ IPSDT2	NSDT1/ IPSDT1	NSDT0/ IPSDT0	Delay amount of the source output
0	0	0	1 INCLK
0	0	1	2 INCLK
0	1	0	3 INCLK
0	1	1	4 INCLK
1	0	0	5 INCLK
1	0	1	6 INCLK
1	1	0	7 INCLK
1	1	1	Setting Disable

Note : INCLK means internal clock for display.

In MPU I/F, INCLK is decided by CRTN. (Refer to the section 5.3.12.6)

In RGB I/F, INCLK is decided by RGB_DIV. (Refer to the section 5.3.16.5)

Status	Default Value
Initial	IPSDT[2:0] = 000 NSDT[2:0] = 000

5.3.15.3. SAP[3:0]

SAP : Adjust the slew-rate of the operational amplifier for the source driver. If higher SAP3-0 is set, LCD panel having higher resolution or higher frame frequency can be driven because the slew-rate of the operational amplifier is increased. But these bits must be set as adequate value because the amount of fixed current of the operational amplifier is also adjusted. During non-display, when SAP3-0 =”0000,” operational amplifiers are turned off, so current consumption can be reduced.

Table 172. SAP[3:0]

SAP3	SAP2	SAP1	SAP0	Source Amp. Current Level	Slew rate[us/V]		Delay[us]	
					XSG=0	XSG=1	XSG=0	XSG=1
0	0	0	0	Amp. Stop	-		-	
0	0	0	1	Setting Disable				
0	0	1	0	Setting Disable				
0	0	1	1	Slow 3	5.16		25.8	
0	1	0	0	Medium Slow 1	3.9		19.5	
0	1	0	1	Medium Slow 2	3.1		15.5	
0	1	1	0	Medium Slow 3	2.58		12.9	
0	1	1	1	Medium Slow 4	2.58	2.22	12.9	11.1
1	0	0	0	Medium Fast 1	2.58	1.94	12.9	9.7
1	0	0	1	Medium Fast 2	2.58	1.72	12.9	8.6
1	0	1	0	Medium Fast 3	2.58	1.52	12.9	7.6
1	0	1	1	Medium Fast 4	2.58	1.36	12.9	6.8
1	1	0	0	Fast1	2.58	1.20	12.9	6.0
1	1	0	1	Fast2	2.58	1.08	12.9	5.4
1	1	1	0	Fast3	2.58	0.94	12.9	4.7
1	1	1	1	Fast4 (the Fastest)	2.58	0.84	12.9	4.2

Status	Default Value
Initial	SAP[3:0] = 0011

5.3.15.4. NBLK_VCIR[1:0]/ IPBLK_VCIR[1:0]/ NDISP_CON[1:0] / IPDISP_CON[1:0]

NBLK_VCIR/ IPBLK_VCIR : In porch period and non-display area VCOM/Source VCIR recycling control

IPBLK_VCIR is applied in Idle Partial mode

Table 173. NBLK_VCIR[1:0]/ IPBLK_VCIR[1:0]

NBLK_VCIR1/ IPBLK_VCIR1/	NBLK_VCIR0/ IPBLK_VCIR0/	Porch period	Non-display area
0	0	Disable	Disable
0	1	Active	Disable
1	0	Disable	Active
1	1	Active	Active

NDISP_CON[1:0] / IPDISP_CON [1:0]: In non-display area, Source driver operation

IPDISP_CON is applied in Idle Partial mode

Table 174. NDISP_CON[1:0]

NDISP_CON1	NDISP_CON0	Operation
0	0	AMP operation
0	1	Binary operation
1	0	AMP operation
1	1	Binary operation

Table 175. IPDISP_CON [1:0]

IPDISP_CON1	IPDISP_CON0	Operation
0	0	Binary operation
0	1	Binary operation
1	0	Binary operation
1	1	Binary operation

Status	Default Value
Initial	NBLK_VCIR1[1:0] = 11, IPBLK_VCIR1[1:0] = 11 NDISP_CON[1:0]=00, IPDISP_CON [1:0] = 00

5.3.15.5. VCOM_BLK_OFF/ NBLK_CON/IPBLK_CON

VCOM_BLK_OFF: If the VCOM_BLK_OFF is high, then in porch period VCOM does not toggle. Else, VCOM is continuously toggled in porch period.

Table 176. VCOM_BLK_OFF

VCOM_BLK_OFF	Operation
0	Operating in porch period
1	Not operation in porch period

NBLK_CON / IPBLK_CON : In porch period, Source driver operation method. IPBLK_CON is applied in Idle partial mode

Table 177. NBLK_CON[1:0]

NBLK_CON1	NBLK_CON0	Operation
0	0	AMP operation
0	1	Binary operation
1	0	GND
1	1	Hi-Z

Table 178. IPBLK_CON[1:0]

IPBLK_CON1	IPBLK_CON0	Operation
0	0	Binary operation
0	1	Binary operation
1	0	GND
1	1	Hi-Z

Status	Default Value
Initial	VCOM_BLK_OFF = 0 NBLK_CON[1:0] = 00 IPBLK_CON[1:0] = 00

5.3.15.6. OCM[1:0]/GOCM[2:0]

GOCM2-0: The control bits to cancel the offset voltage of the gamma amp. This register supports the line and frame offset cancellation mode.

Table 179. GOCM[2:0]

GOCM2	GOCM1	GOCM0	gamma amp. Offset cancellation mode selection
0	0	0	4 line and 8 frame offset cancellation mode
0	0	1	2 line and 8 frame offset cancellation mode
0	1	0	8 frame offset cancellation mode
0	1	1	4 frame offset cancellation mode
1	0	0	4 frame offset cancellation mode
1	0	1	2 line and 4 frame offset cancellation mode
1	1	0	1 line and 4 frame offset cancellation mode
1	1	1	GPOL=”L” fix

Note : GPOL : The register bit for the Gamma amp. polarity.

OCM1-0: The control bits to cancel the offset voltage of the source amp. This register supports the line and frame offset cancellation mode.

Table 180. OCM[1:0]

OCM1	OCM0	Source amp. Offset cancellation mode selection
0	0	2 line and 4 frame offset cancellation mode
0	1	1 line and 4 frame offset cancellation mode
1	0	4 frame offset cancellation mode
1	1	POL=”L” fix, offset cancellation off

Note : POL : The register bit for the source amp polarity.

Status	Default Value
Initial	GOCM[2:0] = 111 OCM[1:0] = 11

5.3.16. IFCTL : Interface Control Register (F6h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IFCTL	R/W	0	1	1	1	1	0	1	1	0	F6h
1st para		1	MY_ EOR	MX_ EOR	MV_ EOR	ML_ EOR	BGR_ EOR	0	0	0	
2nd para		1	IPM 2	IPM 1	IPM 0	MDT 1	MDT 0	0	VSM	DM	
3rd para		1	VPL	HPL	DPL	EPL	ENDIAN	0	0	RIM	
4th para		1	0	0	SPR_ SEL1	SPR_ SEL0	RGB_ DIV3	RGB_ DIV2	RGB_ DIV1	RGB_ DIV0	

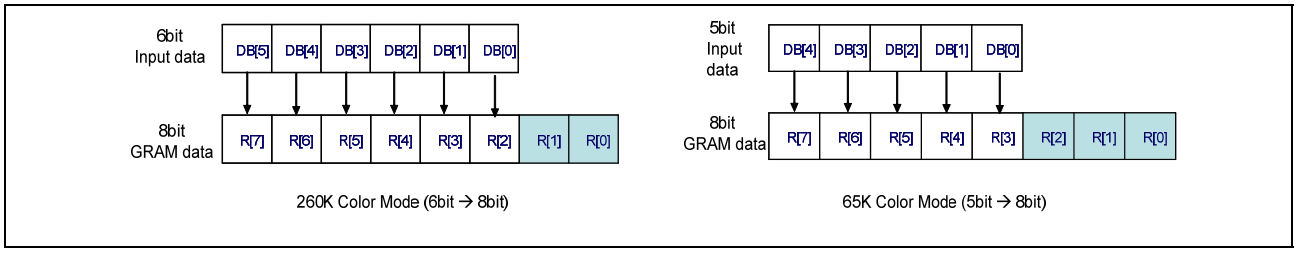
5.3.16.1. MY_EOR/ MX_EOR/ MV_EOR/ ML_EOR/ BGR_EOR

Each of these register will be used inside the IC. The set value of MADCTL is used in the IC is derived as exclusive OR between 1st parameter of IFCTL and MADCTL parameter.

Status	Default Value
Initial	MY_EOR = 0, MX_EOR = 0, MV_EOR = 0 ML_EOR = 0, BGR_EOR =0

5.3.16.2. IPM[2:0]/ MDT[1:0]/ VSM/ DM

IPM: Select the method of display expansion. (Default value = 100)



Data expansion by IMP (example of red color)

Table 181. IPM[2:0]

IPM	6bit → 8bit		5bit → 8bit		
	R[1]	R[0]	R[2]	R[1]	R[0]
000	0	0	DB[4]	0	0
001	0	1	DB[4]	0	1
010	1	0	DB[4]	1	0
011	1	1	DB[4]	1	1
100	DB[5]	DB[4]	DB[4]	DB[4]	DB[3]
101	DB[5]	0	DB[4]	DB[4]	0
110	DB[5]	1	DB[4]	DB[4]	1
111	Not defined		Not defined		

MDT: Select the method of display data transferring. (Refer to the 3.2 Display Data Format section.)

VSM : Select Vsync Interface mode.

When VSM=”1”, VSYNC interface is available. In this interface the internal display operation is synchronized with VSYNC. Data for display is written to RAM via the system interface with higher speed than for internal display operation. This method enables flicker-free display of motion pictures with the conventional interface. Refer to section 3.4.

DM : Specify the display operation mode. The interface can be set based on the bits of DM. This setting enables switching interface between internal operation and the external display interface.

Table 182. DM

DM	Display Operation Mode
0	Internal clock operation
1	RGB interface mode

Note1. Internal Clock Operation Mode with System Interface (DM=0)

Every operation in Internal Clock Operation mode is done in synchronization with the internal clock which is generated by internal OSC.

The signals input through RGB interface are all meaningless. Access to internal GRAM is done via system interface.

Note2. External Clock Operation Mode with RGB Interface (DM=1)

In External Clock Operation mode, frame sync signal (VSYNC), line sync signal (HSYNC) and DOTCLK are used for display operation.

Display data is transferred in the unit of pixel through DB bus and saved to GRAM.

Status	Default Value
Initial	IPM[2:0] = 100 MDT[1:0] = 00 VSM = 0 DM = 0

5.3.16.3. VPL/HPL/DPL/EPL

VPL : Reverses the polarity of the VSYNC signal.

VPL= “0”: VSYNC is low active.

VPL= “1”: VSYNC is high active.

HPL : Reverses the polarity of the HSYNC signal.

HPL= “0”: HSYNC is low active.

HPL= “1”: HSYNC is high active.

DPL : Reverses the polarity of the DOTCLK signal.

DPL= “0”: Display data is fetched at DOTCLK’s rising edge.

DPL= “1”: Display data is fetched at DOTCLK’s falling edge.

EPL : Set the polarity of ENABLE pad while using RGB interface.

- EPL = “0”: ENABLE =”Low” / write data of DB23

  ENABLE =”High” / do not write data of DB23

- EPL = “1”: ENABLE =”High” / write data of DB23

  ENABLE =”Low” / do not write data of DB23

Note. If Interface mode is RGB 6bit, EPL should be set to Low.

Table 183. Relationship between EPL, ENABLE and RAM Access

EPL	ENABLE	RAM write	RAM address
0	0	Valid	Updated
0	1	Invalid	Held
1	1	Valid	Updated
1	0	Invalid	Held

Status	Default Value
Initial	VPL = 0 HPL = 0 DPL = 0 EPL = 1

5.3.16.4. ENDIAN/RIM

ENDIAN: Select Little Endian Interface bit. At Little Endian mode, the host sends LSB data first.

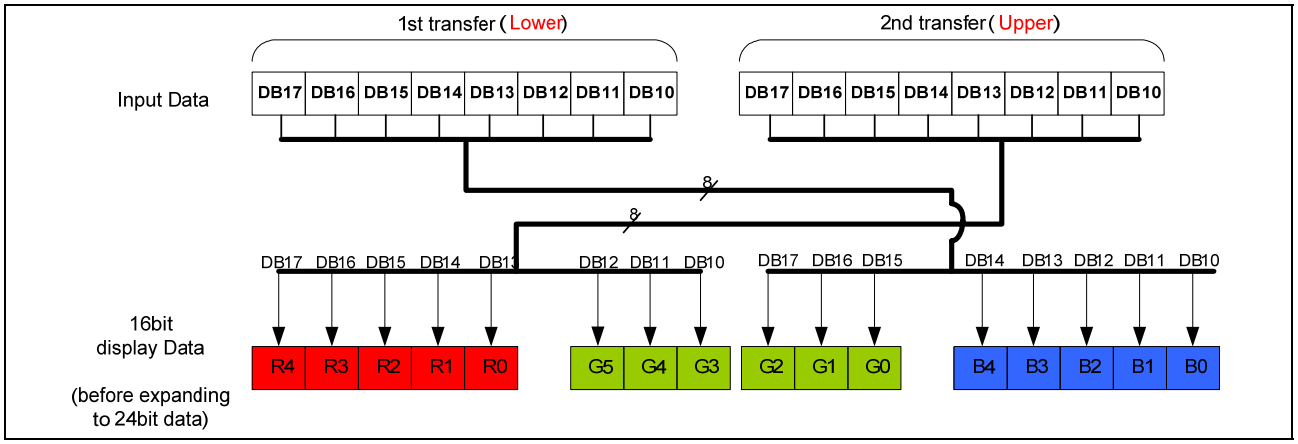


Figure 166. Little endian (65K 8bit I/F)

Table 184. ENDIAN

ENDIAN	Data transfer mode
0	Normal (MSB first)
1	Little Endian (LSB first)

Note. Little Endian is valid on only 260K 9bit I/F(MDT=00), 65K 8bit, 9bit I/F mode.

RIM: Specify the RGB interface mode when the RGB interface is used. These bits should be set before display operation through the RGB interface and should not be set during operation.

Table 185. RIM

RIM	COLMOD[6:4]	RGB Interface Mode
0	111 (16M color)	24- bit RGB interface (1 transfer/pixel)
	110 (262k color)	18- bit RGB interface (1 transfer/pixel)
	101 (65k color)	16- bit RGB interface (1 transfer/pixel)
1	111 (16M color)	8- bit RGB interface (3 transfer/pixel)
	110 (262k color)	6- bit RGB interface (3 transfer/pixel)

Status	Default Value
Initial	ENDIAN = 0 RIM = 0

5.3.16.5. SPR_SEL[1:0] / RGB_DIV[3:0]

SPR_SEL[1:0]: Short Pulse Rejection (SPR) Selection bit. SPR_SEL1 select SPR time and SPR_SEL0 select SPR ON/OFF. SPR_SEL[1:0] is Level 3 Command's register. **To use this register, to set F1h's 1st register to 5Ah must be needed.**

Table 186. SPR_SEL[1:0]

SPR_SEL[1]	SPR_SEL[0]	Description
X	0	Disable SPR function to Logic input pad.
0	1	Activate 5ns SPR function to Logic input pad.
1	1	Activate 10ns SPR function to Logic input pad

RGB_DIV3-0 : Select internal clock in RGB interface mode

Table 187. RGB_DIV[3:0]

	INCLK	
RGB_DIV[3:0]	24/18/16- bit RGB	8/6- bit RGB
0000	16 DOTCLK	16 x 3 DOTCLK
0001	15 DOTCLK	15 x 3 DOTCLK
0010	14 DOTCLK	14 x 3 DOTCLK
0011	13 DOTCLK	13 x 3 DOTCLK
0100	12 DOTCLK	12 x 3 DOTCLK
0101	11 DOTCLK	11 x 3 DOTCLK
0110	10 DOTCLK	10 x 3 DOTCLK
0111	9 DOTCLK	9 x 3 DOTCLK
1000	16 DOTCLK	16 x 3 DOTCLK
1001	17 DOTCLK	17 x 3 DOTCLK
1010	18 DOTCLK	18 x 3 DOTCLK
1011	19 DOTCLK	19 x 3 DOTCLK
1100	20 DOTCLK	20 x 3 DOTCLK
1101	21 DOTCLK	21 x 3 DOTCLK
1110	22 DOTCLK	22 x 3 DOTCLK
1111	23 DOTCLK	23 x 3 DOTCLK

Note. INCLK means Internal Clock for display.

Status	Default Value
Initial	SPR_SEL = 01 RGB_DIV = 0000

5.3.17. RGAMCTL : Positive Gamma Control Register for Red (F7h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RPGAMCTL	R/W	0	1	1	1	1	0	1	1	1	F7h
1st para		1	RGLP 1	RGLP 0	RRFP 5	RRFP 4	RRFP 3	RRFP 2	RRFP 1	RRFP 0	
2nd para		1	0	0	ROSP 5	ROSP 4	ROSP 3	ROSP 2	ROSP 1	ROSP 0	
3rd para		1	0	0	RPKP 05	RPKP 04	RRPK P3	RPKP 02	RPKP 01	RPKP 0	
4th para		1	0	0	RPKP 15	RPKP 14	RPKP 13	RPKP 12	RPKP1 1	RPKP 10	
5th para		1	0	0	RPKP 25	RPKP 24	RPKP 23	RPKP 22	RPKP 21	PKP 20	
6th para		1	0	0	RPKP 35	RPKP 34	RPKP 33	RPKP 32	RPKP 31	RPKP 30	
7th para		1	0	0	RPKP 45	RPKP 44	RPKP 43	RPKP 42	RPKP 41	RPKP 40	
8th para		1	0	0	RPKP 55	RPKP 54	RPKP 53	RPKP 52	RPKP 51	RPKP 50	
9th para		1	0	0	RPKP 65	RPKP 64	RPKP 63	RPKP 62	RPKP 61	RPKP 60	
10th para		1	0	0	RPKP 75	RPKP 74	RPKP 73	RPKP 72	RPKP 71	RPKP 70	
11th para		1	0	0	RPKP 85	RPKP 84	RPKP 83	RPKP 82	RPKP 81	RPKP 80	
12th para		1	0	0	RPKP 95	RPKP 94	RPKP 93	RPKP 92	RPKP 91	RPKP 90	
13th para		1	0	0	RPKP 105	RPKP 104	RPKP 103	RPKP 102	RPKP 101	RPKP 100	
14th para		1	RGSR P03	RGSR P02	RGSR P01	RGSR P00	RGSR P13	RGSR P12	RGSR P11	RGSR P10	
15th para		1	RGSR P23	RGSR P22	RGSR P21	RGSR P20	RGSR P33	RGSR P32	RGSR P31	RGSR P30	

RGLP: The positive voltage of red color grayscale number V1 or V254 is mainly adjusted.

RRFP: The positive voltage of red color grayscale number from V0 is mainly adjusted.

ROSP: The positive voltage of red color grayscale number from V255 is mainly adjusted.

RPKP0~RPKP10: The positive voltage of red color grayscale number from V1 to V254 is finely adjusted.

RGSRP0: The positive voltage of red color grayscale V5 is finely adjusted.

RGSRP1: The positive voltage of red color grayscale V55 is finely adjusted.

RGSRP2: The positive voltage of red color grayscale V200 is finely adjusted.

RGSRP3: The positive voltage of red color grayscale V250 is finely adjusted.

Status	Default Value
Initial	0603_040A_101A_222C_1312_1D11_0222_22h

5.3.18. RNGAMCTL : Negative Gamma Control Register for Red (F8h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RNGAMCTL	R/W	0	1	1	1	1	1	0	0	0	F8h
1st para		1	RGLN 1	RGLN 0	RRFN 5	RRFN 4	RRFN 3	RRFN 2	RRFN 1	RRFN 0	
2nd para		1	0	0	ROSN 5	ROSN 4	ROSN 3	ROSN 2	ROSN 1	ROSN 0	
3rd para		1	0	0	RPKN 05	RPKN 04	RPKN 03	RPKN 02	RPKN 01	RPKN 0	
4th para		1	0	0	RPKN 15	RPKN 14	RPKN 13	RPKN 12	RPKN 11	RPKN 10	
5th para		1	0	0	RPKN 25	RPKN 24	RPKN 23	RPKN 22	RPKN 21	RPKN 20	
6th para		1	0	0	RPKN 35	RPKN 34	RPKN 33	RPKN 32	RPKN 31	RPKN 30	
7th para		1	0	0	RPKN 45	RPKN 44	RPKN 43	RPKN 42	RPKN 41	RPKN 40	
8th para		1	0	0	RPKN 55	RPKN 54	RPKN 53	RPKN 52	RPKN 51	RPKN 50	
9th para		1	0	0	RPKN 65	RPKN 64	RPKN 63	RPKN 62	RPKN 61	RPKN 60	
10th para		1	0	0	RPKN 75	RPKN 74	RPKN 73	RPKN 72	RPKN 71	RPKN 70	
11th para		1	0	0	RPKN 85	RPKN 84	RPKN 83	RPKN 82	RPKN 81	RPKN 80	
12th para		1	0	0	RPKN 95	RPKN 94	RPKN 93	RPKN 92	RPKN 91	RPKN 90	
13th para		1	0	0	RPKN 105	RPKN 104	RPKN 103	RPKN 102	RPKN 101	RPKN 100	
14th para		1	RGSR N03	RGSR N02	RGSR N01	RGSR N00	RGSR N13	RGSR N12	RGSR N11	RGSR N10	
15th para		1	RGSR N23	RGSR N22	RGSR N21	RGSR N20	RGSR N33	RGSR N32	RGSR N31	RGSR N30	

RGLN: The negative voltage of red color grayscale V1 or V254 is mainly adjusted.

RRFN: The negative voltage of red color grayscale number from V0 is mainly adjusted.

ROSN: The negative voltage of red color grayscale number from V255 is mainly adjusted.

RPKN0~RPKN10: The negative red color voltage of grayscale number from V1 to V254 is finely adjusted.

RGSRN0: The negative voltage of red color grayscale V5 is finely adjusted.

RGSRN1: The negative voltage of red color grayscale V55 is finely adjusted.

RGSRN2: The negative voltage of red color grayscale V200 is finely adjusted.

RGSRN3: The negative voltage of red color grayscale V250 is finely adjusted.

Status	Default Value
Initial	0603_040A_101A_222C_1312_1D11_0222_22h

5.3.19. GGAMCTL : Positive Gamma Control Register for Green (F9h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GPGAMCTL	R/W	0	1	1	1	1	1	0	0	1	F9h
1st para		1	GGLP 1	GGLP 0	GRFP 5	GRFP 4	GRFP 3	GRFP 2	GRFP 1	GRFP 0	
2nd para		1	0	0	GOSP 5	GOSP 4	GOSP 3	GOSP 2	GOSP 1	GOSP 0	
3rd para		1	0	0	GPKP 05	GPKP 04	GRPK P3	GPKP 02	GPKP 01	GPKP 0	
4th para		1	0	0	GPKP 15	GPKP 14	GPKP 13	GPKP 12	GPKP 11	GPKP 10	
5th para		1	0	0	GPKP 25	GPKP 24	GPKP 23	GPKP 22	GPKP 21	GPKP 20	
6th para		1	0	0	GPKP 35	GPKP 34	GPKP 33	GPKP 32	GPKP 31	GPKP 30	
7th para		1	0	0	GPKP 45	GPKP 44	GPKP 43	GPKP 42	GPKP 41	GPKP 40	
8th para		1	0	0	GPKP 55	GPKP 54	GPKP 53	GPKP 52	GPKP 51	GPKP 50	
9th para		1	0	0	GPKP 65	GPKP 64	GPKP 63	GPKP 62	GPKP 61	GPKP 60	
10th para		1	0	0	GPKP 75	GPKP 74	GPKP 73	GPKP 72	GPKP 71	GPKP 70	
11th para		1	0	0	GPKP 85	GPKP 84	GPKP 83	GPKP 82	GPKP 81	GPKP 80	
12th para		1	0	0	GPKP 95	GPKP 94	GPKP 93	GPKP 92	GPKP 91	GPKP 90	
13th para		1	0	0	GPKP 105	GPKP 104	GPKP 103	GPKP 102	GPKP 101	GPKP 100	
14th para		1	GGSR P03	GGSR P02	GGSR P01	GGSR P00	GGSR P13	GGSR P12	GGSR P11	GGSR P10	
15th para		1	GGSR P23	GGSR P22	GGSR P21	GGSR P20	GGSR P33	GGSR P32	GGSR P31	GGSR P30	

GGLP: The positive voltage of green color grayscale V1 or V254 is mainly adjusted.

GRFP: The positive voltage of green color grayscale number from V0 is mainly adjusted.

GOSP: The positive voltage of green color grayscale number from V255 is mainly adjusted.

GPKP0~GPKP10: The positive voltage of green color grayscale number from V1 to V254 is finely adjusted.

GGSRP0: The positive voltage of green color grayscale V5 is finely adjusted.

GGSRP1: The positive voltage of green color grayscale V55 is finely adjusted.

GGSRP2: The positive voltage of green color grayscale V200 is finely adjusted.

GGSRP3: The positive voltage of green color grayscale V250 is finely adjusted.

Status	Default Value
Initial	0603_040A_101A_222C_1312_1D11_0222_22h

5.3.20. GNGAMCTL : Negative Gamma Control Register for Green (FAh)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GNGAMCTL	R/W	0	1	1	1	1	1	0	1	0	FAh
1st para		1	GGLN 1	GGLN 0	GRFN 5	GRFN 4	GRFN 3	GRFN 2	GRFN 1	GRFN 0	
2nd para		1	0	0	GOSN 5	GOSN 4	GOSN 3	GOSN 2	GOSN 1	GOSN 0	
3rd para		1	0	0	GPKN 05	GPKN 04	GPKN 03	GPKN 02	GPKN 01	GPKN 00	
4th para		1	0	0	GPKN 15	GPKN 14	GPKN 13	GPKN 12	GPKN 11	GPKN 10	
5th para		1	0	0	GPKN 25	GPKN 24	GPKN 23	GPKN 22	GPKN 21	GPKN 20	
6th para		1	0	0	GPKN 35	GPKN 34	GPKN 33	GPKN 32	GPKN 31	GPKN 30	
7th para		1	0	0	GPKN 45	GPKN 44	GPKN 43	GPKN 42	GPKN 41	GPKN 40	
8th para		1	0	0	GPKN 55	GPKN 54	GPKN 53	GPKN 52	GPKN 51	GPKN 50	
9th para		1	0	0	GPKN 65	GPKN 64	GPKN 63	GPKN 62	GPKN 61	GPKN 60	
10th para		1	0	0	GPKN 75	GPKN 74	GPKN 73	GPKN 72	GPKN 71	GPKN 70	
11th para		1	0	0	GPKN 85	GPKN 84	GPKN 83	GPKN 82	GPKN 81	GPKN 80	
12th para		1	0	0	GPKN 95	GPKN 94	GPKN 93	GPKN 92	GPKN 91	GPKN 90	
13th para		1	0	0	GPKN 105	GPKN 104	GPKN 103	GPKN 102	GPKN 101	GPKN 100	
14th para		1	GGSR N03	GGSR N02	GGSR N01	GGSR N00	GGSR N13	GGSR N12	GGSR N11	GGSR N10	
15th para		1	GGSR N23	GGSR N22	GGSR N21	GGSR N20	GGSR N33	GGSR N32	GGSR N31	GGSR N30	

GGLN: The negative voltage of green color grayscale V1 or V254 is mainly adjusted.

GRFN: The negative voltage of green color grayscale number from V0 is mainly adjusted.

GOSN: The negative voltage of green color grayscale number from V255 is mainly adjusted.

GPKN0~GPKN10: The negative green color voltage of grayscale number from V1 to V254 is finely adjusted.

GGSRN0: The negative voltage of green color grayscale V5 is finely adjusted.

GGSRN1: The negative voltage of green color grayscale V55 is finely adjusted.

GGSRN2: The negative voltage of green color grayscale V200 is finely adjusted.

GGSRN3: The negative voltage of green color grayscale V250 is finely adjusted.

Status	Default Value
Initial	0603_040A_101A_222C_1312_1D11_0222_22h

5.3.21. BGAMCTL : Positive Gamma Control Register for Blue (FBh)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BPGAMCTL	R/W	0	1	1	1	1	1	0	1	1	FBh
1st para		1	BGLP 1	BGLP 0	BRFP 5	BRFP 4	BRFP 3	BRFP 2	BRFP 1	BRFP 0	
2nd para		1	0	0	BOSP 5	BOSP 4	BOSP 3	BOSP 2	BOSP 1	BOSP 0	
3rd para		1	0	0	BPKP 05	BPKP 04	BRPK P3	BPKP 02	BPKP 01	BPKP 0	
4th para		1	0	0	BPKP 15	BPKP 14	BPKP 13	BPKP 12	BPKP1 1	BPKP 10	
5th para		1	0	0	BPKP 25	BPKP 24	BPKP 23	BPKP 22	BPKP 21	BKP20	
6th para		1	0	0	BPKP 35	BPKP 34	BPKP 33	BPKP 32	BPKP 31	BPKP 30	
7th para		1	0	0	BPKP 45	BPKP 44	BPKP 43	BPKP 42	BPKP 41	BPKP 40	
8th para		1	0	0	BPKP 55	BPKP 54	BPKP 53	BPKP 52	BPKP 51	BPKP 50	
9th para		1	0	0	BPKP 65	BPKP 64	BPKP 63	BPKP 62	BPKP 61	BPKP 60	
10th para		1	0	0	BPKP 75	BPKP 74	BPKP 73	BPKP 72	BPKP 71	BPKP 70	
11th para		1	0	0	BPKP 85	BPKP 84	BPKP 83	BPKP 82	BPKP 81	BPKP 80	
12th para		1	0	0	BPKP 95	BPKP 94	BPKP 93	BPKP 92	BPKP 91	BPKP 90	
13th para		1	0	0	BPKP 105	BPKP 104	BPKP 103	BPKP 102	BPKP 101	BPKP 100	
14th para		1	BGSR P03	BGSR P02	BGSR P01	BGSR P00	BGSR P13	BGSR P12	BGSR P11	BGSR P10	
15th para		1	BGSR P23	BGSR P22	BGSR P21	BGSR P20	BGSR P33	BGSR P32	BGSR P31	BGSR P30	

BGLP: The positive voltage of blue color grayscale V1 or V254 is mainly adjusted.

BRFP: The positive voltage of blue color grayscale number from V0 is mainly adjusted.

BOSP: The positive voltage of blue color grayscale number from V255 is mainly adjusted.

BPKP0~BPKP10: The positive voltage of blue color grayscale number from V1 to V254 is finely adjusted.

BGSRP0: The positive voltage of blue color grayscale V5 is finely adjusted.

BGSRP1: The positive voltage of blue color grayscale V55 is finely adjusted.

BGSRP2: The positive voltage of blue color grayscale V200 is finely adjusted.

BGSRP3: The positive voltage of blue color grayscale V250 is finely adjusted.

Status	Default Value
Initial	0603_040A_101A_222C_1312_1D11_0222_22h

5.3.22. BNGAMCTL : Negative Gamma Control Register for Blue(FCh)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BNGAMCTL	R/W	0	1	1	1	1	1	1	0	0	FCh
1st para		1	BGLN 1	BGLN 0	BRFN 5	BRFN 4	BRFN 3	BRFN 2	BRFN 1	BRFN 0	
2nd para		1	0	0	BOSN 5	BOSN 4	BOSN 3	BOSN 2	BOSN 1	BOSN 0	
3rd para		1	0	0	BPKN 05	BPKN 04	BPKN 03	BPKN 02	BPKN 01	BPKN 0	
4th para		1	0	0	BPKN 15	BPKN 14	BPKN 13	BPKN 12	BPKN1 1	BPKN 10	
5th para		1	0	0	BPKN 25	BPKN 24	BPKN 23	BPKN 22	BPKN 21	BPKN 20	
6th para		1	0	0	BPKN 35	BPKN 34	BPKN 33	BPKN 32	BPKN 31	BPKN 30	
7th para		1	0	0	BPKN 45	BPKN 44	BPKN 43	BPKN 42	BPKN 41	BPKN 40	
8th para		1	0	0	BPKN 55	BPKN 54	BPKN 53	BPKN 52	BPKN 51	BPKN 50	
9th para		1	0	0	BPKN 65	BPKN 64	BPKN 63	BPKN 62	BPKN 61	BPKN 60	
10th para		1	0	0	BPKN 75	BPKN 74	BPKN 73	BPKN 72	BPKN 71	BPKN 70	
11th para		1	0	0	BPKN 85	BPKN 84	BPKN 83	BPKN 82	BPKN 81	BPKN 80	
12th para		1	0	0	BPKN 95	BPKN 94	BPKN 93	BPKN 92	BPKN 91	BPKN 90	
13th para		1	0	0	BPKN 105	BPKN 104	BPKN 103	BPKN 102	BPKN 101	BPKN 100	
14th para		1	BGSR N03	BGSR N02	BGSR N01	BGSR N00	BGSR N13	BGSR N12	BGSR N11	BGSR N10	
15th para		1	BGSR N23	BGSR N22	BGSR N21	BGSR N20	BGSR N33	BGSR N32	BGSR N31	BGSR N30	

BGLN: The negative voltage of blue color grayscale number from V1 or V254 is mainly adjusted.

BRFN: The negative voltage of blue color grayscale number from V0 is mainly adjusted.

BOSN: The negative voltage of blue color grayscale number from V255 is mainly adjusted.

BPKN0~BPKN10: The negative blue color voltage of grayscale number from V1 to V254 is finely adjusted.

BGSRN0: The negative voltage of blue color grayscale V5 is finely adjusted.

BGSRN1: The negative voltage of blue color grayscale V55 is finely adjusted.

BGSRN2: The negative voltage of blue color grayscale V200 is finely adjusted.

BGSRN3: The negative voltage of blue color grayscale V250 is finely adjusted.

Status	Default Value
Initial	0603_040A_101A_222C_1312_1D11_0222_22h

5.3.23. GATECTL : Gate Control Register (FDh)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GATECTL	R/W	0	1	1	1	1	1	1	0	1	FDh
1st param		1	0	IPNO 2	IPNO 1	IPNO 0	0	NNO 2	NNO 1	NNO 0	
2nd param		1	0	0	0	0	0	0	SEL_ NL1	SEL_ NL0	

IPNO/NNO : Set amount of non-overlap for the gate output.

IPNO is applied in Idle Partial mode.

Table 188. IPNO[2:0]/ NNO[2:0]

IPNO2/ NNO2	IPNO1/ NNO1	IPNO0/NNO0	Amount of non-overlap
0	0	0	Setting disable
0	0	1	1 INCLK
0	1	0	2 INCLK
0	1	1	3 INCLK
1	0	0	4 INCLK
1	0	1	5 INCLK
1	1	0	6 INCLK
1	1	1	7 INCLK

Note1. The amount of non-overlap time is defined from starting time of 1H.

Note2. INCLK means internal clock for display.

In MPU I/F, INCLK is decided by CRTN. (Refer to the section 5.3.12.6)

In RGB I/F, INCLK is decided by RGB_DIV. (Refer to the section 5.3.16.5)

SEL_NL[1:0] : Selects the number of lines driving LCD drive.

Table 189. SEL_NL[1:0] and Drive Duty

SEL_NL[1:0]	Display Size	Drive Line
00	240 X 432	432
01	240 X 400	400
1*	240 X 320	320

Status	Default Value
Initial	IPNO[2:0] = 001, NNO[2:0] = 001 SEL_NL[1:0] = 00

5.3.24. DCON : Manual Display Control Register (D9h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DCON	R/W	0	1	1	1	1	1	1	1	1	D9h
1st param		1	0	0	0	0	0	D_CON2	D_CON1	D_CON0	

D_CON2: When APON=0 and D_CON2=1, Display Status is controled by D_CON[1:0]. When D_CON2=0, D_CON[1:0] Setting is ignored.

D_CON1-0: Display Status is controled by D_CON[1:0], Please refer Following Table.

Table 190. D_CON[1:0]

Register		Chip Operation			Display Status
D_CON[1:0]	GON	SOURCE	VCOM	GATE	
00	X	AVSS	AVSS	VSS	Halt
01	0	AVSS	AVSS	VGL	Halt
01	1	AVSS	AVSS	Operate	Blank Display
10	0	Operate (Same Phase of VCOM)	Operate	VGL	Halt
10	1	Operate (Same Phase of VCOM)	Operate	Operate	Blank Display
11	0	Operate (GRAM Data)	Operate	VGL	Halt
11	1	Operate (GRAM Data)	Operate	Operate	GRAM Display

Status	Default Value
Initial	D_CON[2:0]=000

5.3.25. TESTKEY : TEST KEY Control Register (F1h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DCON	W	0	1	1	1	1	1	1	1	1	F1h
1st param		1	TESTK 7	TESTK 6	TESTK 5	TESTK 4	TESTK 3	TESTK 2	TESTK 1	TESTK 0	

TESTK7-0: Level 3 Command Protection TEST_KEY.If use Level 3 Command(FFh & F6h's SPR_SEL). This Register should be set to "5Ah" for writing Level 3 registers.

Status	Default Value
Initial	TESTK[7:0]=0000_0000

5.3.26. EDSTEST : Logic Test Register2 (FFh)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
EDSTEST	R/W	0	1	1	1	1	1	1	1	1	FFh
1st param		1	-	-	0	0	0	0	0	0	
2nd param		1	-	-	0	0	0	0	0	0	
3rd param		1	-	-	0	0	0	0	0	0	
4th param		1	-	SD_EN	SD1	SD2	SD3	0	0	0	

FFh command is Level 3 command, so to use this command, to set F1h's 1st register to 5Ah must be needed.

SD_EN : Select S/D Free On/Off (0 : OFF, 1: ON)

SD1 : S/D Free control register. At auto power mode, L→ H PON after 1/4 frame.

SD2 : S/D Free control register. At auto power mode, L→ H PON1 after 1/2 frame.

SD3 : S/D Free control register. At auto power mode, same as PON2.

Status	Default Value
Initial	1st para: 0000_0000 2nd para: 0000_0000 3rd para: 0000_0000 4th para: 0000_0000

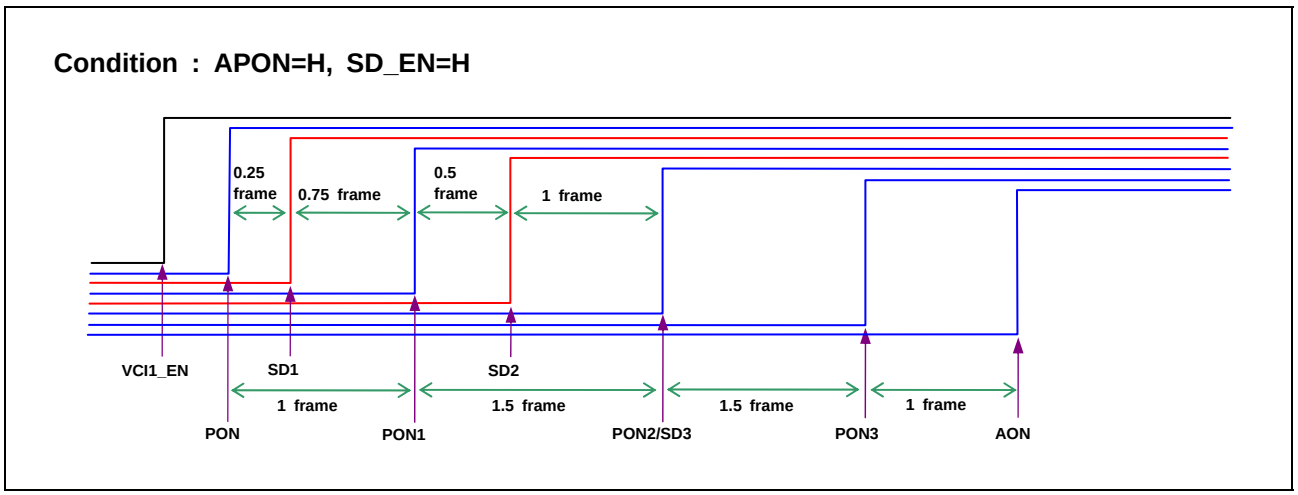


Figure 167. S/D Free Signal Timing Diagram in Automatic Power-up Sequence

CHAPTER 6

APPENDIX

6 APPENDIX

6.1. APPLICATION CIRCUIT

A typical application circuit is shown in following figure.

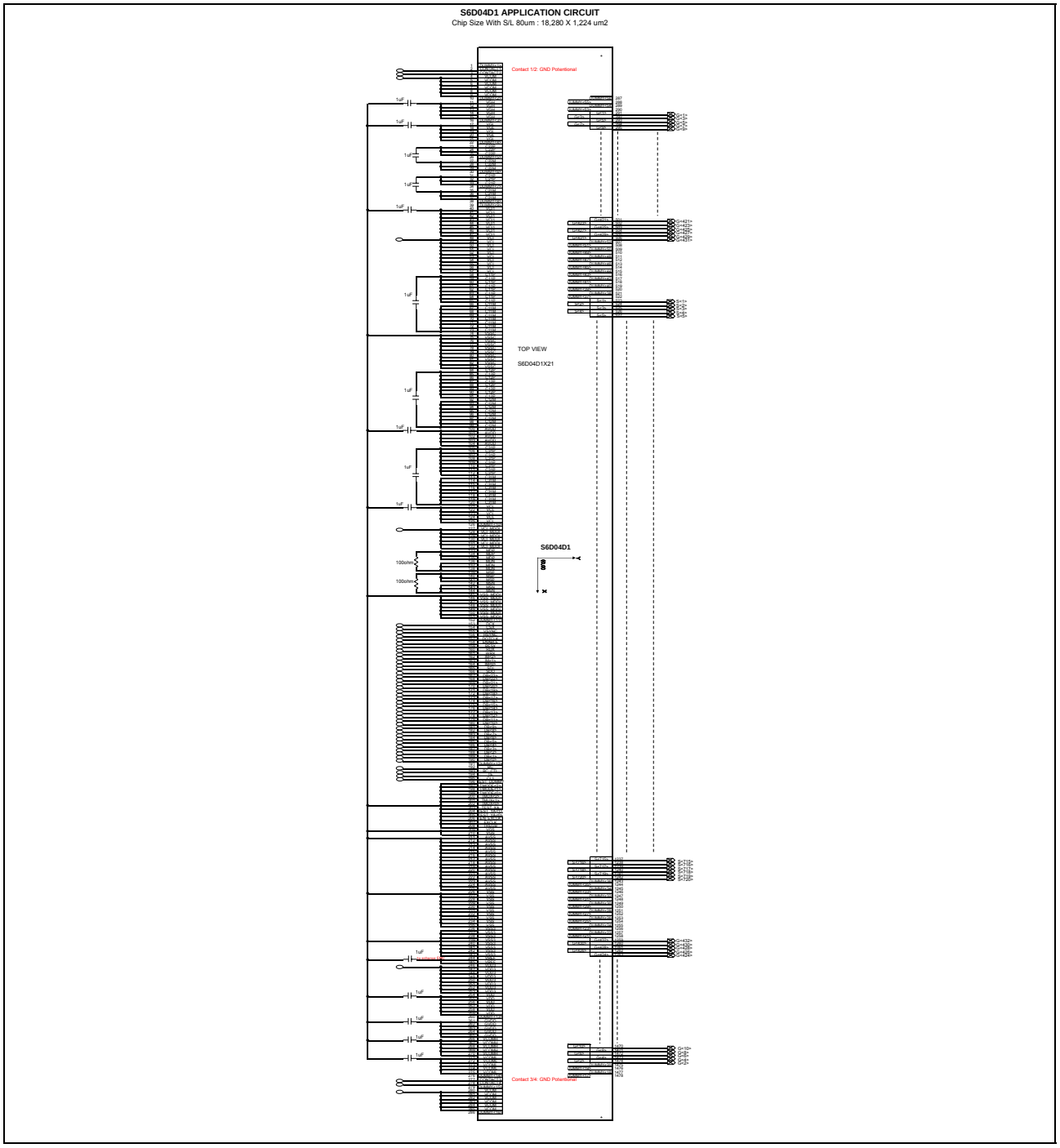


Figure 168. Application circuit

6.2. EXTERNAL COMPONENT

Table 191. External components

Name	Device	Value	Connection	Note	
C1	Capacitor	1uF	VGH – GND		18V
C2	Capacitor	1uF	VGL – GND		18V
C3	Capacitor	1uF	C22M – C22P		18V
C4	Capacitor	1uF	C21M – C21P		18V
C5	Capacitor	1uF	VCI1 – GND		3V
C6	Capacitor	1uF	C11M – C11P		6V
C7	Capacitor	1uF	C12M – C12P		6V
C8	Capacitor	1uF	C31M – C31P	Maximum	6V
C9	Capacitor	1uF	VCL – GND	Ratings	3V
C10	Capacitor	1uF	AVDD – GND	Voltage	10V
C11	Capacitor	1uF	VDD – GND		3V
C12	Capacitor	1uF	VREF – GND		3V
C13	Capacitor	1uF	GVDD – GND		6V
C14	Capacitor	1uF	VCOMH – GND		6V
C15	Capacitor	1uF	VCOML – GND		6V
R1	Resistor	100 Ohm	MDP – MDN		-
R2	Resistor	100 Ohm	MSP – MSN		-

Note. Component C12 (described in gray-color) is optional for this application.

6.3. PAD CENTER COORDINATES

Table 192. Pad center coordinates [Unit: μm]

NO	Name	X	Y	NO	Name	X	Y	NO	Name	X	Y
1	DUMMY<1>	-8912.5	-537	51	VCI	-5912.5	-537	101	AVDD	-2912.5	-537
2	CONTACT1	-8852.5	-537	52	VCI	-5852.5	-537	102	AVDD	-2852.5	-537
3	CONTACT2	-8792.5	-537	53	VCI	-5792.5	-537	103	AVDD	-2792.5	-537
4	VCOM	-8732.5	-537	54	VCI	-5732.5	-537	104	AVDD	-2732.5	-537
5	VCOM	-8672.5	-537	55	VCI	-5672.5	-537	105	C31P	-2672.5	-537
6	VCOM	-8612.5	-537	56	VCI	-5612.5	-537	106	C31P	-2612.5	-537
7	VCOM	-8552.5	-537	57	VCI	-5552.5	-537	107	C31P	-2552.5	-537
8	VCOM	-8492.5	-537	58	C11P	-5492.5	-537	108	C31P	-2492.5	-537
9	VCOM	-8432.5	-537	59	C11P	-5432.5	-537	109	C31P	-2432.5	-537
10	DUMMY<2>	-8372.5	-537	60	C11P	-5372.5	-537	110	C31P	-2372.5	-537
11	VGH	-8312.5	-537	61	C11P	-5312.5	-537	111	C31P	-2312.5	-537
12	VGH	-8252.5	-537	62	C11P	-5252.5	-537	112	C31P	-2252.5	-537
13	VGH	-8192.5	-537	63	C11P	-5192.5	-537	113	C31M	-2192.5	-537
14	VGH	-8132.5	-537	64	C11P	-5132.5	-537	114	C31M	-2132.5	-537
15	VGH	-8072.5	-537	65	C11P	-5072.5	-537	115	C31M	-2072.5	-537
16	DUMMY<3>	-8012.5	-537	66	C11M	-5012.5	-537	116	C31M	-2012.5	-537
17	VGL	-7952.5	-537	67	C11M	-4952.5	-537	117	C31M	-1952.5	-537
18	VGL	-7892.5	-537	68	C11M	-4892.5	-537	118	C31M	-1892.5	-537
19	VGL	-7832.5	-537	69	C11M	-4832.5	-537	119	C31M	-1832.5	-537
20	VGL	-7772.5	-537	70	C11M	-4772.5	-537	120	C31M	-1772.5	-537
21	VGL	-7712.5	-537	71	C11M	-4712.5	-537	121	VCL	-1712.5	-537
22	DUMMY<4>	-7652.5	-537	72	C11M	-4652.5	-537	122	VCL	-1652.5	-537
23	C22P	-7592.5	-537	73	C11M	-4592.5	-537	123	VCL	-1592.5	-537
24	C22P	-7532.5	-537	74	VSSC	-4532.5	-537	124	VCL	-1532.5	-537
25	C22P	-7472.5	-537	75	VSSC	-4472.5	-537	125	VCL	-1472.5	-537
26	DUMMY<5>	-7412.5	-537	76	VSSC	-4412.5	-537	126	DUMMY<10>	-1412.5	-537
27	C22M	-7352.5	-537	77	VSSC	-4352.5	-537	127	VCI_MDDI	-1352.5	-537
28	C22M	-7292.5	-537	78	VSSC	-4292.5	-537	128	VCI_MDDI	-1292.5	-537
29	C22M	-7232.5	-537	79	VSSC	-4232.5	-537	129	VCI_MDDI	-1232.5	-537
30	DUMMY<6>	-7172.5	-537	80	VSSC	-4172.5	-537	130	VCI_MDDI	-1172.5	-537
31	C21P	-7112.5	-537	81	VSSC	-4112.5	-537	131	VCI_MDDI	-1112.5	-537
32	C21P	-7052.5	-537	82	VSSC	-4052.5	-537	132	VCI_MDDI	-1052.5	-537
33	C21P	-6992.5	-537	83	VSSC	-3992.5	-537	133	MDP	-992.5	-537
34	DUMMY<7>	-6932.5	-537	84	C12P	-3932.5	-537	134	MDP	-932.5	-537
35	C21M	-6872.5	-537	85	C12P	-3872.5	-537	135	MDP	-872.5	-537
36	C21M	-6812.5	-537	86	C12P	-3812.5	-537	136	MDN	-812.5	-537
37	C21M	-6752.5	-537	87	C12P	-3752.5	-537	137	MDN	-752.5	-537
38	DUMMY<8>	-6692.5	-537	88	C12P	-3692.5	-537	138	MDN	-692.5	-537
39	DUMMY<9>	-6632.5	-537	89	C12P	-3632.5	-537	139	MSP	-632.5	-537
40	VCI1	-6572.5	-537	90	C12P	-3572.5	-537	140	MSP	-572.5	-537
41	VCI1	-6512.5	-537	91	C12P	-3512.5	-537	141	MSP	-512.5	-537
42	VCI1	-6452.5	-537	92	C12M	-3452.5	-537	142	MSN	-452.5	-537
43	VCI1	-6392.5	-537	93	C12M	-3392.5	-537	143	MSN	-392.5	-537
44	VCI1	-6332.5	-537	94	C12M	-3332.5	-537	144	MSN	-332.5	-537
45	VCI1	-6272.5	-537	95	C12M	-3272.5	-537	145	VSS_MDDI	-272.5	-537
46	VCI1	-6212.5	-537	96	C12M	-3212.5	-537	146	VSS_MDDI	-212.5	-537
47	VCI1	-6152.5	-537	97	C12M	-3152.5	-537	147	VSS_MDDI	-152.5	-537
48	VCI	-6092.5	-537	98	C12M	-3092.5	-537	148	VSS_MDDI	-92.5	-537
49	VCI	-6032.5	-537	99	C12M	-3032.5	-537	149	VSS_MDDI	-32.5	-537
50	VCI	-5972.5	-537	100	AVDD	-2972.5	-537	150	VSS_MDDI	27.5	-537

Note. Contact1 and Contact2 pins show ground potential during power-on status.

NO	Name	X	Y	NO	Name	X	Y	NO	Name	X	Y
151	VSS_MDDI	87.5	-537	201	TMUX<1>	3812.5	-537	251	VDD3	6812.5	-537
152	DUMMY<11>	147.5	-537	202	TMUX<0>	3872.5	-537	252	VDD3	6872.5	-537
153	DCX	207.5	-537	203	TEST_XA	3932.5	-537	253	VDD3	6932.5	-537
154	CSX	267.5	-537	204	TEST_YA<1>	3992.5	-537	254	VDD	6992.5	-537
155	VSYNC	327.5	-537	205	TEST_YA<0>	4052.5	-537	255	VDD	7052.5	-537
156	HSYNC	387.5	-537	206	EN_EXCLK	4112.5	-537	256	VDD	7112.5	-537
157	DOTCLK	447.5	-537	207	EXCLK	4172.5	-537	257	VDD	7172.5	-537
158	ENABLE	507.5	-537	208	TREGB	4232.5	-537	258	VDD	7232.5	-537
159	RESX	567.5	-537	209	VGS	4292.5	-537	259	VDD	7292.5	-537
160	RDX	627.5	-537	210	VGS	4352.5	-537	260	DUMMY<13>	7352.5	-537
161	WRX	687.5	-537	211	AVSS	4412.5	-537	261	GVDD	7412.5	-537
162	IM<2>	747.5	-537	212	AVSS	4472.5	-537	262	GVDD	7472.5	-537
163	IM<1>	807.5	-537	213	AVSS	4532.5	-537	263	GVDD	7532.5	-537
164	IM<0>	867.5	-537	214	AVSS	4592.5	-537	264	GVDD	7592.5	-537
165	SDI	927.5	-537	215	AVSS	4652.5	-537	265	GVDD	7652.5	-537
166	SDO	987.5	-537	216	AVSS	4712.5	-537	266	VCOMH	7712.5	-537
167	DB<23>	1072.5	-537	217	AVSS	4772.5	-537	267	VCOMH	7772.5	-537
168	DB<22>	1157.5	-537	218	AVSS	4832.5	-537	268	VCOMH	7832.5	-537
169	DB<21>	1242.5	-537	219	AVSS	4892.5	-537	269	VCOMH	7892.5	-537
170	DB<20>	1327.5	-537	220	AVSS	4952.5	-537	270	VCOMH	7952.5	-537
171	DB<19>	1412.5	-537	221	AVSS	5012.5	-537	271	VCOML	8012.5	-537
172	DB<18>	1497.5	-537	222	AVSS	5072.5	-537	272	VCOML	8072.5	-537
173	DB<17>	1582.5	-537	223	AVSS	5132.5	-537	273	VCOML	8132.5	-537
174	DB<16>	1667.5	-537	224	AVSS	5192.5	-537	274	VCOML	8192.5	-537
175	DB<15>	1752.5	-537	225	AVSS	5252.5	-537	275	VCOML	8252.5	-537
176	DB<14>	1837.5	-537	226	VSS	5312.5	-537	276	DUMMY<14>	8312.5	-537
177	DB<13>	1922.5	-537	227	VSS	5372.5	-537	277	CONTACT3	8372.5	-537
178	DB<12>	2007.5	-537	228	VSS	5432.5	-537	278	CONTACT4	8432.5	-537
179	DB<11>	2092.5	-537	229	VSS	5492.5	-537	279	DUMMY<15>	8492.5	-537
180	DB<10>	2177.5	-537	230	VSS	5552.5	-537	280	VCOM	8552.5	-537
181	DB<9>	2262.5	-537	231	VSS	5612.5	-537	281	VCOM	8612.5	-537
182	DB<8>	2347.5	-537	232	VSS	5672.5	-537	282	VCOM	8672.5	-537
183	DB<7>	2432.5	-537	233	VSS	5732.5	-537	283	VCOM	8732.5	-537
184	DB<6>	2517.5	-537	234	VSS	5792.5	-537	284	VCOM	8792.5	-537
185	DB<5>	2602.5	-537	235	VSS	5852.5	-537	285	VCOM	8852.5	-537
186	DB<4>	2687.5	-537	236	VSS3	5912.5	-537	286	DUMMY<16>	8912.5	-537
187	DB<3>	2772.5	-537	237	VSS3	5972.5	-537	287	DUMMY<17>	8992.5	344
188	DB<2>	2857.5	-537	238	VSS3	6032.5	-537	288	DUMMY<18>	8977.5	500
189	DB<1>	2942.5	-537	239	VSS3	6092.5	-537	289	DUMMY<19>	8962.5	344
190	DB<0>	3027.5	-537	240	VSS3	6152.5	-537	290	DUMMY<20>	8947.5	500
191	DUMMY<12>	3112.5	-537	241	VSS3	6212.5	-537	291	G<2>	8932.5	344
192	BC	3172.5	-537	242	VSS3	6272.5	-537	292	G<4>	8917.5	500
193	BC_CTL	3257.5	-537	243	VSS3	6332.5	-537	293	G<6>	8902.5	344
194	TE	3342.5	-537	244	VREF	6392.5	-537	294	G<8>	8887.5	500
195	CL1	3427.5	-537	245	VREF	6452.5	-537	295	G<10>	8872.5	344
196	TEST_DUMMY	3512.5	-537	246	VDD3	6512.5	-537	296	G<12>	8857.5	500
197	TMODE<2>	3572.5	-537	247	VDD3	6572.5	-537	297	G<14>	8842.5	344
198	TMODE<1>	3632.5	-537	248	VDD3	6632.5	-537	298	G<16>	8827.5	500
199	TMODE<0>	3692.5	-537	249	VDD3	6692.5	-537	299	G<18>	8812.5	344
200	TMUX<2>	3752.5	-537	250	VDD3	6752.5	-537	300	G<20>	8797.5	500

Note. Contact3 and Contact4 pins show ground potential during power-on status.

NO	Name	X	Y	NO	Name	X	Y	NO	Name	X	Y
301	G<22>	8782.5	344	351	G<122>	8032.5	344	401	G<222>	7282.5	344
302	G<24>	8767.5	500	352	G<124>	8017.5	500	402	G<224>	7267.5	500
303	G<26>	8752.5	344	353	G<126>	8002.5	344	403	G<226>	7252.5	344
304	G<28>	8737.5	500	354	G<128>	7987.5	500	404	G<228>	7237.5	500
305	G<30>	8722.5	344	355	G<130>	7972.5	344	405	G<230>	7222.5	344
306	G<32>	8707.5	500	356	G<132>	7957.5	500	406	G<232>	7207.5	500
307	G<34>	8692.5	344	357	G<134>	7942.5	344	407	G<234>	7192.5	344
308	G<36>	8677.5	500	358	G<136>	7927.5	500	408	G<236>	7177.5	500
309	G<38>	8662.5	344	359	G<138>	7912.5	344	409	G<238>	7162.5	344
310	G<40>	8647.5	500	360	G<140>	7897.5	500	410	G<240>	7147.5	500
311	G<42>	8632.5	344	361	G<142>	7882.5	344	411	G<242>	7132.5	344
312	G<44>	8617.5	500	362	G<144>	7867.5	500	412	G<244>	7117.5	500
313	G<46>	8602.5	344	363	G<146>	7852.5	344	413	G<246>	7102.5	344
314	G<48>	8587.5	500	364	G<148>	7837.5	500	414	G<248>	7087.5	500
315	G<50>	8572.5	344	365	G<150>	7822.5	344	415	G<250>	7072.5	344
316	G<52>	8557.5	500	366	G<152>	7807.5	500	416	G<252>	7057.5	500
317	G<54>	8542.5	344	367	G<154>	7792.5	344	417	G<254>	7042.5	344
318	G<56>	8527.5	500	368	G<156>	7777.5	500	418	G<256>	7027.5	500
319	G<58>	8512.5	344	369	G<158>	7762.5	344	419	G<258>	7012.5	344
320	G<60>	8497.5	500	370	G<160>	7747.5	500	420	G<260>	6997.5	500
321	G<62>	8482.5	344	371	G<162>	7732.5	344	421	G<262>	6982.5	344
322	G<64>	8467.5	500	372	G<164>	7717.5	500	422	G<264>	6967.5	500
323	G<66>	8452.5	344	373	G<166>	7702.5	344	423	G<266>	6952.5	344
324	G<68>	8437.5	500	374	G<168>	7687.5	500	424	G<268>	6937.5	500
325	G<70>	8422.5	344	375	G<170>	7672.5	344	425	G<270>	6922.5	344
326	G<72>	8407.5	500	376	G<172>	7657.5	500	426	G<272>	6907.5	500
327	G<74>	8392.5	344	377	G<174>	7642.5	344	427	G<274>	6892.5	344
328	G<76>	8377.5	500	378	G<176>	7627.5	500	428	G<276>	6877.5	500
329	G<78>	8362.5	344	379	G<178>	7612.5	344	429	G<278>	6862.5	344
330	G<80>	8347.5	500	380	G<180>	7597.5	500	430	G<280>	6847.5	500
331	G<82>	8332.5	344	381	G<182>	7582.5	344	431	G<282>	6832.5	344
332	G<84>	8317.5	500	382	G<184>	7567.5	500	432	G<284>	6817.5	500
333	G<86>	8302.5	344	383	G<186>	7552.5	344	433	G<286>	6802.5	344
334	G<88>	8287.5	500	384	G<188>	7537.5	500	434	G<288>	6787.5	500
335	G<90>	8272.5	344	385	G<190>	7522.5	344	435	G<290>	6772.5	344
336	G<92>	8257.5	500	386	G<192>	7507.5	500	436	G<292>	6757.5	500
337	G<94>	8242.5	344	387	G<194>	7492.5	344	437	G<294>	6742.5	344
338	G<96>	8227.5	500	388	G<196>	7477.5	500	438	G<296>	6727.5	500
339	G<98>	8212.5	344	389	G<198>	7462.5	344	439	G<298>	6712.5	344
340	G<100>	8197.5	500	390	G<200>	7447.5	500	440	G<300>	6697.5	500
341	G<102>	8182.5	344	391	G<202>	7432.5	344	441	G<302>	6682.5	344
342	G<104>	8167.5	500	392	G<204>	7417.5	500	442	G<304>	6667.5	500
343	G<106>	8152.5	344	393	G<206>	7402.5	344	443	G<306>	6652.5	344
344	G<108>	8137.5	500	394	G<208>	7387.5	500	444	G<308>	6637.5	500
345	G<110>	8122.5	344	395	G<210>	7372.5	344	445	G<310>	6622.5	344
346	G<112>	8107.5	500	396	G<212>	7357.5	500	446	G<312>	6607.5	500
347	G<114>	8092.5	344	397	G<214>	7342.5	344	447	G<314>	6592.5	344
348	G<116>	8077.5	500	398	G<216>	7327.5	500	448	G<316>	6577.5	500
349	G<118>	8062.5	344	399	G<218>	7312.5	344	449	G<318>	6562.5	344
350	G<120>	8047.5	500	400	G<220>	7297.5	500	450	G<320>	6547.5	500

NO	Name	X	Y	NO	Name	X	Y	NO	Name	X	Y
451	G<322>	6532.5	344	501	G<422>	5782.5	344	551	S<692>	4972.5	344
452	G<324>	6517.5	500	502	G<424>	5767.5	500	552	S<691>	4957.5	500
453	G<326>	6502.5	344	503	G<426>	5752.5	344	553	S<690>	4942.5	344
454	G<328>	6487.5	500	504	G<428>	5737.5	500	554	S<689>	4927.5	500
455	G<330>	6472.5	344	505	G<430>	5722.5	344	555	S<688>	4912.5	344
456	G<332>	6457.5	500	506	G<432>	5707.5	500	556	S<687>	4897.5	500
457	G<334>	6442.5	344	507	DUMMY<21>	5692.5	344	557	S<686>	4882.5	344
458	G<336>	6427.5	500	508	DUMMY<22>	5677.5	500	558	S<685>	4867.5	500
459	G<338>	6412.5	344	509	DUMMY<23>	5662.5	344	559	S<684>	4852.5	344
460	G<340>	6397.5	500	510	DUMMY<24>	5647.5	500	560	S<683>	4837.5	500
461	G<342>	6382.5	344	511	DUMMY<25>	5632.5	344	561	S<682>	4822.5	344
462	G<344>	6367.5	500	512	DUMMY<26>	5617.5	500	562	S<681>	4807.5	500
463	G<346>	6352.5	344	513	DUMMY<27>	5602.5	344	563	S<680>	4792.5	344
464	G<348>	6337.5	500	514	DUMMY<28>	5587.5	500	564	S<679>	4777.5	500
465	G<350>	6322.5	344	515	DUMMY<29>	5512.5	344	565	S<678>	4762.5	344
466	G<352>	6307.5	500	516	DUMMY<30>	5497.5	500	566	S<677>	4747.5	500
467	G<354>	6292.5	344	517	DUMMY<31>	5482.5	344	567	S<676>	4732.5	344
468	G<356>	6277.5	500	518	DUMMY<32>	5467.5	500	568	S<675>	4717.5	500
469	G<358>	6262.5	344	519	DUMMY<33>	5452.5	344	569	S<674>	4702.5	344
470	G<360>	6247.5	500	520	DUMMY<34>	5437.5	500	570	S<673>	4687.5	500
471	G<362>	6232.5	344	521	DUMMY<35>	5422.5	344	571	S<672>	4672.5	344
472	G<364>	6217.5	500	522	DUMMY<36>	5407.5	500	572	S<671>	4657.5	500
473	G<366>	6202.5	344	523	S<720>	5392.5	344	573	S<670>	4642.5	344
474	G<368>	6187.5	500	524	S<719>	5377.5	500	574	S<669>	4627.5	500
475	G<370>	6172.5	344	525	S<718>	5362.5	344	575	S<668>	4612.5	344
476	G<372>	6157.5	500	526	S<717>	5347.5	500	576	S<667>	4597.5	500
477	G<374>	6142.5	344	527	S<716>	5332.5	344	577	S<666>	4582.5	344
478	G<376>	6127.5	500	528	S<715>	5317.5	500	578	S<665>	4567.5	500
479	G<378>	6112.5	344	529	S<714>	5302.5	344	579	S<664>	4552.5	344
480	G<380>	6097.5	500	530	S<713>	5287.5	500	580	S<663>	4537.5	500
481	G<382>	6082.5	344	531	S<712>	5272.5	344	581	S<662>	4522.5	344
482	G<384>	6067.5	500	532	S<711>	5257.5	500	582	S<661>	4507.5	500
483	G<386>	6052.5	344	533	S<710>	5242.5	344	583	S<660>	4492.5	344
484	G<388>	6037.5	500	534	S<709>	5227.5	500	584	S<659>	4477.5	500
485	G<390>	6022.5	344	535	S<708>	5212.5	344	585	S<658>	4462.5	344
486	G<392>	6007.5	500	536	S<707>	5197.5	500	586	S<657>	4447.5	500
487	G<394>	5992.5	344	537	S<706>	5182.5	344	587	S<656>	4432.5	344
488	G<396>	5977.5	500	538	S<705>	5167.5	500	588	S<655>	4417.5	500
489	G<398>	5962.5	344	539	S<704>	5152.5	344	589	S<654>	4402.5	344
490	G<400>	5947.5	500	540	S<703>	5137.5	500	590	S<653>	4387.5	500
491	G<402>	5932.5	344	541	S<702>	5122.5	344	591	S<652>	4372.5	344
492	G<404>	5917.5	500	542	S<701>	5107.5	500	592	S<651>	4357.5	500
493	G<406>	5902.5	344	543	S<700>	5092.5	344	593	S<650>	4342.5	344
494	G<408>	5887.5	500	544	S<699>	5077.5	500	594	S<649>	4327.5	500
495	G<410>	5872.5	344	545	S<698>	5062.5	344	595	S<648>	4312.5	344
496	G<412>	5857.5	500	546	S<697>	5047.5	500	596	S<647>	4297.5	500
497	G<414>	5842.5	344	547	S<696>	5032.5	344	597	S<646>	4282.5	344
498	G<416>	5827.5	500	548	S<695>	5017.5	500	598	S<645>	4267.5	500
499	G<418>	5812.5	344	549	S<694>	5002.5	344	599	S<644>	4252.5	344
500	G<420>	5797.5	500	550	S<693>	4987.5	500	600	S<643>	4237.5	500

Note. DUMMY<36:21> pins between gate and source show floating state during normal operating condition.

NO	Name	X	Y	NO	Name	X	Y	NO	Name	X	Y
601	S<642>	4222.5	344	651	S<592>	3472.5	344	701	S<542>	2722.5	344
602	S<641>	4207.5	500	652	S<591>	3457.5	500	702	S<541>	2707.5	500
603	S<640>	4192.5	344	653	S<590>	3442.5	344	703	S<540>	2692.5	344
604	S<639>	4177.5	500	654	S<589>	3427.5	500	704	S<539>	2677.5	500
605	S<638>	4162.5	344	655	S<588>	3412.5	344	705	S<538>	2662.5	344
606	S<637>	4147.5	500	656	S<587>	3397.5	500	706	S<537>	2647.5	500
607	S<636>	4132.5	344	657	S<586>	3382.5	344	707	S<536>	2632.5	344
608	S<635>	4117.5	500	658	S<585>	3367.5	500	708	S<535>	2617.5	500
609	S<634>	4102.5	344	659	S<584>	3352.5	344	709	S<534>	2602.5	344
610	S<633>	4087.5	500	660	S<583>	3337.5	500	710	S<533>	2587.5	500
611	S<632>	4072.5	344	661	S<582>	3322.5	344	711	S<532>	2572.5	344
612	S<631>	4057.5	500	662	S<581>	3307.5	500	712	S<531>	2557.5	500
613	S<630>	4042.5	344	663	S<580>	3292.5	344	713	S<530>	2542.5	344
614	S<629>	4027.5	500	664	S<579>	3277.5	500	714	S<529>	2527.5	500
615	S<628>	4012.5	344	665	S<578>	3262.5	344	715	S<528>	2512.5	344
616	S<627>	3997.5	500	666	S<577>	3247.5	500	716	S<527>	2497.5	500
617	S<626>	3982.5	344	667	S<576>	3232.5	344	717	S<526>	2482.5	344
618	S<625>	3967.5	500	668	S<575>	3217.5	500	718	S<525>	2467.5	500
619	S<624>	3952.5	344	669	S<574>	3202.5	344	719	S<524>	2452.5	344
620	S<623>	3937.5	500	670	S<573>	3187.5	500	720	S<523>	2437.5	500
621	S<622>	3922.5	344	671	S<572>	3172.5	344	721	S<522>	2422.5	344
622	S<621>	3907.5	500	672	S<571>	3157.5	500	722	S<521>	2407.5	500
623	S<620>	3892.5	344	673	S<570>	3142.5	344	723	S<520>	2392.5	344
624	S<619>	3877.5	500	674	S<569>	3127.5	500	724	S<519>	2377.5	500
625	S<618>	3862.5	344	675	S<568>	3112.5	344	725	S<518>	2362.5	344
626	S<617>	3847.5	500	676	S<567>	3097.5	500	726	S<517>	2347.5	500
627	S<616>	3832.5	344	677	S<566>	3082.5	344	727	S<516>	2332.5	344
628	S<615>	3817.5	500	678	S<565>	3067.5	500	728	S<515>	2317.5	500
629	S<614>	3802.5	344	679	S<564>	3052.5	344	729	S<514>	2302.5	344
630	S<613>	3787.5	500	680	S<563>	3037.5	500	730	S<513>	2287.5	500
631	S<612>	3772.5	344	681	S<562>	3022.5	344	731	S<512>	2272.5	344
632	S<611>	3757.5	500	682	S<561>	3007.5	500	732	S<511>	2257.5	500
633	S<610>	3742.5	344	683	S<560>	2992.5	344	733	S<510>	2242.5	344
634	S<609>	3727.5	500	684	S<559>	2977.5	500	734	S<509>	2227.5	500
635	S<608>	3712.5	344	685	S<558>	2962.5	344	735	S<508>	2212.5	344
636	S<607>	3697.5	500	686	S<557>	2947.5	500	736	S<507>	2197.5	500
637	S<606>	3682.5	344	687	S<556>	2932.5	344	737	S<506>	2182.5	344
638	S<605>	3667.5	500	688	S<555>	2917.5	500	738	S<505>	2167.5	500
639	S<604>	3652.5	344	689	S<554>	2902.5	344	739	S<504>	2152.5	344
640	S<603>	3637.5	500	690	S<553>	2887.5	500	740	S<503>	2137.5	500
641	S<602>	3622.5	344	691	S<552>	2872.5	344	741	S<502>	2122.5	344
642	S<601>	3607.5	500	692	S<551>	2857.5	500	742	S<501>	2107.5	500
643	S<600>	3592.5	344	693	S<550>	2842.5	344	743	S<500>	2092.5	344
644	S<599>	3577.5	500	694	S<549>	2827.5	500	744	S<499>	2077.5	500
645	S<598>	3562.5	344	695	S<548>	2812.5	344	745	S<498>	2062.5	344
646	S<597>	3547.5	500	696	S<547>	2797.5	500	746	S<497>	2047.5	500
647	S<596>	3532.5	344	697	S<546>	2782.5	344	747	S<496>	2032.5	344
648	S<595>	3517.5	500	698	S<545>	2767.5	500	748	S<495>	2017.5	500
649	S<594>	3502.5	344	699	S<544>	2752.5	344	749	S<494>	2002.5	344
650	S<593>	3487.5	500	700	S<543>	2737.5	500	750	S<493>	1987.5	500

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752	S<491>	1957.5	500	802	S<441>	1207.5	500	852	S<391>	457.5	500
753	S<490>	1942.5	344	803	S<440>	1192.5	344	853	S<390>	442.5	344
754	S<489>	1927.5	500	804	S<439>	1177.5	500	854	S<389>	427.5	500
755	S<488>	1912.5	344	805	S<438>	1162.5	344	855	S<388>	412.5	344
756	S<487>	1897.5	500	806	S<437>	1147.5	500	856	S<387>	397.5	500
757	S<486>	1882.5	344	807	S<436>	1132.5	344	857	S<386>	382.5	344
758	S<485>	1867.5	500	808	S<435>	1117.5	500	858	S<385>	367.5	500
759	S<484>	1852.5	344	809	S<434>	1102.5	344	859	S<384>	352.5	344
760	S<483>	1837.5	500	810	S<433>	1087.5	500	860	S<383>	337.5	500
761	S<482>	1822.5	344	811	S<432>	1072.5	344	861	S<382>	322.5	344
762	S<481>	1807.5	500	812	S<431>	1057.5	500	862	S<381>	307.5	500
763	S<480>	1792.5	344	813	S<430>	1042.5	344	863	S<380>	292.5	344
764	S<479>	1777.5	500	814	S<429>	1027.5	500	864	S<379>	277.5	500
765	S<478>	1762.5	344	815	S<428>	1012.5	344	865	S<378>	262.5	344
766	S<477>	1747.5	500	816	S<427>	997.5	500	866	S<377>	247.5	500
767	S<476>	1732.5	344	817	S<426>	982.5	344	867	S<376>	232.5	344
768	S<475>	1717.5	500	818	S<425>	967.5	500	868	S<375>	217.5	500
769	S<474>	1702.5	344	819	S<424>	952.5	344	869	S<374>	202.5	344
770	S<473>	1687.5	500	820	S<423>	937.5	500	870	S<373>	187.5	500
771	S<472>	1672.5	344	821	S<422>	922.5	344	871	S<372>	172.5	344
772	S<471>	1657.5	500	822	S<421>	907.5	500	872	S<371>	157.5	500
773	S<470>	1642.5	344	823	S<420>	892.5	344	873	S<370>	142.5	344
774	S<469>	1627.5	500	824	S<419>	877.5	500	874	S<369>	127.5	500
775	S<468>	1612.5	344	825	S<418>	862.5	344	875	S<368>	112.5	344
776	S<467>	1597.5	500	826	S<417>	847.5	500	876	S<367>	97.5	500
777	S<466>	1582.5	344	827	S<416>	832.5	344	877	S<366>	82.5	344
778	S<465>	1567.5	500	828	S<415>	817.5	500	878	S<365>	67.5	500
779	S<464>	1552.5	344	829	S<414>	802.5	344	879	S<364>	52.5	344
780	S<463>	1537.5	500	830	S<413>	787.5	500	880	S<363>	37.5	500
781	S<462>	1522.5	344	831	S<412>	772.5	344	881	S<362>	22.5	344
782	S<461>	1507.5	500	832	S<411>	757.5	500	882	S<361>	7.5	500
783	S<460>	1492.5	344	833	S<410>	742.5	344	883	S<360>	-7.5	344
784	S<459>	1477.5	500	834	S<409>	727.5	500	884	S<359>	-22.5	500
785	S<458>	1462.5	344	835	S<408>	712.5	344	885	S<358>	-37.5	344
786	S<457>	1447.5	500	836	S<407>	697.5	500	886	S<357>	-52.5	500
787	S<456>	1432.5	344	837	S<406>	682.5	344	887	S<356>	-67.5	344
788	S<455>	1417.5	500	838	S<405>	667.5	500	888	S<355>	-82.5	500
789	S<454>	1402.5	344	839	S<404>	652.5	344	889	S<354>	-97.5	344
790	S<453>	1387.5	500	840	S<403>	637.5	500	890	S<353>	-112.5	500
791	S<452>	1372.5	344	841	S<402>	622.5	344	891	S<352>	-127.5	344
792	S<451>	1357.5	500	842	S<401>	607.5	500	892	S<351>	-142.5	500
793	S<450>	1342.5	344	843	S<400>	592.5	344	893	S<350>	-157.5	344
794	S<449>	1327.5	500	844	S<399>	577.5	500	894	S<349>	-172.5	500
795	S<448>	1312.5	344	845	S<398>	562.5	344	895	S<348>	-187.5	344
796	S<447>	1297.5	500	846	S<397>	547.5	500	896	S<347>	-202.5	500
797	S<446>	1282.5	344	847	S<396>	532.5	344	897	S<346>	-217.5	344
798	S<445>	1267.5	500	848	S<395>	517.5	500	898	S<345>	-232.5	500
799	S<444>	1252.5	344	849	S<394>	502.5	344	899	S<344>	-247.5	344
800	S<443>	1237.5	500	850	S<393>	487.5	500	900	S<343>	-262.5	500

NO	Name	X	Y	NO	Name	X	Y	NO	Name	X	Y
901	S<342>	-277.5	344	951	S<292>	-1027.5	344	1001	S<242>	-1777.5	344
902	S<341>	-292.5	500	952	S<291>	-1042.5	500	1002	S<241>	-1792.5	500
903	S<340>	-307.5	344	953	S<290>	-1057.5	344	1003	S<240>	-1807.5	344
904	S<339>	-322.5	500	954	S<289>	-1072.5	500	1004	S<239>	-1822.5	500
905	S<338>	-337.5	344	955	S<288>	-1087.5	344	1005	S<238>	-1837.5	344
906	S<337>	-352.5	500	956	S<287>	-1102.5	500	1006	S<237>	-1852.5	500
907	S<336>	-367.5	344	957	S<286>	-1117.5	344	1007	S<236>	-1867.5	344
908	S<335>	-382.5	500	958	S<285>	-1132.5	500	1008	S<235>	-1882.5	500
909	S<334>	-397.5	344	959	S<284>	-1147.5	344	1009	S<234>	-1897.5	344
910	S<333>	-412.5	500	960	S<283>	-1162.5	500	1010	S<233>	-1912.5	500
911	S<332>	-427.5	344	961	S<282>	-1177.5	344	1011	S<232>	-1927.5	344
912	S<331>	-442.5	500	962	S<281>	-1192.5	500	1012	S<231>	-1942.5	500
913	S<330>	-457.5	344	963	S<280>	-1207.5	344	1013	S<230>	-1957.5	344
914	S<329>	-472.5	500	964	S<279>	-1222.5	500	1014	S<229>	-1972.5	500
915	S<328>	-487.5	344	965	S<278>	-1237.5	344	1015	S<228>	-1987.5	344
916	S<327>	-502.5	500	966	S<277>	-1252.5	500	1016	S<227>	-2002.5	500
917	S<326>	-517.5	344	967	S<276>	-1267.5	344	1017	S<226>	-2017.5	344
918	S<325>	-532.5	500	968	S<275>	-1282.5	500	1018	S<225>	-2032.5	500
919	S<324>	-547.5	344	969	S<274>	-1297.5	344	1019	S<224>	-2047.5	344
920	S<323>	-562.5	500	970	S<273>	-1312.5	500	1020	S<223>	-2062.5	500
921	S<322>	-577.5	344	971	S<272>	-1327.5	344	1021	S<222>	-2077.5	344
922	S<321>	-592.5	500	972	S<271>	-1342.5	500	1022	S<221>	-2092.5	500
923	S<320>	-607.5	344	973	S<270>	-1357.5	344	1023	S<220>	-2107.5	344
924	S<319>	-622.5	500	974	S<269>	-1372.5	500	1024	S<219>	-2122.5	500
925	S<318>	-637.5	344	975	S<268>	-1387.5	344	1025	S<218>	-2137.5	344
926	S<317>	-652.5	500	976	S<267>	-1402.5	500	1026	S<217>	-2152.5	500
927	S<316>	-667.5	344	977	S<266>	-1417.5	344	1027	S<216>	-2167.5	344
928	S<315>	-682.5	500	978	S<265>	-1432.5	500	1028	S<215>	-2182.5	500
929	S<314>	-697.5	344	979	S<264>	-1447.5	344	1029	S<214>	-2197.5	344
930	S<313>	-712.5	500	980	S<263>	-1462.5	500	1030	S<213>	-2212.5	500
931	S<312>	-727.5	344	981	S<262>	-1477.5	344	1031	S<212>	-2227.5	344
932	S<311>	-742.5	500	982	S<261>	-1492.5	500	1032	S<211>	-2242.5	500
933	S<310>	-757.5	344	983	S<260>	-1507.5	344	1033	S<210>	-2257.5	344
934	S<309>	-772.5	500	984	S<259>	-1522.5	500	1034	S<209>	-2272.5	500
935	S<308>	-787.5	344	985	S<258>	-1537.5	344	1035	S<208>	-2287.5	344
936	S<307>	-802.5	500	986	S<257>	-1552.5	500	1036	S<207>	-2302.5	500
937	S<306>	-817.5	344	987	S<256>	-1567.5	344	1037	S<206>	-2317.5	344
938	S<305>	-832.5	500	988	S<255>	-1582.5	500	1038	S<205>	-2332.5	500
939	S<304>	-847.5	344	989	S<254>	-1597.5	344	1039	S<204>	-2347.5	344
940	S<303>	-862.5	500	990	S<253>	-1612.5	500	1040	S<203>	-2362.5	500
941	S<302>	-877.5	344	991	S<252>	-1627.5	344	1041	S<202>	-2377.5	344
942	S<301>	-892.5	500	992	S<251>	-1642.5	500	1042	S<201>	-2392.5	500
943	S<300>	-907.5	344	993	S<250>	-1657.5	344	1043	S<200>	-2407.5	344
944	S<299>	-922.5	500	994	S<249>	-1672.5	500	1044	S<199>	-2422.5	500
945	S<298>	-937.5	344	995	S<248>	-1687.5	344	1045	S<198>	-2437.5	344
946	S<297>	-952.5	500	996	S<247>	-1702.5	500	1046	S<197>	-2452.5	500
947	S<296>	-967.5	344	997	S<246>	-1717.5	344	1047	S<196>	-2467.5	344
948	S<295>	-982.5	500	998	S<245>	-1732.5	500	1048	S<195>	-2482.5	500
949	S<294>	-997.5	344	999	S<244>	-1747.5	344	1049	S<194>	-2497.5	344
950	S<293>	-1012.5	500	1000	S<243>	-1762.5	500	1050	S<193>	-2512.5	500

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1052	S<191>	-2542.5	500	1102	S<141>	-3292.5	500	1152	S<91>	-4042.5	500
1053	S<190>	-2557.5	344	1103	S<140>	-3307.5	344	1153	S<90>	-4057.5	344
1054	S<189>	-2572.5	500	1104	S<139>	-3322.5	500	1154	S<89>	-4072.5	500
1055	S<188>	-2587.5	344	1105	S<138>	-3337.5	344	1155	S<88>	-4087.5	344
1056	S<187>	-2602.5	500	1106	S<137>	-3352.5	500	1156	S<87>	-4102.5	500
1057	S<186>	-2617.5	344	1107	S<136>	-3367.5	344	1157	S<86>	-4117.5	344
1058	S<185>	-2632.5	500	1108	S<135>	-3382.5	500	1158	S<85>	-4132.5	500
1059	S<184>	-2647.5	344	1109	S<134>	-3397.5	344	1159	S<84>	-4147.5	344
1060	S<183>	-2662.5	500	1110	S<133>	-3412.5	500	1160	S<83>	-4162.5	500
1061	S<182>	-2677.5	344	1111	S<132>	-3427.5	344	1161	S<82>	-4177.5	344
1062	S<181>	-2692.5	500	1112	S<131>	-3442.5	500	1162	S<81>	-4192.5	500
1063	S<180>	-2707.5	344	1113	S<130>	-3457.5	344	1163	S<80>	-4207.5	344
1064	S<179>	-2722.5	500	1114	S<129>	-3472.5	500	1164	S<79>	-4222.5	500
1065	S<178>	-2737.5	344	1115	S<128>	-3487.5	344	1165	S<78>	-4237.5	344
1066	S<177>	-2752.5	500	1116	S<127>	-3502.5	500	1166	S<77>	-4252.5	500
1067	S<176>	-2767.5	344	1117	S<126>	-3517.5	344	1167	S<76>	-4267.5	344
1068	S<175>	-2782.5	500	1118	S<125>	-3532.5	500	1168	S<75>	-4282.5	500
1069	S<174>	-2797.5	344	1119	S<124>	-3547.5	344	1169	S<74>	-4297.5	344
1070	S<173>	-2812.5	500	1120	S<123>	-3562.5	500	1170	S<73>	-4312.5	500
1071	S<172>	-2827.5	344	1121	S<122>	-3577.5	344	1171	S<72>	-4327.5	344
1072	S<171>	-2842.5	500	1122	S<121>	-3592.5	500	1172	S<71>	-4342.5	500
1073	S<170>	-2857.5	344	1123	S<120>	-3607.5	344	1173	S<70>	-4357.5	344
1074	S<169>	-2872.5	500	1124	S<119>	-3622.5	500	1174	S<69>	-4372.5	500
1075	S<168>	-2887.5	344	1125	S<118>	-3637.5	344	1175	S<68>	-4387.5	344
1076	S<167>	-2902.5	500	1126	S<117>	-3652.5	500	1176	S<67>	-4402.5	500
1077	S<166>	-2917.5	344	1127	S<116>	-3667.5	344	1177	S<66>	-4417.5	344
1078	S<165>	-2932.5	500	1128	S<115>	-3682.5	500	1178	S<65>	-4432.5	500
1079	S<164>	-2947.5	344	1129	S<114>	-3697.5	344	1179	S<64>	-4447.5	344
1080	S<163>	-2962.5	500	1130	S<113>	-3712.5	500	1180	S<63>	-4462.5	500
1081	S<162>	-2977.5	344	1131	S<112>	-3727.5	344	1181	S<62>	-4477.5	344
1082	S<161>	-2992.5	500	1132	S<111>	-3742.5	500	1182	S<61>	-4492.5	500
1083	S<160>	-3007.5	344	1133	S<110>	-3757.5	344	1183	S<60>	-4507.5	344
1084	S<159>	-3022.5	500	1134	S<109>	-3772.5	500	1184	S<59>	-4522.5	500
1085	S<158>	-3037.5	344	1135	S<108>	-3787.5	344	1185	S<58>	-4537.5	344
1086	S<157>	-3052.5	500	1136	S<107>	-3802.5	500	1186	S<57>	-4552.5	500
1087	S<156>	-3067.5	344	1137	S<106>	-3817.5	344	1187	S<56>	-4567.5	344
1088	S<155>	-3082.5	500	1138	S<105>	-3832.5	500	1188	S<55>	-4582.5	500
1089	S<154>	-3097.5	344	1139	S<104>	-3847.5	344	1189	S<54>	-4597.5	344
1090	S<153>	-3112.5	500	1140	S<103>	-3862.5	500	1190	S<53>	-4612.5	500
1091	S<152>	-3127.5	344	1141	S<102>	-3877.5	344	1191	S<52>	-4627.5	344
1092	S<151>	-3142.5	500	1142	S<101>	-3892.5	500	1192	S<51>	-4642.5	500
1093	S<150>	-3157.5	344	1143	S<100>	-3907.5	344	1193	S<50>	-4657.5	344
1094	S<149>	-3172.5	500	1144	S<99>	-3922.5	500	1194	S<49>	-4672.5	500
1095	S<148>	-3187.5	344	1145	S<98>	-3937.5	344	1195	S<48>	-4687.5	344
1096	S<147>	-3202.5	500	1146	S<97>	-3952.5	500	1196	S<47>	-4702.5	500
1097	S<146>	-3217.5	344	1147	S<96>	-3967.5	344	1197	S<46>	-4717.5	344
1098	S<145>	-3232.5	500	1148	S<95>	-3982.5	500	1198	S<45>	-4732.5	500
1099	S<144>	-3247.5	344	1149	S<94>	-3997.5	344	1199	S<44>	-4747.5	344
1100	S<143>	-3262.5	500	1150	S<93>	-4012.5	500	1200	S<43>	-4762.5	500

NO	Name	X	Y	NO	Name	X	Y	NO	Name	X	Y
1201	S<42>	-4777.5	344	1251	DUMMY<45>	-5587.5	344	1301	G<347>	-6337.5	344
1202	S<41>	-4792.5	500	1252	DUMMY<46>	-5602.5	500	1302	G<345>	-6352.5	500
1203	S<40>	-4807.5	344	1253	DUMMY<47>	-5617.5	344	1303	G<343>	-6367.5	344
1204	S<39>	-4822.5	500	1254	DUMMY<48>	-5632.5	500	1304	G<341>	-6382.5	500
1205	S<38>	-4837.5	344	1255	DUMMY<49>	-5647.5	344	1305	G<339>	-6397.5	344
1206	S<37>	-4852.5	500	1256	DUMMY<50>	-5662.5	500	1306	G<337>	-6412.5	500
1207	S<36>	-4867.5	344	1257	DUMMY<51>	-5677.5	344	1307	G<335>	-6427.5	344
1208	S<35>	-4882.5	500	1258	DUMMY<52>	-5692.5	500	1308	G<333>	-6442.5	500
1209	S<34>	-4897.5	344	1259	G<431>	-5707.5	344	1309	G<331>	-6457.5	344
1210	S<33>	-4912.5	500	1260	G<429>	-5722.5	500	1310	G<329>	-6472.5	500
1211	S<32>	-4927.5	344	1261	G<427>	-5737.5	344	1311	G<327>	-6487.5	344
1212	S<31>	-4942.5	500	1262	G<425>	-5752.5	500	1312	G<325>	-6502.5	500
1213	S<30>	-4957.5	344	1263	G<423>	-5767.5	344	1313	G<323>	-6517.5	344
1214	S<29>	-4972.5	500	1264	G<421>	-5782.5	500	1314	G<321>	-6532.5	500
1215	S<28>	-4987.5	344	1265	G<419>	-5797.5	344	1315	G<319>	-6547.5	344
1216	S<27>	-5002.5	500	1266	G<417>	-5812.5	500	1316	G<317>	-6562.5	500
1217	S<26>	-5017.5	344	1267	G<415>	-5827.5	344	1317	G<315>	-6577.5	344
1218	S<25>	-5032.5	500	1268	G<413>	-5842.5	500	1318	G<313>	-6592.5	500
1219	S<24>	-5047.5	344	1269	G<411>	-5857.5	344	1319	G<311>	-6607.5	344
1220	S<23>	-5062.5	500	1270	G<409>	-5872.5	500	1320	G<309>	-6622.5	500
1221	S<22>	-5077.5	344	1271	G<407>	-5887.5	344	1321	G<307>	-6637.5	344
1222	S<21>	-5092.5	500	1272	G<405>	-5902.5	500	1322	G<305>	-6652.5	500
1223	S<20>	-5107.5	344	1273	G<403>	-5917.5	344	1323	G<303>	-6667.5	344
1224	S<19>	-5122.5	500	1274	G<401>	-5932.5	500	1324	G<301>	-6682.5	500
1225	S<18>	-5137.5	344	1275	G<399>	-5947.5	344	1325	G<299>	-6697.5	344
1226	S<17>	-5152.5	500	1276	G<397>	-5962.5	500	1326	G<297>	-6712.5	500
1227	S<16>	-5167.5	344	1277	G<395>	-5977.5	344	1327	G<295>	-6727.5	344
1228	S<15>	-5182.5	500	1278	G<393>	-5992.5	500	1328	G<293>	-6742.5	500
1229	S<14>	-5197.5	344	1279	G<391>	-6007.5	344	1329	G<291>	-6757.5	344
1230	S<13>	-5212.5	500	1280	G<389>	-6022.5	500	1330	G<289>	-6772.5	500
1231	S<12>	-5227.5	344	1281	G<387>	-6037.5	344	1331	G<287>	-6787.5	344
1232	S<11>	-5242.5	500	1282	G<385>	-6052.5	500	1332	G<285>	-6802.5	500
1233	S<10>	-5257.5	344	1283	G<383>	-6067.5	344	1333	G<283>	-6817.5	344
1234	S<9>	-5272.5	500	1284	G<381>	-6082.5	500	1334	G<281>	-6832.5	500
1235	S<8>	-5287.5	344	1285	G<379>	-6097.5	344	1335	G<279>	-6847.5	344
1236	S<7>	-5302.5	500	1286	G<377>	-6112.5	500	1336	G<277>	-6862.5	500
1237	S<6>	-5317.5	344	1287	G<375>	-6127.5	344	1337	G<275>	-6877.5	344
1238	S<5>	-5332.5	500	1288	G<373>	-6142.5	500	1338	G<273>	-6892.5	500
1239	S<4>	-5347.5	344	1289	G<371>	-6157.5	344	1339	G<271>	-6907.5	344
1240	S<3>	-5362.5	500	1290	G<369>	-6172.5	500	1340	G<269>	-6922.5	500
1241	S<2>	-5377.5	344	1291	G<367>	-6187.5	344	1341	G<267>	-6937.5	344
1242	S<1>	-5392.5	500	1292	G<365>	-6202.5	500	1342	G<265>	-6952.5	500
1243	DUMMY<37>	-5407.5	344	1293	G<363>	-6217.5	344	1343	G<263>	-6967.5	344
1244	DUMMY<38>	-5422.5	500	1294	G<361>	-6232.5	500	1344	G<261>	-6982.5	500
1245	DUMMY<39>	-5437.5	344	1295	G<359>	-6247.5	344	1345	G<259>	-6997.5	344
1246	DUMMY<40>	-5452.5	500	1296	G<357>	-6262.5	500	1346	G<257>	-7012.5	500
1247	DUMMY<41>	-5467.5	344	1297	G<355>	-6277.5	344	1347	G<255>	-7027.5	344
1248	DUMMY<42>	-5482.5	500	1298	G<353>	-6292.5	500	1348	G<253>	-7042.5	500
1249	DUMMY<43>	-5497.5	344	1299	G<351>	-6307.5	344	1349	G<251>	-7057.5	344
1250	DUMMY<44>	-5512.5	500	1300	G<349>	-6322.5	500	1350	G<249>	-7072.5	500

Note. DUMMY<52:37> pins between gate and source show floating state during normal operating condition.

NO	Name	X	Y	NO	Name	X	Y	NO	Name	X	Y
1351	G<247>	-7087.5	344	1401	G<147>	-7837.5	344	1451	G<47>	-8587.5	344
1352	G<245>	-7102.5	500	1402	G<145>	-7852.5	500	1452	G<45>	-8602.5	500
1353	G<243>	-7117.5	344	1403	G<143>	-7867.5	344	1453	G<43>	-8617.5	344
1354	G<241>	-7132.5	500	1404	G<141>	-7882.5	500	1454	G<41>	-8632.5	500
1355	G<239>	-7147.5	344	1405	G<139>	-7897.5	344	1455	G<39>	-8647.5	344
1356	G<237>	-7162.5	500	1406	G<137>	-7912.5	500	1456	G<37>	-8662.5	500
1357	G<235>	-7177.5	344	1407	G<135>	-7927.5	344	1457	G<35>	-8677.5	344
1358	G<233>	-7192.5	500	1408	G<133>	-7942.5	500	1458	G<33>	-8692.5	500
1359	G<231>	-7207.5	344	1409	G<131>	-7957.5	344	1459	G<31>	-8707.5	344
1360	G<229>	-7222.5	500	1410	G<129>	-7972.5	500	1460	G<29>	-8722.5	500
1361	G<227>	-7237.5	344	1411	G<127>	-7987.5	344	1461	G<27>	-8737.5	344
1362	G<225>	-7252.5	500	1412	G<125>	-8002.5	500	1462	G<25>	-8752.5	500
1363	G<223>	-7267.5	344	1413	G<123>	-8017.5	344	1463	G<23>	-8767.5	344
1364	G<221>	-7282.5	500	1414	G<121>	-8032.5	500	1464	G<21>	-8782.5	500
1365	G<219>	-7297.5	344	1415	G<119>	-8047.5	344	1465	G<19>	-8797.5	344
1366	G<217>	-7312.5	500	1416	G<117>	-8062.5	500	1466	G<17>	-8812.5	500
1367	G<215>	-7327.5	344	1417	G<115>	-8077.5	344	1467	G<15>	-8827.5	344
1368	G<213>	-7342.5	500	1418	G<113>	-8092.5	500	1468	G<13>	-8842.5	500
1369	G<211>	-7357.5	344	1419	G<111>	-8107.5	344	1469	G<11>	-8857.5	344
1370	G<209>	-7372.5	500	1420	G<109>	-8122.5	500	1470	G<9>	-8872.5	500
1371	G<207>	-7387.5	344	1421	G<107>	-8137.5	344	1471	G<7>	-8887.5	344
1372	G<205>	-7402.5	500	1422	G<105>	-8152.5	500	1472	G<5>	-8902.5	500
1373	G<203>	-7417.5	344	1423	G<103>	-8167.5	344	1473	G<3>	-8917.5	344
1374	G<201>	-7432.5	500	1424	G<101>	-8182.5	500	1474	G<1>	-8932.5	500
1375	G<199>	-7447.5	344	1425	G<99>	-8197.5	344	1475	DUMMY<53>	-8947.5	344
1376	G<197>	-7462.5	500	1426	G<97>	-8212.5	500	1476	DUMMY<54>	-8962.5	500
1377	G<195>	-7477.5	344	1427	G<95>	-8227.5	344	1477	DUMMY<55>	-8977.5	344
1378	G<193>	-7492.5	500	1428	G<93>	-8242.5	500	1478	DUMMY<56>	-8992.5	500
1379	G<191>	-7507.5	344	1429	G<91>	-8257.5	344				
1380	G<189>	-7522.5	500	1430	G<89>	-8272.5	500				
1381	G<187>	-7537.5	344	1431	G<87>	-8287.5	344				
1382	G<185>	-7552.5	500	1432	G<85>	-8302.5	500				
1383	G<183>	-7567.5	344	1433	G<83>	-8317.5	344				
1384	G<181>	-7582.5	500	1434	G<81>	-8332.5	500				
1385	G<179>	-7597.5	344	1435	G<79>	-8347.5	344				
1386	G<177>	-7612.5	500	1436	G<77>	-8362.5	500				
1387	G<175>	-7627.5	344	1437	G<75>	-8377.5	344				
1388	G<173>	-7642.5	500	1438	G<73>	-8392.5	500				
1389	G<171>	-7657.5	344	1439	G<71>	-8407.5	344				
1390	G<169>	-7672.5	500	1440	G<69>	-8422.5	500				
1391	G<167>	-7687.5	344	1441	G<67>	-8437.5	344				
1392	G<165>	-7702.5	500	1442	G<65>	-8452.5	500				
1393	G<163>	-7717.5	344	1443	G<63>	-8467.5	344				
1394	G<161>	-7732.5	500	1444	G<61>	-8482.5	500				
1395	G<159>	-7747.5	344	1445	G<59>	-8497.5	344				
1396	G<157>	-7762.5	500	1446	G<57>	-8512.5	500				
1397	G<155>	-7777.5	344	1447	G<55>	-8527.5	344				
1398	G<153>	-7792.5	500	1448	G<53>	-8542.5	500				
1399	G<151>	-7807.5	344	1449	G<51>	-8557.5	344				
1400	G<149>	-7822.5	500	1450	G<49>	-8572.5	500				

6.4. DISPLAY MODULE DEFAULT POSITION

The default position (display driver, glass, filter order, etc) of the display module is always as follow, when MADCTL's (36h) parameter is 00h. The color filter is always RGB (if color filters are used).

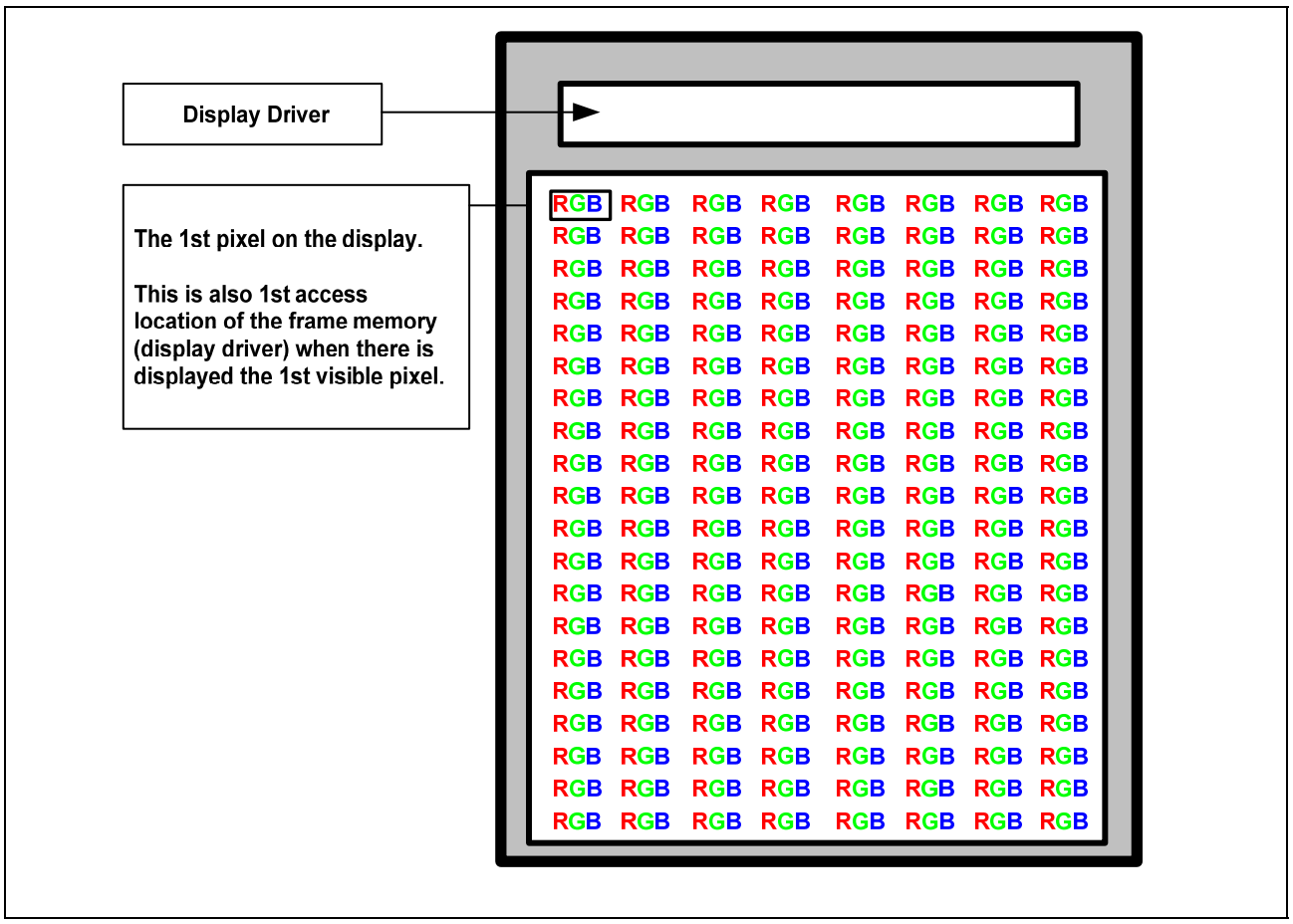

Figure 169. Display module default position